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Design of a CMOS temperature sensor with EEPROM error correction scheme

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ABSTRACT

DESIGN OF A CMOS TEMPERATURE SENSOR WITH EEPROM ERROR CORRECTION SCHEME

By Jin-ku Kang, MSEE, 1990
New Jersey Institute of Technology
Thesis Advisor : Dr. William N. Carr

This thesis describes the design and operation of a CMOS temperature sensor operating at very low power with an EEPROM error correction scheme including the physical layout. This device is designed for applications requiring very low power including biomedical and optically powered device applications. The sensor output is an analog voltage. The temperature sensing cell is implemented with two BJTs having different emitter areas. An op amp dissipating about 300 micro-watts power is designed and is used to amplify the sensor output voltage with a gain of 85dB. A novel EEPROM is used to correct nonlinearity error of the temperature sensor. This scheme uses hot electron injection and the Fowler-Nordheim tunneling mechanism to decrease and increase the floating gate potential, respectively. Programming is done through a bootstrap capacitor and dedicated diode bias control pins. EEPROM error correction is used at three different stages to control (1) the offset voltage, (2) the gain of the op amp, (3) and to correct nonlinearity. The calculated power dissipation is 0.875 to 1mW for the entire chip with a 5V power supply based on simulation by SPICE 2G.5 using MOSIS parameters. The measured power dissipation is 0.776mW at 23°C. The physical database is created using the Mentor Graphics Chipgraph editor. The final chip is 2.2mm×2.2mm including 40 bonding pads. This device was processed using the 2μm CMOS P-well double level poly and double level metal process through the MOSIS silicon foundry brokerage. The experimental and simulated sensitivity of the temperature sensing cell agree closely at 2.3mV/°C and 2.2mV/°C, respectively. In this thesis experimental characterization is presented for the temperature sensor and the EEPROM error correction transistors.

DESIGN OF A CMOS TEMPERATURE SENSOR WITH EEPROM ERROR CORRECTION SCHEME

by
Jin-ku Kang

Thesis submitted to the Faculty of the Graduate School of
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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1

Introduction

This thesis describes the design of a CMOS temperature sensor consuming low power with an EEPROM error correction scheme. Three important design goals have been achieved carefully. First, the temperature sensor has been designed for micropower dissipation of less than 1mW. Second, the CMOS op amp is designed for a large open loop gain, low offset voltage, providing a reduced sensitivity to temperature changes. Thirdly, the correction of errors is accomplished using EEPROM circuit techniques. The design has been implemented into silicon through the MOSIS brokerage Foundry service.

The sensor chosen uses two bipolar junction transistors and combinations of resistors for sensing temperature. This sensing cell is designed for an output voltage of 10.6mV/°C. The output can be directly connected to the CMOS op amp stage

without any loading error.

A cascode single stage CMOS op amp is designed for sensor signal amplification. This op amp uses an MOS input transistor operating in the subthreshold region so that the bias current of $5\mu A$ is selected. This allows the op amp to operate at a micropower level. The cascode circuit with higher open loop gain and higher PSRR has improved temperature insensitivity. Simulated results show that the open loop gain is 18,500 at room temperature, and the PSRR is 98dB.

In current production to reduce the offset voltage of op amp, conventionally resistor trimming based on laser machining is typically used. In this thesis, a novel EEPROM technique is selected instead. The EEPROM permits reprogramming time and time again. Moreover, the EEPROM is used for correcting sensor nonlinearity, and voltage offset. The EEPROM chosen is compatible with standard CMOS processing.

Circuit simulation is accomplished using SPICE 2G.5 with parameters of MOSIS $2\mu m$ CMOS P-well process. Layout is based on the $2\mu m$ CMOS P-well double poly double and metal process design rules. The sensor chip has been fabricated as a MOSIS Tinychip project.

The following is a brief, chapter-by-chapter discussion of material presented in this thesis.

Chapter 2 deals with the outline of this temperature sensor. A block diagram and device specification is presented.

Chapter 3 discusses basic temperature sensing principles, deals with selected circuit and analysis of the simulated results. This chapter also covers the error correction circuit placed within the sensor cell.

Chapter 4 is devoted to the design of the CMOS micropower op amp, including principles of the CMOS op amp, design and analysis of the op amp circuit selected.

Chapter 5 presents the EEPROM structures and their application to reduce the offset voltage of the op amp. The novel structure of the EEPROM and its physical principles is described. Layout for the EEPROM circuit is presented and discussed.

Chapter 6 describes the chip design, layout and measurement procedures.

Chapter 7 presents the experimental results of the chip fabricated by the MOSIS foundry facility.

Chapter 8 summarizes the device characteristics and presents the conclusions.

Chapter 2

Design Specifications

2-1. Performance specification

1. This chip will be fabricated by MOSIS 2μm P-well double poly and double metal process.

2. This chip must operate on a 5V single power supply.

3. The offset voltage of the op amp must be reduced to the value of μV range by EEPROM offset control scheme.

4. Good linearity of voltage within 0.01% corresponding to temperature could be obtained by EEPROM correction scheme.

5. Chip output sensitivity of 10mV/°C is desired.

6. Output should drive an external ADC circuit.

The performance specification is summarized in the Table (2-1-1).

2-2. Design outline

This temperature sensor consists of the temperature sensing block amplification part and error correction circuits. The temperature sensing block circuit is composed of two bipolar junction transistors which have different emitter areas, the current source and resistors. The basic idea of sensing a temperature is that the voltages which are proportional to the temperature can be detected at the collector of bipolar junction transistors. And this voltage can be amplified to the voltage level which can be applied to an analog to digital converter circuit. A CMOS op amp operating with less than 1mW power is designed for amplification of the sensor output.

Due to the I-V charateristic of the diode, the voltage can not be exactly linear. Therefore, for correcting this nonlinearity and calibrating, a compensation circuit should be placed on the chip. A novel EEPROM structure is selected for this. The circuit diagram is shown in Fig (2-1-1). This chip is operating at single 5V supply and consumes maximum 1mW power. Temperature sensing range is from -50 to 150 degrees in Centigrade. The simulation of this circuit is done by the SPICE 2G.5 using MOSIS 2μm CMOS parameters and the physical layout is done using Mentor Graphics Chipgraph on Apollo workstation in NJIT Microelectronics laboratory. This device could be implemented within an optically powered sensors system.[2-1] In the optically powered sensors approach, optical power is transmitted to the remote sensor via the fiber link so that adequate level of optically generated electrical power is available for data acquisition and transmission. Experimentally 1-2mW of electrical

power is available at the sensor using commercially avilable laser diodes to supply optical power into fibers. Therefore every discrete system in the sensor cell should be designed for micro-power operation.

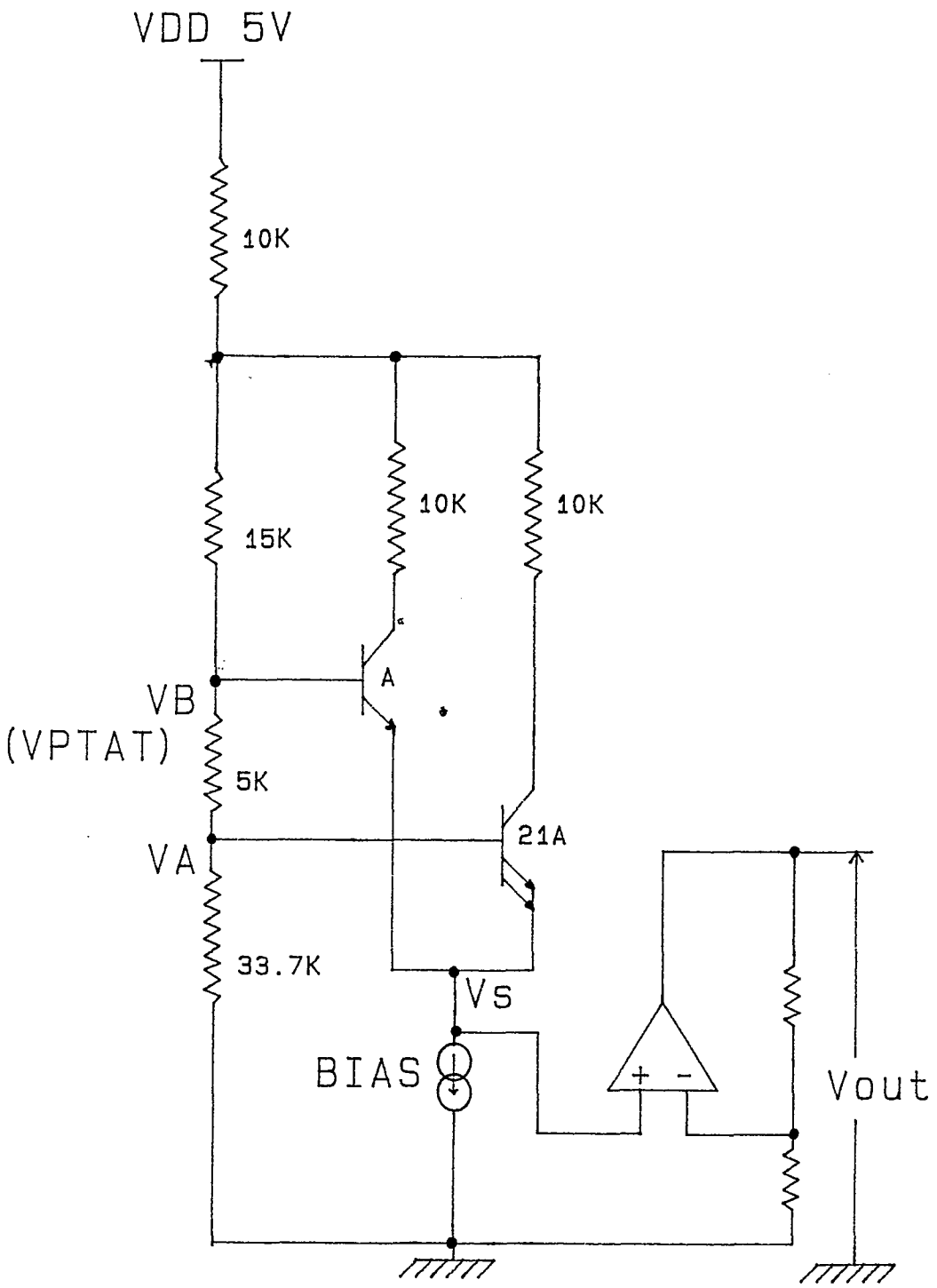


Fig (2-1-1). Circuit diagram of the temperature sensor.

Items	*Specifications*
Technology	MOSIS CMOS 2μm p-well double poly, double metal process(SCPE)
Power supply	+ 5.0V
Power consumption	$\leq$1mW
Temperature sensing range	-50 to 150°C
Offset voltage of op amp	μV range
Gain of op amp	$\geq$80dB
PSRR of op amp	$\geq$90dB(@DC)
EEPROM programming voltage	$\pm$15V
Linearity error of the sensor	$\pm$0.01%
Output voltage(V_{out})	10mV/°C
Output drive resolution	8 bit ADC

Table (2-1-1). Design specifications.

Chapter 3

Temperature Sensing Cell Design

This chapter describes the temperature sensing cell design. The temperature dependence of a semiconductor diode derives from the ideal diode equation for a p-n junction diode:

$$I_D = I_S[exp(qV/kT) - 1] \qquad 3-1.1$$

where I_S is the saturation current.

3-1 Review of Temperature Sensing Circuit Techniques

There are three sensing techniques that could be used within the design constraints of this project. One sensing technique uses the base-emitter voltage, V_{be} of a bipolar transistor and is described in section 3-1.1. Another method for measuring temperature with bipolar elements is the single-transistor temperature sensor technique, i.e.

measuring the base-emitter voltage V_{be} described in section 3-1.2. A third technique is called PTAT sensing and is based on sensing of the base-emitter voltage difference ΔV_{be} of two transistors. In this design the technique of section 3-1.2 has been chosen for implementation.

3-1.1 Single-Transistor Temperature Sensor

When we apply a constant collector current I_c, we can measure a base-emitter voltage which decreases almost linearly with temperature T. This behavior can be approximated by Eq.3-1.2 :

$$V_{be} = 1.27V - CT \qquad 3-1.2$$

where C is a constant that depends on the process. The value 1.27V in Eq.3-1.2 is independent of process parameter, bias current, and transistor size. This important property permits the transistor to be used as a temperature sensor.

3-1.2 Proportional To Absolute Temperature PTAT Sensors

We may measure the absolute temperature from the differential voltage ΔV_{be} between the base-emitter voltages of two transistor sensors if the ratio of the emitter areas of two temperature transistor sensors is carefully selected. When the two temperature transistors are at the same temperature, we may find:

$$\Delta V_{be} = V_{be1} - V_{be2} = (kT/q)ln[(I_{C1}/I_{C2})(I_{S2}/I_{S1})] \qquad 3-1.3$$

Since the saturation currentI_S, is proportional to the emitter area :

$$\Delta V_{be} = (kT/q)ln(pr) \qquad 3-1.4$$

where p is the ratio of collector currents, r is the ratio of saturation currents between two transistor sensors. Here the differential voltage ΔV_{be} is proportional to the absolute temperature. Fig.(3-1-1) shows the principle of the PTAT temperature sensor per Meijer[3-2]. We may find :

(1). I_o, the output current is PTAT, if R is temperature independent. (2). Due to the interconnection of the base of Q1 and Q2, I_o is independent of the bias current I_{bias}. The voltage vs. temperature curve of the circuit in Fig(3-1-1) is shown in Fig (3-1-2). For a detailed description of Fig (3-1-1), refer to [3-2].

3-1.3 CMOS Weak Inversion Temperature Sensor

The I-V characteristic of MOS transistor in the weak inversion region is given as:

$$I = (\frac{W}{L}) \times I_{D0} \times exp[\frac{qV_{GS}}{nkT}] \qquad 3-2.1$$

The equation clearly shows a temperature dependence. Therefore, we can realize a temperature sensing device using this characteristic. Fig (3-1-3) shows a CMOS temperature sensor circuit with weak inversion bias [3-3]. The all-complementary current mirrors and P-channel MOS transistors which are used as resistors form the sensor circuit [3-4]. We may fix the drain current ratio by specifying the beta ratio

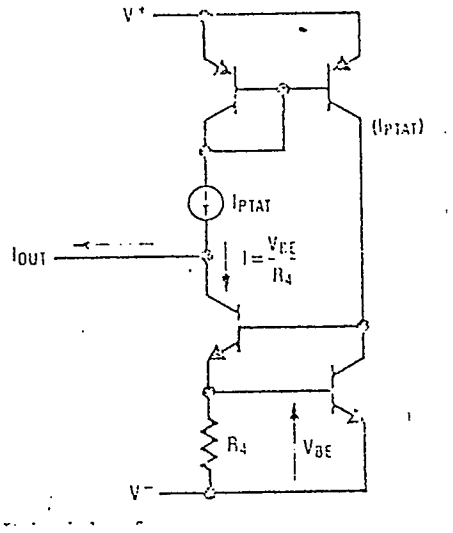


Fig (3-1-1) PTAT circuit per Meijer.[3-2]

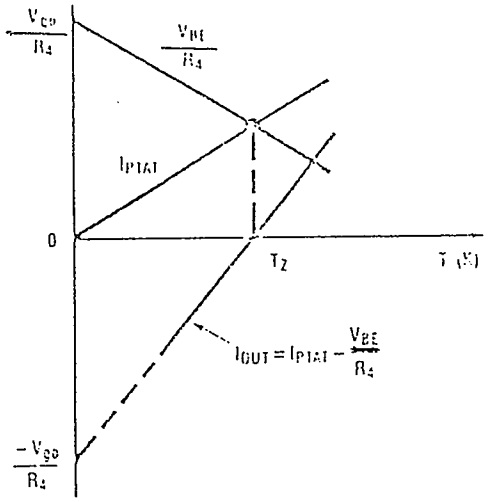
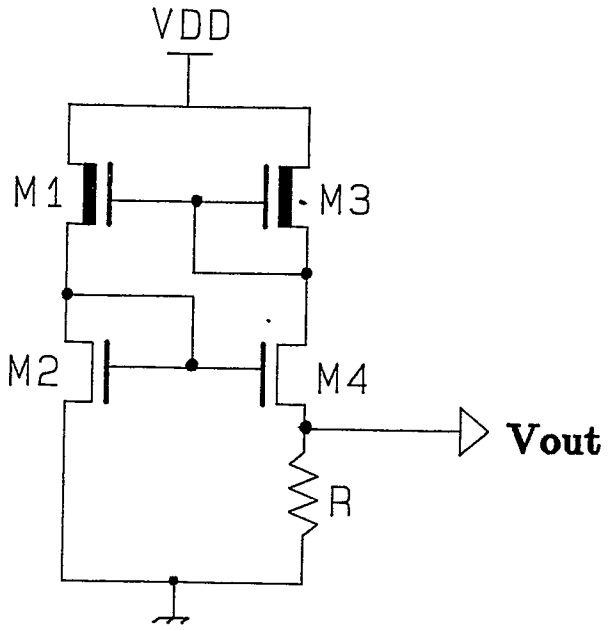
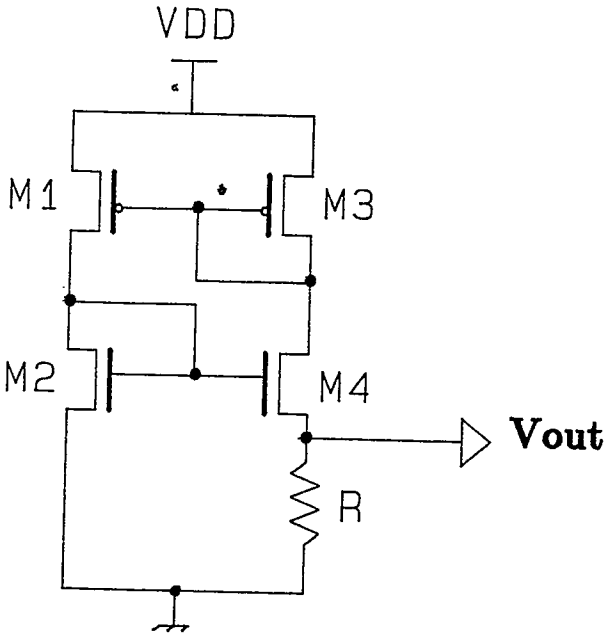


Fig (3-1-2) Voltage curve characteristic of the PTAT.[3-2]



(a). NMOS version



(b). CMOS version

Fig (3-1-3) CMOS weak inversion temperature sensor circuit.

of MP1 and MP3 as :

$$\frac{(W/L)_{M1}}{(W/L)_{M3}} = \frac{(W/L)_{M2}}{(W/L)_{M4}} \qquad 3-2.2$$

From Fig.3-1-3 we find :

$$V_{GS2} = V_{GS4} - V_o \qquad 3-2.3a$$

Thus $\rightarrow$

$$V_o = V_{GS2} - V_{GS4} \qquad 3-2.3b$$

From Eq.3-2.1 we can derive :

$$(q/kT)(V_{GS2} - V_{GS4}) = ln[\frac{(W/L)_{M1}}{(W/L)_{M3}} / \frac{(W/L)_{M2}}{(W/L)_{M4}}] \qquad 3-2.4$$

Combining Eq.3-2.3 and Eq.3-2.4 we get $\rightarrow$

$$V_o = V_{GS2} - V_{GS4} = (kT/q)ln[\frac{(W/L)_{M1}}{(W/L)_{M3}} / \frac{(W/L)_{M2}}{(W/L)_{M4}}] \qquad 3-2.5$$

The output voltage, V_o of this sensor circuit is linearly dependent on the temperature T to this first order approximation.

3-2 Temperature Sensing cell design

The voltage of a forward-biased semiconductor junction diode V_F has long been known to be a stable and fairly linear temperature indicator. However , the wide production spread of this V_F has prevented the diode from becoming a popular temperature sensor because it is not easily specified or precisely calibrated. Other drawbacks

of the silicon diode are its low sensitivity and its nonlinearity, on the order of 1 to 3 percent over a 100°C temperature range.

When two silicon junctions are operated at different current densities (J_1, J_2), the differential voltage(V_{F1} - V_{F2}) is a predictable, accurate, and linear function of the temperature. The current density flowing through a diode is proportional to the junction area as:

$$I_D = J_S \times A_D \times exp(qV/kT) \qquad 3-3.1$$

where J_S is the saturation current density, A_D is the P-N junction area, and V is the applied voltage on the P-N junction diodes.

From Eq.3-3.1 we get:

$$V = (kT/q) \times ln(\frac{I_D}{J_S \times A_D}) \qquad 3-3.2$$

$$V_{F1} = (kT/q) \times ln(\frac{I_1}{J_{S1} \times A_1}) \qquad 3-3.3$$

$$V_{F2} = (kT/q) \times ln(\frac{I_2}{J_{S2} \times A_2}) \qquad 3-3.4$$

Thus we get :

$$V_{F2} - V_{F1} = (kT/q) \times ln(\frac{J_{S1}}{J_{S2}}) \qquad 3-3.5$$

Comparing Eq.3-3.2 and Eq.3-3.5, we find that we can even use a single P-N junction diode as a temperature sensor. But the sensing precision will depend on a current density that is temperature dependent and slightly nonlinear. We can get a wider sensing temperature range by using two diodes as temperature sensors to reduce the

nonlinearity caused by the temperature effect. Example circuits of this idea are presented in Fig (3-2-1) and Fig (3-2-2). However, this turns out to be impractical because of the small output voltage level V_{F2}-V_{F1}.

The I_{PTAT}(Current Proportional to Absolute Temperature) circuit technique in Fig (3-1-1) and Fig (3-1-2) avoids some of the drawbacks of two diode pairs, since the resulting current is inherently calibrated, when it is properly trimmed at any one temperature. It can be shown that the total output current varies linearly with the temterature. This circuit has several weaknesses, however. It is necessary to trim accurately both the gain and the offset, for at any given temperature one cannot tell which is contributing more to the output current. Also, a current-mode output is susceptible to noise pickup from any source of ac, or by leakage of dc current. Worst of all, when the resistors have a linear temperature coefficient, they can cause nonlinear(quadratic) current errors over a wide temperature range, in addition to the slope errors shown in Fig(3-1-2).[3-2]

A recently published circuit design[3-5] takes advantage of the basic V_{PTAT} principle. The circuit of Fig(3-2-3) avoids the drawbacks of the other schemes, and provides benefits also. Within the circuit of Fig (3-2-3) a V_{PTAT} at room temperature is generated, and two V_F's are substracted from it. The resulting voltage V_{out} is amplified by an op amp to provide an output voltage that is linearly proportional to temperature. From Fig (3-2-3), we have a-b-c-d.

$$V_{R1} = V_{be2} - V_{be1}$$

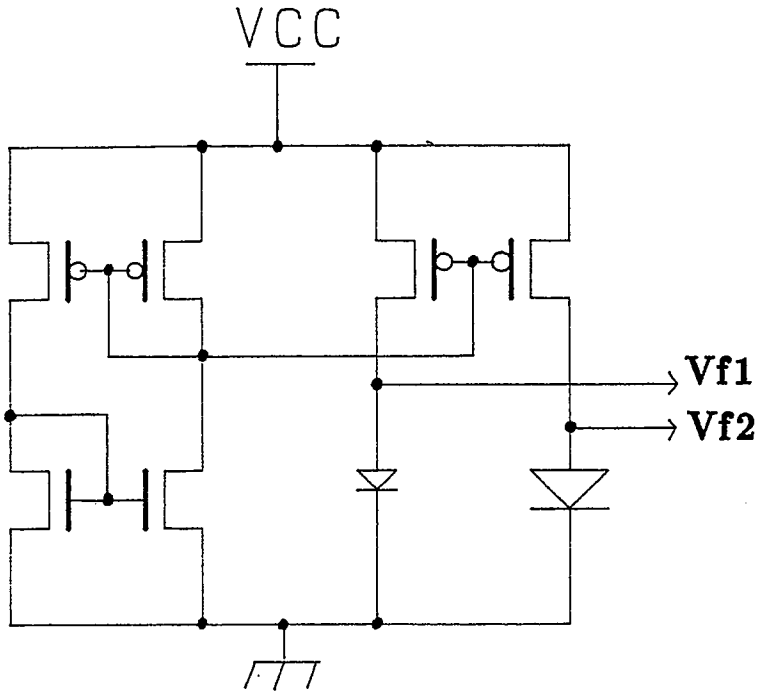


Fig (3-2-1) CMOS differential diode temperature sensor circuit I.

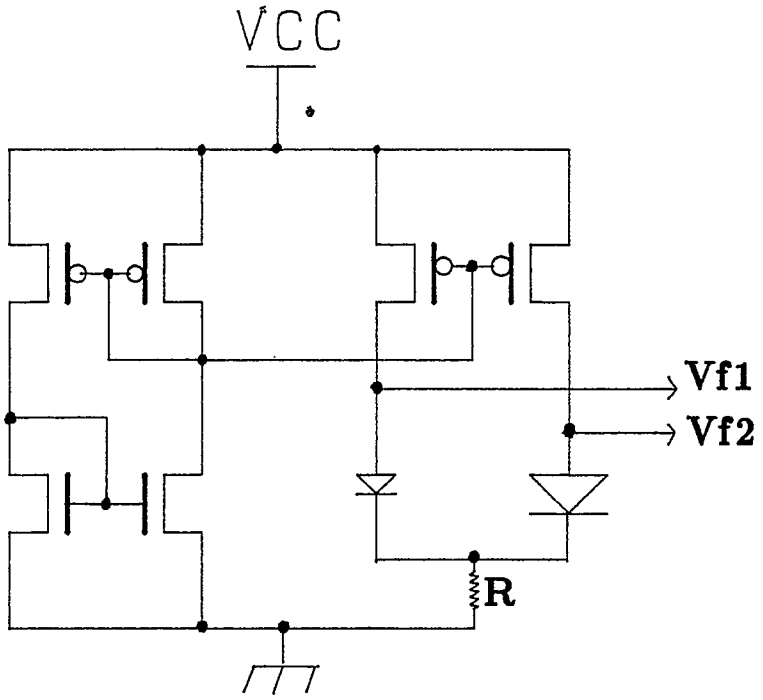


Fig (3-2-2) Diode temperature sensor circuit II.

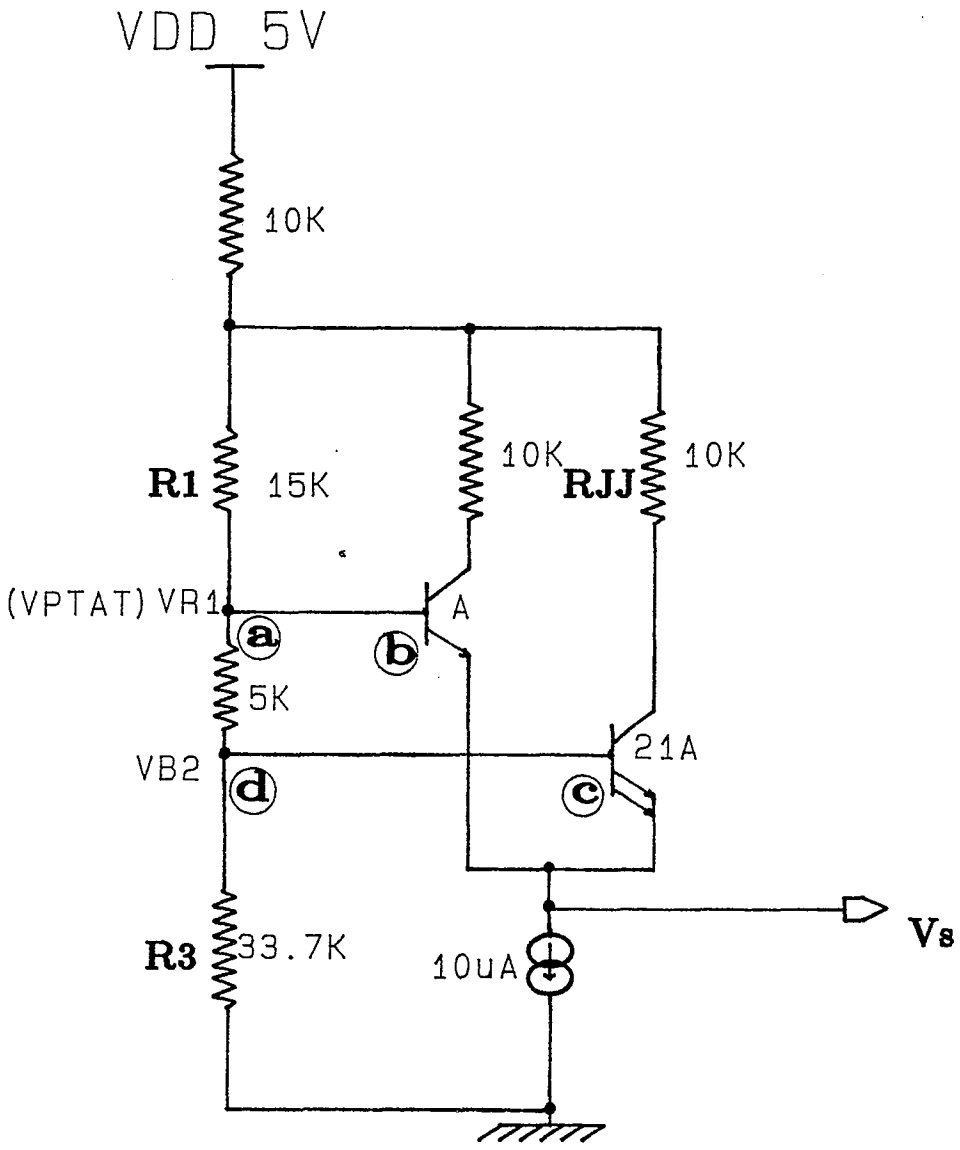


Fig (3-2-3) Circuit diagram of the temperature sensor selected.

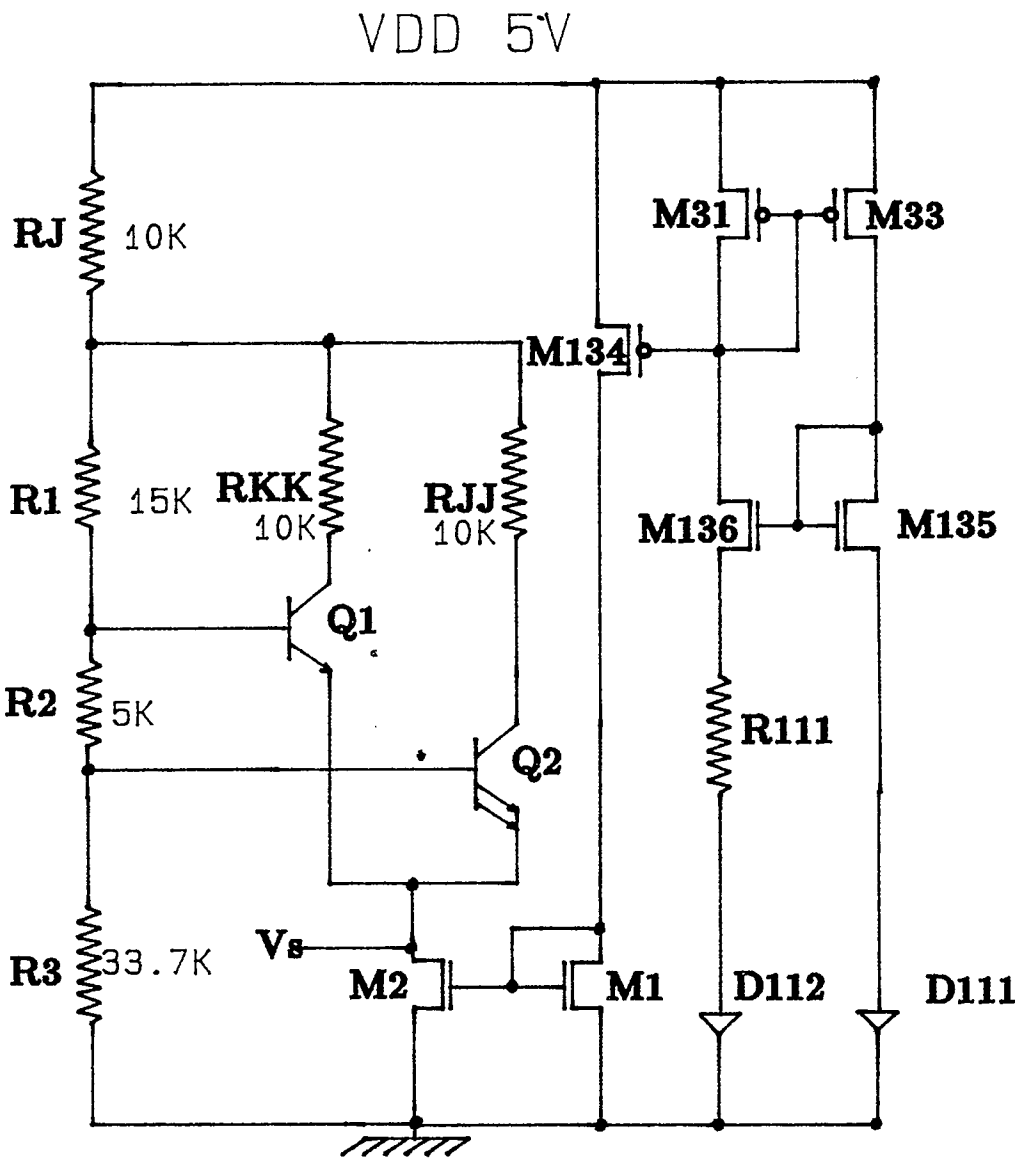


Fig (3-2-3 A) Circuit diagram of the temperature sensor for SPICE input file

and

$$V_{R1} = kT\ln(n)$$

This gives,

$$V_{be2} - V_{be1} = kT\ln(n)$$

where n is the ratio of the emitter area between two bipolar transistors. Since Q1's emitter area is twenty one times as large as that of Q2, the voltage across R1 in Fig (3-2-3) is given by

$$V_{R1} = (kT/q)\ln 21$$

Thus, V_{R1} is PTAT, and if the i_b of two bipolar transistors is neglected, V_{B2} is also PTAT. V_S is the output voltage of the temperature sensing cell and $V_S = V_{R1}$ - $V_{be,A}$. The simulated net sensitivity of the voltage V_s is about 2.2mV/°C. There is a curvature compensation circuit added to compensate for the inherent nonlinearities of V_F versus temperature. Chapter 5 covers this in detail.

3-3 Simulation and Analysis of Temperature Sensing Circuit

A current source is designed to produce 10μA, its principle is described in chapter 4.[3-6]. Fig (3-3-1) shows the SPICE simulation input file for the circuit of Fig (3-2-1). The results of the simulation show an average output voltage V_S of 2.2mV/°C over the range -50 - 100°C. Table (3-3-1) shows the output voltage of V_S versus temperature. Fig (3-3-2) shows the output voltage of V_S for the circuit of Fig (3-2-3) from -50

```
**TEMPERATURE SENSOR CIRCUIT**
VCC 1 0 5.0
**TRDESCRIPTION**
RJJ 1 11 10K
RKK 11 34 10K
RJ 11 13 10K
RK 11 12 10K
R1 34 35 5K
R2 35 36 5K
R3 36 0  33.7K
Q1 13 35 37 NP
Q2 12 36 37 NP 21
.OPTIONS ITL1=500 ITL5=0
.OPTIONS LIMPTS=500
**IBIAS CIRCUIT**
M31 133 132 1 1 P W=8U L=6U
M33 111 132 1 1 P W=8U L=6U
M134 132 132 1 1 P W=8U L=6U
M135 133 133 134 134 N W=4U L=36U
M136 132 133 135 135 N W=4U L=36U
D111 134 0 D1
D112 136 0 D1 10
R111 135 136 5K
M1 111 111 0 0 N W=4U L=36U
M2 37 111 0 0 N W=4U L=36U
.OPTIONS NOPAGE
.WIDTH OUT 80
.TEMP -50 0 50 100 150
**MODEL DEFINITION**
.MODEL D1 D IS=1.0E-14 VJ=0.8
.MODEL NP NPN IS=1.0E-14 BF=10
.MODEL N NMOS LEVEL=2.00000 RSH=20 TOX=520.000E-10
+ LD=0.280000U XJ=0.400000U CJ=4.5E-4 CJSW=6.0E-10
+ UO=200.000 VTO=0.587229 CGSO=5.2E-10 CGDO=5.2E-10
+ NSUB=4.575777E15 VMAX=10.E4 KP=3.848050E-05
+ MJ=0.5 MJSW=0.33 NFS=5.033532E11 GAMMA=0.922197
+ PHI=0.60000 UEXP=1.001000E-03 UCRIT=999000
+ DELTA=1.59123 LAMBDA=2.208002E-02 NEFF=1.001000E-02
+ NSS=0.000000E+00 TPG=1.00000 CGBO=8.0E-10 PB=0.700000
.MODEL P PMOS LEVEL=2.00000 RSH=55 TOX=520.000E-10
+ LD=0.280000U XJ=0.400000U CJ=3.6E-4 CJSW=6.0E-10
+ UO=100.000 VTO=-0.784085 CGSO=4E-10 CGDO=4E-10
+ NSUB=2.534947E14 VMAX=10.E4 KP=1.394594E-05
+ MJ=0.5 MJSW=0.33 NFS=8.870574E11 GAMMA=0.536443
+ PHI=0.600000 UEXP=0.171457 UCRIT=51857.9
+ DELTA=1.89818 LAMBDA=4.720123E-02 NEFF=1.001000E-02
+ NSS=0.000000E+00 TPG=-1.00000 CGBO=1.3E-09 PB=0.750000
.END
```

Fig (3-3-1) SPICE input file of the temperature sensing part circuit.

Temperature (°C)	*Output voltage(V_S) (volt)*	ΔmV	*Sensitivity (mV/°C)*
-50	2.280		
0	2.390	110	2.2
50	2.500	110	2.2
100	2.610	110	2.2
150	2.740	130	2.6

Table (3-3-1) Simulated output voltage(V_S) vs. temperature for Fig(3-3-3) circuit.

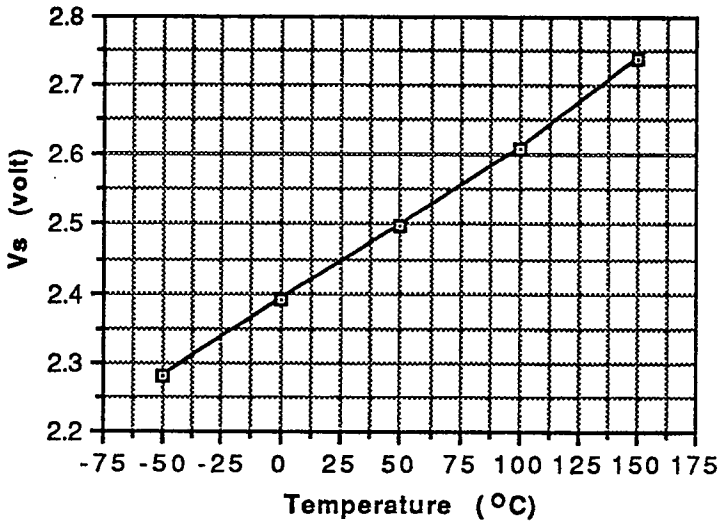


Fig (3-3-2) Simulated output voltage(V_S) vs. temperature in Fig(3-2-3).

to 150°C. As shown in Table (3-3-1) nonlinearity occurs at temperature over 110°C. This is mainly caused by the inherent nonlinearity of the diode I-V characteristic. The error analysis of simulated data by variation of resistors by ±10%, β-value of two lateral BJTs by ±50% and all other parameters by ±10% is also illustrated in Fig (3-3-3), (3-3-4), (3-3-5) and (3-3-6). As indicated in those figures, the slope is not affected by the process variations. We will compensate for these errors by the offset correction circuit to be developed in Chapter 5. As far as the layout of the sensing cell is concerned, poly silicon(doped) is used for resistors and lateral bipolar transistors are implemented in a P-well process. These BJTs have a relatively lower β value than the vertical BJT. Therfore, SPICE simulation has been done assuming the typical value of β=10.

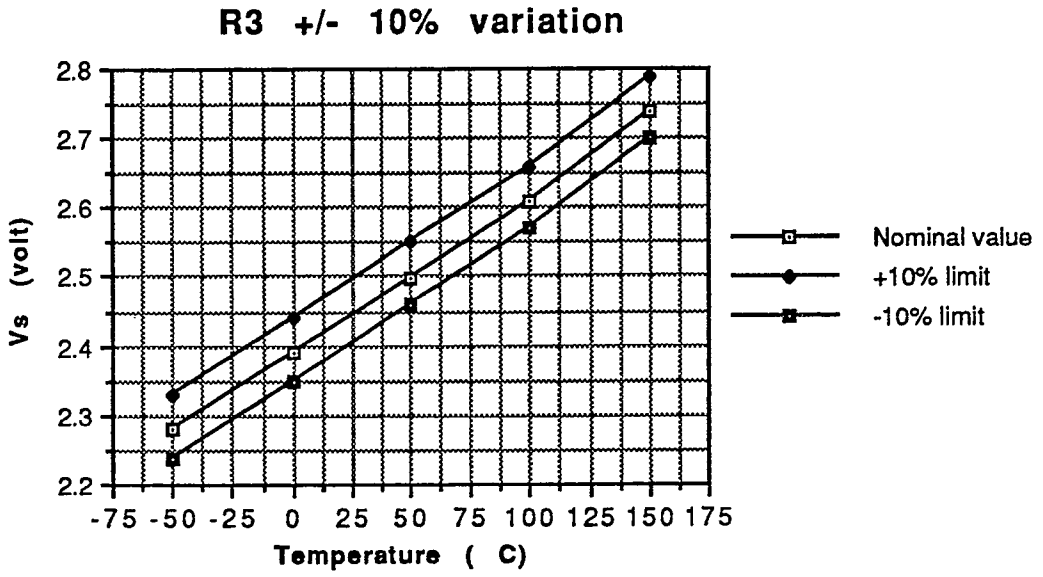


Fig (3-3-3) Simulated error analysis by ±10%variation of R_3 in Fig (3-2-3)

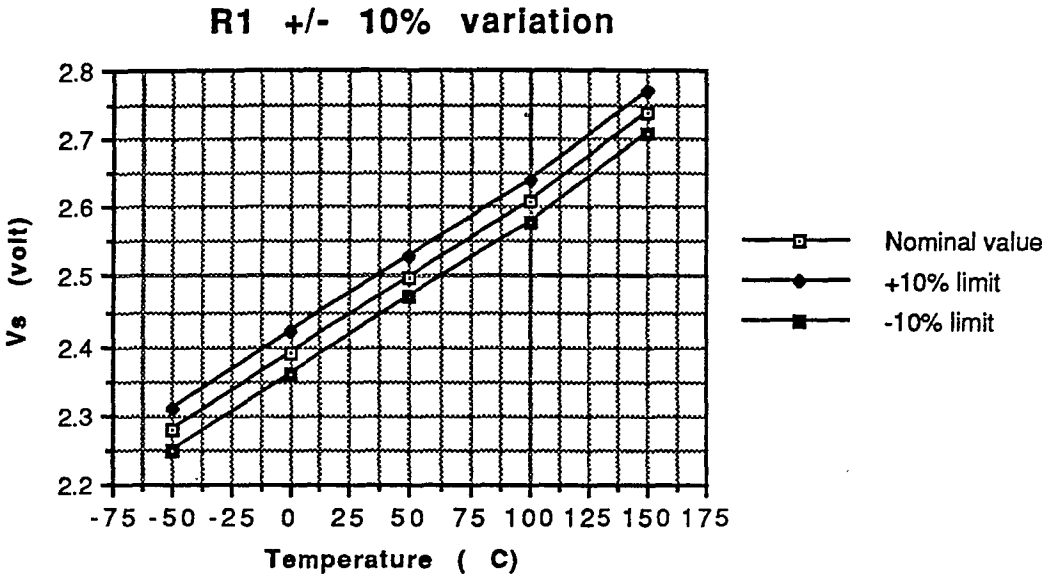


Fig (3-3-4) Simulated error analysis by $\pm 10\%$variation of R_1 for Fig(3-3-3) circuit.

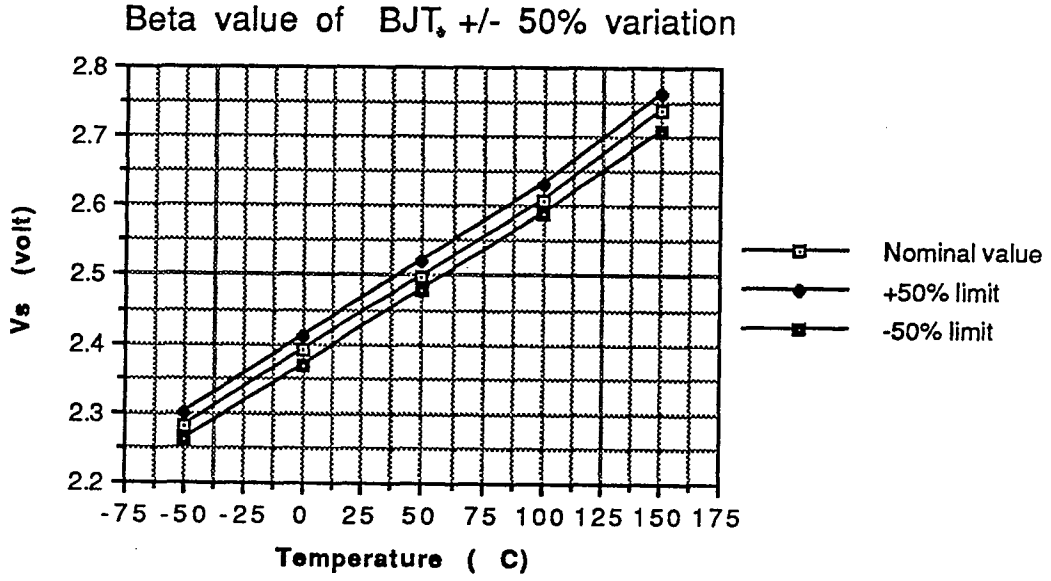


Fig (3-3-5) Simulated error analysis by $\pm 50\%$variation of β of BJT

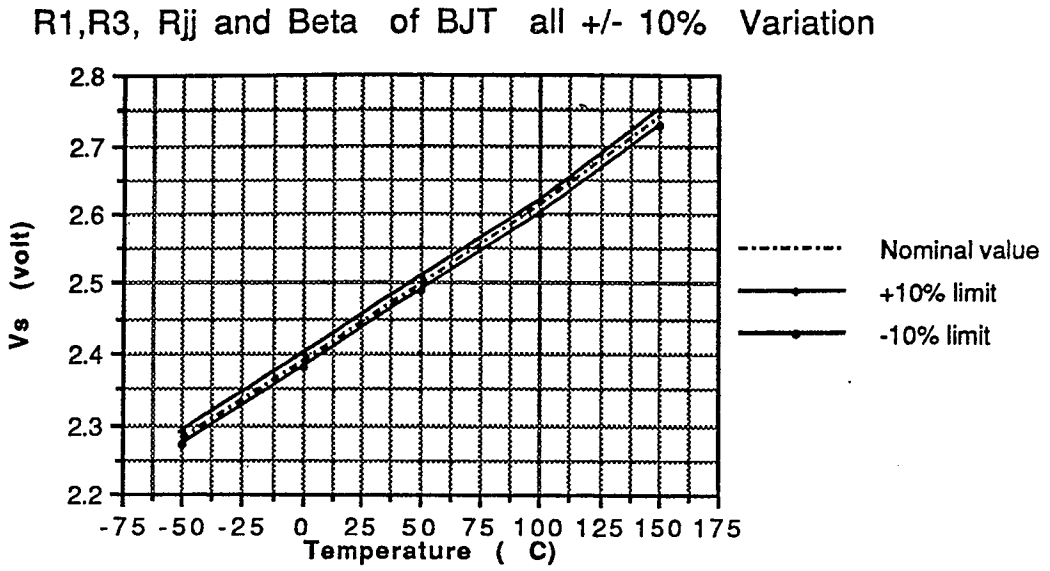


Fig (3-3-4) Simulated error analysis by $\pm 10\%$variation of R_3, R_1,R_{jj} and β of BJT.

for Fig(3-3-3) circuit.

Chapter 4

CMOS Op amp Design

The output signals of the temperature sensing cell are not large enough to be read directly. It needs to be amplified to a higher level to be connected to the next stage such as an analog-to-digital converter. The design outline for an op amp for amlifying the sensing block output is; (1) low-power consuming, (2) high gain, high PSRR , (3) insensitive to temperature change and (4) lower offset voltage. The object of this chapter is to present the concept and circuit design of the low-power CMOS cascode two stage op amp for the temperature sensor. Detailed background can be found in several references [4-1],[4-2], [4-3], and [4-4].

4-1 Principle of CMOS Two-Stage Op Amp

The design of a simple two-stage CMOS op amp is shown in Fig (4-1-1). By using

the small signal model given in Fig (4-1-2a) and the simplified model given in Fig (4-1-2b), the parameters of this model can be derived as follows:

$$g_{mI} = g_{m1} = g_{m2} \qquad 4-1.1$$

$$R_I = R_2 = r_{ds2}//r_{ds4} \qquad 4-1.2$$

$$C_I = C_2 = C_{gd2} + C_{gd4} + C_{gs5} + C_{db2} + C_{db4} \qquad 4-1.3$$

$$g_{mII} = g_{m5} \qquad 4-1.4$$

$$R_{II} = R_3 = r_{ds5}//r_{ds6} \qquad 4-1.5$$

and

$$C_{II} = C_3 = C_{gd6} + C_{bd5} + C_{db6} + C_L \qquad 4-1.6$$

The key equations pertaining to the CMOS two-stage op amp design are given as;

$$A_o = g_{mI}g_{mII}R_IR_{II} = \frac{g_{m2}g_{m5}(r_{ds2}r_{ds4})(r_{ds5}r_{ds6})}{(r_{ds2}+r_{ds4})(r_{ds5}+r_{ds6})} \qquad 4-1.7$$

$$= [(\frac{1}{\lambda_2+\lambda_4})(\frac{2K_{N'}W_1}{I_{D1}L_1})^{1/2}][(\frac{1}{\lambda_5+\lambda_6})(\frac{2K_{P'}W_5}{I_{D5}L_1})^{1/2}] \qquad 4-1.8$$

$$\simeq (\frac{1}{2\lambda^2})(\frac{K_{N'}K_{P'}W_1W_5}{I_{D1}I_{D5}L_1L_5})^{1/2} \qquad 4-1.9$$

The Gain-Band Width is :

$$GB = \frac{g_{mI}}{C_c} = \frac{g_{m1}}{C_c} = \frac{1}{C_c}(\frac{2K_{N'}W_1I_{D1}}{L_1})^{1/2} \qquad 4-1.10$$

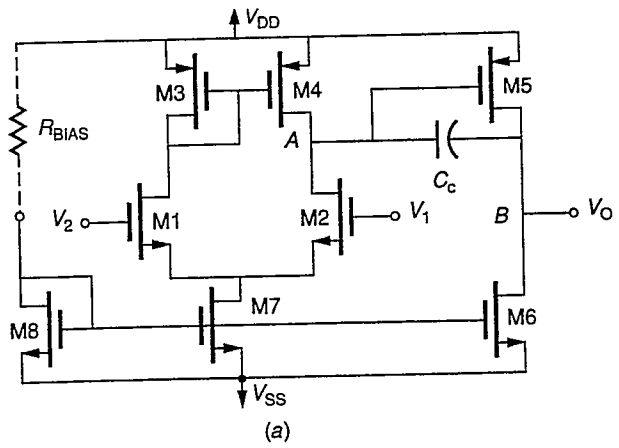
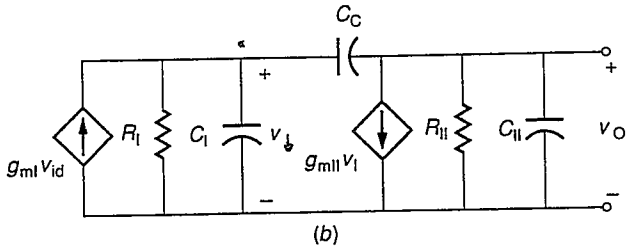
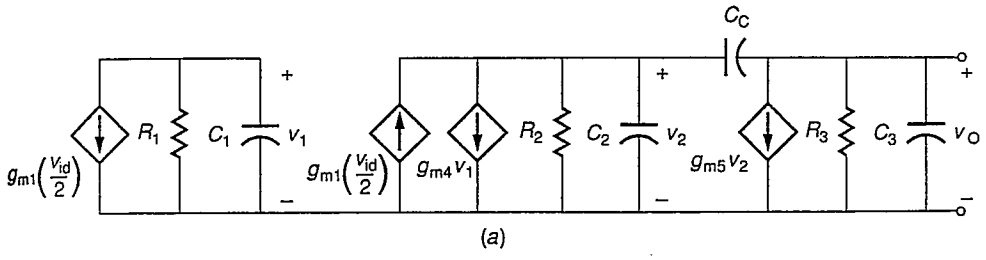


Fig (4-1-1) Two stage CMOS op amp.[4-2]



(a). Small signal model



(b). Simplified model

Fig (4-1-2) Small signal model[4-2]

The slew rate, maximum output voltage rate of the amplifier is :

$$Slew - rate = SR = \frac{I}{C_c} \qquad 4-1.11$$

where I is the smaller of I_{c1} or I_{c5}. Suppose M4 in Fig (4-1-1) is operating in the saturation region and all other devices operate in saturation either by their connection or by external potentials applied to the inputs or outputs. For matching and symmetry, we must choose $W_1/L_1 = W_2/L_2$ and $W_3/L_3 = W_4/L_4$. If we force V_{GS3} to be equal to V_{GS5} by the following relationship

$$\frac{W_3}{L_3} = (\frac{W_5}{L_5})(\frac{I_3}{I_5}) \qquad 4-1.12$$

then since $I_5 = I_6, I_3 = I_4$, and $W_3/L_3 = W_4/L_4$, we may express Eq. 4-1.10 as

$$\frac{W_4}{L_4} = (\frac{W_5}{L_5})(\frac{I_4}{I_6}) \qquad 4-1.13$$

However, because $I_4 = 0.5I_7$ and $I_7/I_8 = (W_7/L_7)/(W_8/L_8)$, the condition for M4 to remain in saturation becomes

$$\frac{W_4}{L_4} = (\frac{W_5/L_5}{2})(\frac{W_7/L_7}{W_6/L_6}) = (\frac{W_5/L_5}{2})(\frac{I_7}{I_6}) \qquad 4-1.14$$

To illustrate the design of a two-stage CMOS op amp such as that given in Fig(4-1-1), assume that the desired specifications are $A_o \geq 50,000$, GB=1MH_Z, and the slew rate is 2μV. Assume that the device parameters are $K_{N'} = 2K_{P'} = 25\mu A/V^2$, λ=0.01V^{-1} and C_c=5pF. From the slew rate specification and C_c, we see that I_{D1}=5μA. If we pick I_{D5} equal to 50μA, W_1/L_1 =4.0. Since M1 and M2 are matched , W_2/L_2 is also

4.0. W_5/L_5 can be found from Eq.(4-1.9) to be 4.5. And from Eq.(4-1.13) W_5/L_5 is 0.45. Finally, one can solve for the value of W_8/L_8 necessary to establish a resonable current in M8 and solve for W_6/L_6 and W_7/L_7 using the current ratios. The small signal input resistance, R_{id}, of the CMOS op amp is infinity because of the infinite gate resistance. The output resistance is equal to the parallel combination of r_{ds5} and r_{ds6} and is 1MΩ for this example. For detailed description, refer to [4-2].

4-2. Cascode Op amp

Performance limitations of the two stage op amp include insufficient gain, limited stable bandwidth, and a poor power-supply rejection ratio. There are three ways in which the gain could be increased: (1) add an additional gain stage, (2) increase the transconductance of the first or second stage and (3) increase the output resistance seen by the first or second stage. Generally to increase r_{out} rather than g_m is considered to be more efficient. This could be achieved by a cascode op amplifier. Cascode op amps also offer the possibility of improved PSRR performance.

$$PSRR = \frac{\Delta V_{DD} A_o}{\Delta V_o} \qquad 4-2.1$$

This parameter becomes more important if power for the temperature sensor is supplied to optically or by indirect methods. Detail descriptions of cascode op amp are referred to in [4-1],[4-2],[4-3] and [4-4].

4-3. Micropower op amp design

Amplifiers operating in the weak inversion region of transistor operation are gaining attention because of their low-power applications. The usefulness of amplifiers operating in this region is not only the very low power supply currents that they draw but also their very low power supply voltage operation. Going back to Fig(4-1-1), and now assume operation in the weak inversion region (subthreshold region). Fig (4-3-1) illustrates the operating region of weak inversion in the I-V characteristic of a MOS transistor. The linear portion of the curve represents the subthreshold region. The subthreshold current is given as

$$I_D = (\frac{W}{L})I_{DO}exp[\frac{qV_{GS}}{nkT}] \qquad 4-3.1$$

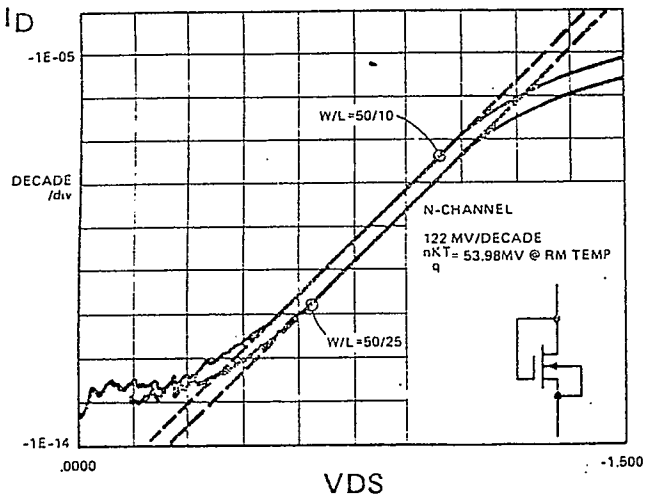
From this equation, the transconductance can be easily derived as

$$g_m = \frac{I_D}{nkT/q} \qquad 4-3.2$$

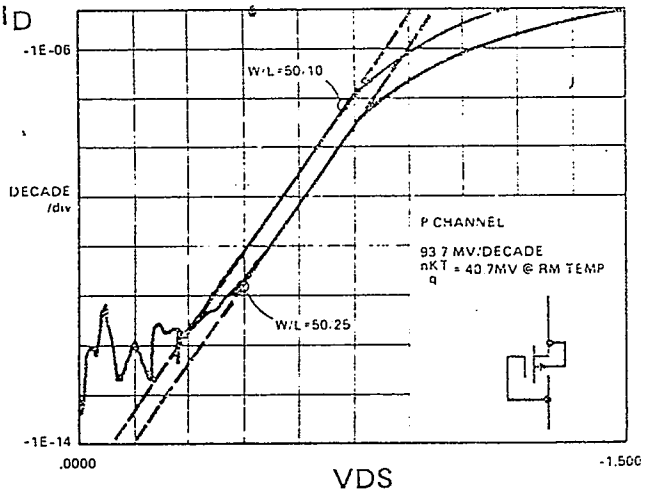
where n is determined by the process parameters.

This result is very interesting in that it shows a linear relationship between transconductance and drain current. Futhermore, the transconductance is independent of device geometry. The transconductance of the MOS device operating in the weak inversion region behaves like that of a bipolar transistor. The expression for the output resistance in weak inversion is

$$r_o = \frac{1}{\lambda I_D} \qquad 4-3.3$$



(a). NMOS transistor



(b). PMOS transistor

Fig (4-3-1) I-V characteristics in the subthreshold region.[4-7]

With these things in mind, the dc gain of the two-stage op amp in Fig (4-1-2) operating in weak inversion is same as eq.(4-1.7), and given as

$$A_o = g_{m2}g_{m5}(\frac{r_{o2}r_{o4}}{r_{o2}+r_{o4}})(\frac{r_{o5}r_{o6}}{r_{o5}+r_{o6}}) \qquad 4-3.4$$

$$\simeq \frac{1}{n_2 n_6 (kT/q)^2(\lambda_2+\lambda_4)(\lambda_5+\lambda_6)} \qquad 4-3.5$$

The gain bandwidth is

$$GB = \frac{g_{m1}}{C_c} = \frac{I_{D1}}{(nkT/q)C_c} \qquad 4-3.6$$

The slew rate is

$$SR = \frac{I_{D5}}{C_c} = 2\frac{I_{D1}}{C_c} \qquad 4-3.7$$

Comparing with the equations we have in section (4-1), the weak- inversion operating op amp is fully applicable. The disadvantage of this amplifier is its inability to provide large output currents while still maintaining micro-power consumption when quiescent. The solution to this problem can be found in [4-5]. When operating transistors in the susthreshold region, the gate-source voltage applied for proper circuit operation can easily be below the threshold voltage by 100mV or more. The V_{DS} saturation voltage is typically below 100mV also. As a result of these small voltage drops, the op amp operating in weak-inversion can easily function with a 1.5V supply, provided that the signal swings are kept small. Because of this low-voltage operation, this op amp is very applicable to implantable, biomedical applications, where battery

4-4. Selected OP Amp circuit for the temperature sensor

4-4-1. Circuit diagram and its operation

Selected circuits of op amps for the temperature sensor are shown in Fig(4-4-1). A cascode op amp is selected for higher gain and improved PSRR, and the push-pull output stage scheme is used to drive a low resistive output load. About 5μA of the bias current is designed to flow in the circuit. This ensures that the transistors M7, M8, M11 and M12 are operating in the weak inversion region. The transistors M31, M33, M34, M35, M36, D1 and D2 comprise the bias circuit, and transistors M1, M9, M10, and M14 comprise the push-pull output stage

4-4-2. Bias circuit design

The problem of establishing bias conditions that are independent of temperature and supply voltage variations and, to the extent possible, process variations is of particular importance in MOS circuits. In order to achieve power supply independence, one must refer the bias circuit to some potential other than the supply voltage. And to achieve the insensitivity to temperature change, various methods of biasing are presented.[4-8]. A V_T-referenced current source is implemented in the op amp circuit for current biasing. The circuit diagram is shown in Fig (4-4-2). Diodes D1 and D2 have areas that differ by a factor 10, and the feedback loop forces them to operate at the same bias current. As a result, the difference between the two V_fs must appear across the

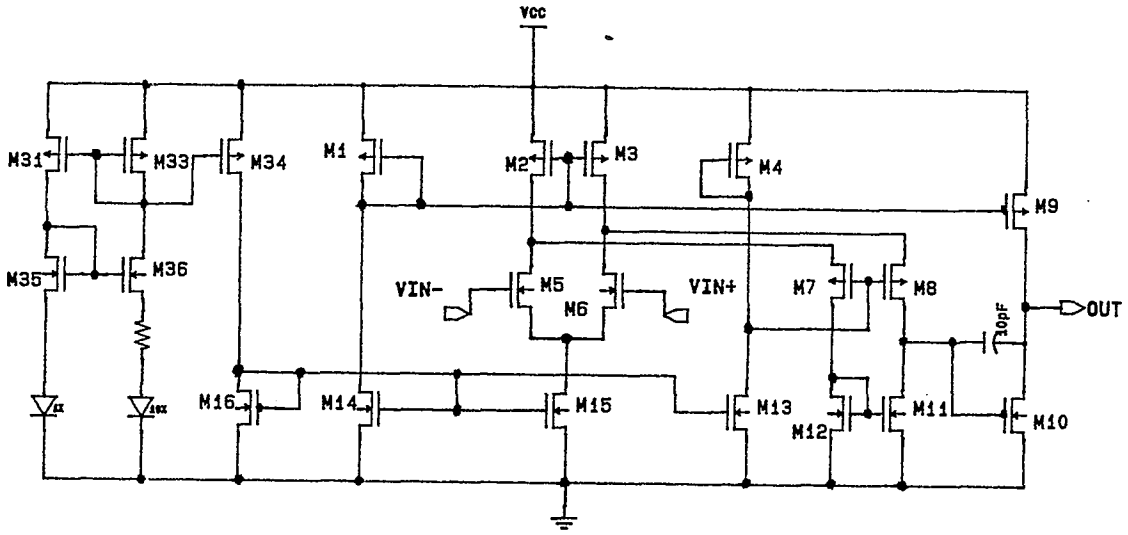
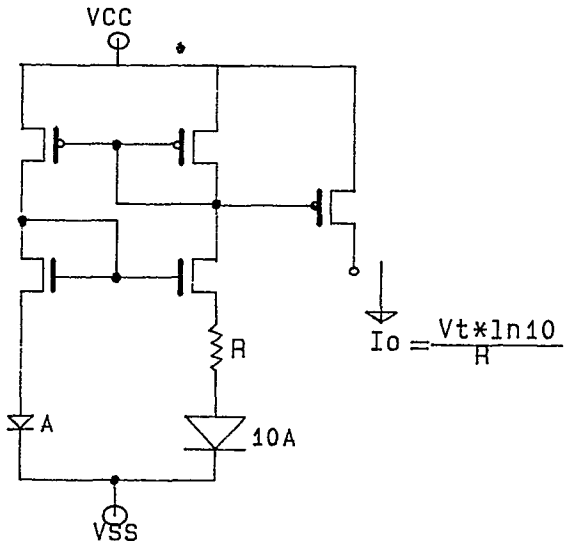


Fig (4-4-1) Op amp circuit.



BIAS CIRCUIT

Fig (4-4-2) Selected bias circuit.[4-8]

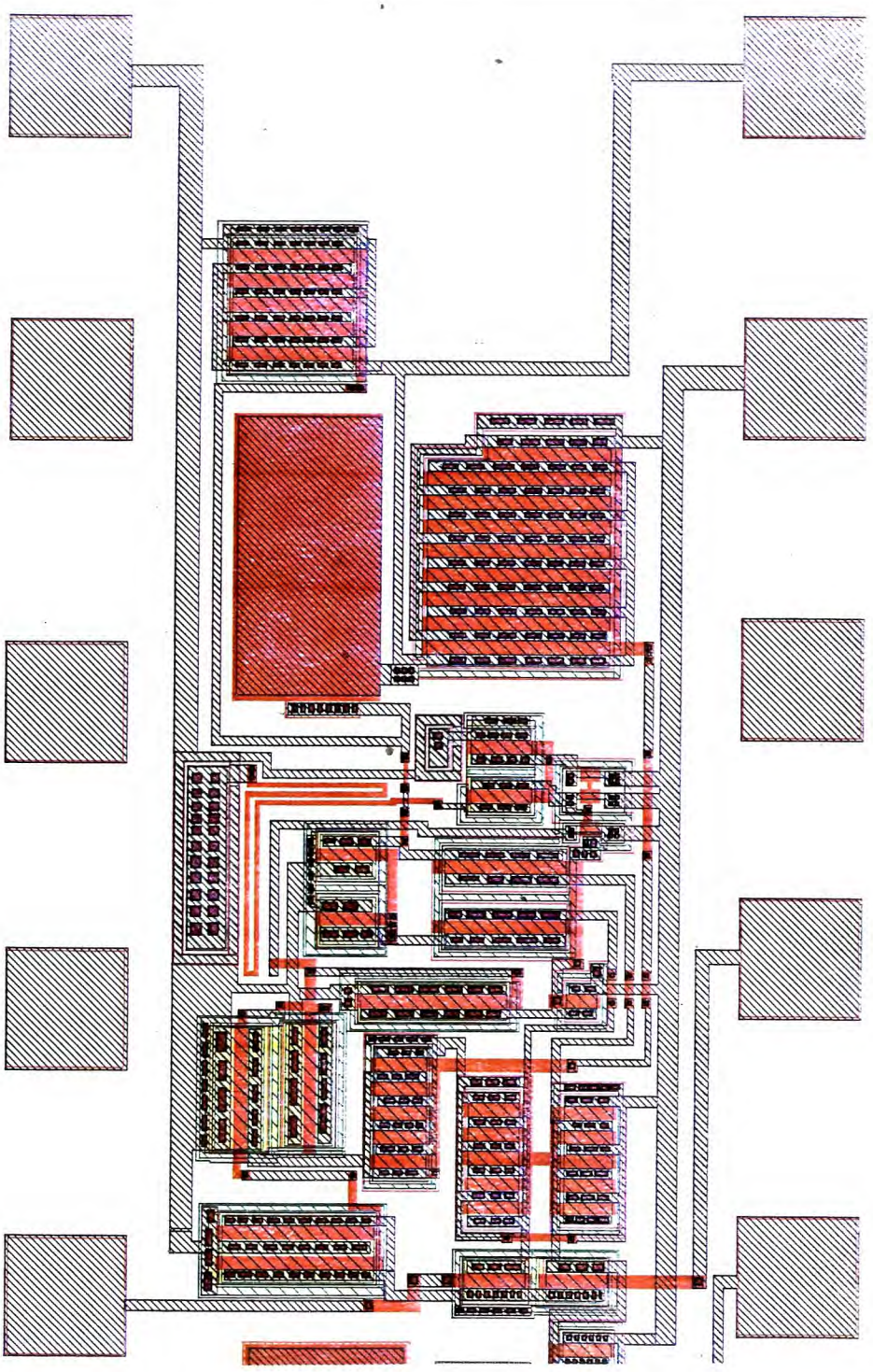


Fig (4-4-3) Layout of the selected op amp.

resistor R. The resulting current is given by

$$I = \frac{V_T \ln(n)}{R} \qquad 4-4-1$$

Where $V_T = (kT/q)$. V_T has a positive temperature coefficient and the positive temperature coefficient of the resistor(poly) gives a relatively temperature independent output current. Therfore, we can achieve a power-independent and temperature-independent current source in the op amp. Because this op amp is on the same chip as the temperarure sensing part, temperature-independent characteristica are very important. The layout of the op amp is shown in Fig (4-4-3).

4-4-3. Simulation data analysis of the Op amp circuit

The input file of SPICE for the op amp is shown in Fig(4-4-4). At 27°C, the typical output shape of the op amp is shown in Fig(4-4-5). Fig(4-4-6) shows the simulated bias current and expected data vs. temperature. During simulation, we assumed that resistance is not changed with temperature. Table (4-4-1) shows the output gain and power consumption vs. temperature. As we expected from Eq.(4-3-6), the gain is decreasing as temperature increases.

4-5. Design of the gain stage and its analysis

To control the temperature sensor output level, appropriate gain should be determined to amplify the voltage level of the sensing cell. The circuit diagram of the closed loop non-inverting amplifier selected[4-9] is illustrated in Fig (4-5-1). The gain

```
***CASCODE CMOS OP AMP CIRCUIT***
**BIAS CIRCUIT**
VCC 1 0 2.50
VSS 0 100 2.5
**TR DESCRIPTION**
M31 33 32 1 1 P W=5U L=16U
M33 11 32 1 1 P W=5U L=16U
M34 32 32 1 1 P W=5U L=16U
M35 33 33 34 34 N W=50U L=6U
M36 32 33 35 35 N W=50U L=6U
D1 34 100 D1
D2 36 100 D1 10
R1 35 36 5K
M32 11 11 100 100 N W=100U L=10U
**MODEL DEFINITION**
.MODEL D1 D IS=1.0E-16 VJ=0.8
**OPAMP CIRCUIT**
VIN+ 6 0 0.0
VIN- 5 0 0
**TRANSISTOR DESCRIPTION**
M1 2 2 1 1 P W=200U L=10U
M2 3 2 1 1 P W=200U L=10U
M3 4 2 1 1 P W=200U L=10U
M4 8 8 1 1 P W=25U  L=10U
M5 3 5 7 7 N W=50U L=10U
M6 4 6 7 7 N W=50U L=10U
M7 9 8 3 1 P W=100U L=10U
M8 10 8 4 1 P W=100U L=10U
M9 12 2 1 1 P W=2400U L=10U
M10 12 10 100 100 N W=100U L=10U
CC 10 12 10PF
CL 12 0 1.2PF
M11 9 9 100 100 N W=42.5U L=10U
M12 10 9 100 100 N W=42.5U L=10U
M13 8 11 100 100 N W=100U L=10U
M14 2 11 100 100 N W=100U L=10U
M15 7 11 100 100 N W=200U L=10U
M16 11 11 100 100 N W=100U =10U
.TF V(12) VIN+
.DC VIN+ -0.03 0.03 0.01
.OPTIONS NOPAGE
.WIDTH OUT 80
.PRINT DC V(12)
.TEMP   0  50  100 150
**MODEL DEFINITION**
.MODEL N NMOS LEVEL=2.00000 RSH=20 TOX=520.000E-10
+ LD=0.280000U XJ=0.400000U CJ=4.5E-4 CJSW=6.0E-10
+ UO=200.000 VTO=0.587229 CGSO=5.2E-10 CGDO=5.2E-10
+ NSUB=4.575777E15 VMAX=10.E4 KP=3.848050E-05
+ MJ=0.5 MJSW=0.33 NFS=5.033532E11 GAMMA=0.922197
+ PHI=0.60000 UEXP=1.001000E-03 UCRIT=999000
+ DELTA=1.59123 LAMBDA=2.208002E-02 NEFF=1.001000E-02
+ NSS=0.000000E+00 TPG=1.00000 CGBO=8.0E-10 PB=0.700000
.MODEL P PMOS LEVEL=2.00000 RSH=55 TOX=520.000E-10
+ LD=0.280000U XJ=0.400000U CJ=3.6E-4 CJSW=6.0E-10
+ UO=100.000 VTO=-0.784085 CGSO=4E-10 CGDO=4E-10
+ NSUB=2.534947E14 VMAX=10.E4 KP=1.394594E-05
+ MJ=0.5 MJSW=0.33 NFS=8.870574E11 GAMMA=0.536443
+ PHI=0.600000 UEXP=0.171457 UCRIT=51857.9
+ DELTA=1.89818 LAMBDA=4.720123E-02 NEFF=1.001000E-02
+ NSS=0.000000E+00 TPG=-1.00000 CGBO=1.3E-09 PB=0.750000
```

Fig (4-4-4) SPICE input file of the selected op amp.

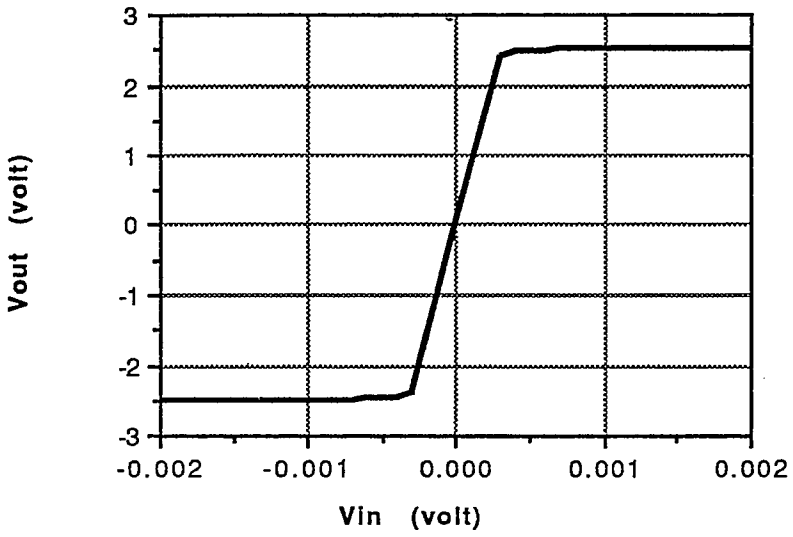


Fig (4-4-5) Simulated output characteristics of open loop op amp.

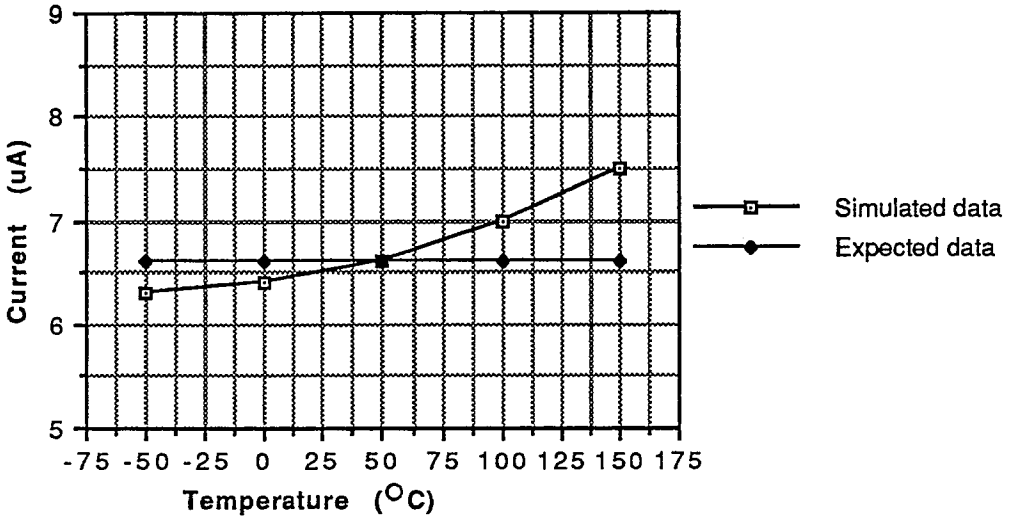


Fig (4-4-6) Simulated bias current vs. temperature.

Temperature (°C)	*Open loop gain($V_{out}/\Delta V_{in}$)*	*Power consumption (μW)*
-50	19600	320
0	19300	332
50	17800	347
100	12200	369
150	7900	440

Table (4-4-1) Simulated output gain vs. temperature.

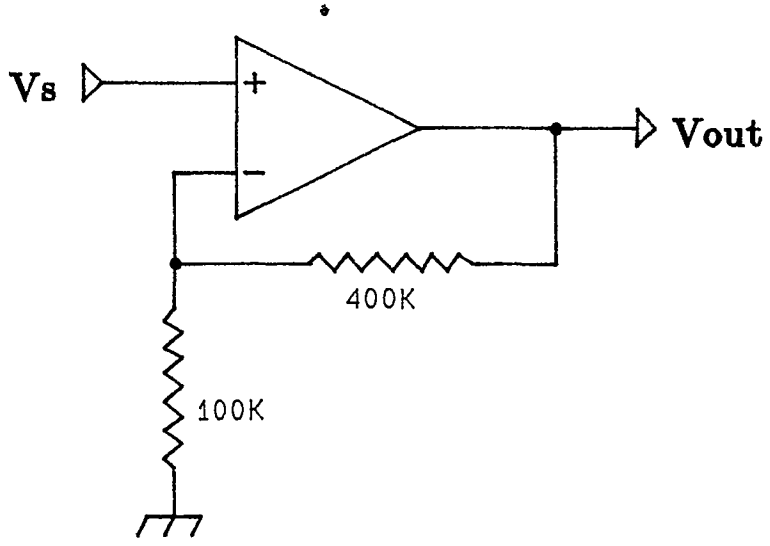


Fig (4-5-1) Circuit diagram of the gain stage.

```
***CLOSED LOOP NON-INVERTING OP AMP CIRCUIT***
**BIAS CIRCUIT**
VCC 1 0 5
**TR DESCRIPTION**
M31 33 32 1 1 P W=5U L=16U
M33 11 32 1 1 P W=5U L=16U
M34 32 32 1 1 P W=5U L=16U
M35 33 33 34 34 N W=50U L=6U
M36 32 33 35 35 N W=50U L=6U
D1 34 0 D1
D2 36 0 D1 10
R1 35 36 5K
M32 11 11 0 0 N W=100U L=10U
**MODEL DEFINITION**
.MODEL D1 D IS=1.0E-16 VJ=0.8
**ED DIFF AMP**
VA 6 0 2.5
RQ1 1 100 10K
RQ2 100 0 10K
RAA 5 12 400K
RBB 5 100 100K
**TRANSISTOR DESCRIPTION**
M1 2 2 1 1 P W=200U L=10U
M2 3 2 1 1 P W=200U L=10U
M3 4 2 1 1 P W=200U L=10U
M4 8 8 1 1 P W=25U  L=10U
M5 3 5 7 7 N W=50U L=10U
M6 4 6 7 7 N W=50U L=10U
M7 9 8 3 1 P W=100U L=10U
M8 10 8 4 1 P W=100U L=10U
M9 12 2 1 1 P W=2000U L=10U
M10 12 10 0 0 N W=100U L=10U
CC 10 12 10PF
CL 12 0 1.2PF
M11 9 9 0 0 N W=42.5U L=10U
M12 10 9 0 0 N W=42.5U L=10U
M13 8 11 0 0 N W=100U L=10U
M14 2 11 0 0 N W=100U L=10U
M15 7 11 0 0 N W=200U L=10U
M16 11 11 0 0 N W=100U L=10U
.DC VA  2.25 2.75 0.05
.OPTIONS NOPAGE
.OPTIONS ITL1=500 ITL5=0
.OPTIONS LIMPTS=50000
.WIDTH OUT 80
.PRINT DC V(5) V(6) V(100) V(12)
.TEMP  -50 0 50 100 150
**MODEL DEFINITION**
.MODEL N NMOS LEVEL=2.00000 RSH=20 TOX=520.000E-10
+ LD=0.280000U XJ=0.400000U CJ=4.5E-4 CJSW=6.0E-10
+ UO=200.000 VTO=0.587229 CGSO=5.2E-10 CGDO=5.2E-10
+ NSUB=4.575777E15 VMAX=10.E4 KP=3.848050E-05
+ MJ=0.5 MJSW=0.33 NFS=5.033532E11 GAMMA=0.922197
+ PHI=0.60000 UEXP=1.001000E-03 UCRIT=999000
+ DELTA=1.59123 LAMBDA=2.208002E-02 NEFF=1.001000E-02
+ NSS=0.000000E+00 TPG=1.00000 CGBO=8.0E-10 PB=0.700000
.MODEL P PMOS LEVEL=2.00000 RSH=55 TOX=520.000E-10
+ LD=0.280000U XJ=0.400000U CJ=3.6E-4 CJSW=6.0E-10
```

Fig (4-5-2) SPICE input file of the gain stage.

factor is approximately 4. Because the output driving current of the op amp is small for operating in the micro-watt power region, we have to choose relatively high resistance values for resistors in the closed loop of the amplifier. A p-well resistor is used for these resistors in the chip design. The SPICE input file is given in Fig (4-5-2) and simulated output voltage curve vs. temperature is illustrated in Fig (4-5-3).

Temperature (°C)	*Output voltage(V_{out}) (volt)*	ΔmV	*Sensitivity (mV/°C)*
-50	1.450		
0	1.980	530	10.6
50	2.510	530	10.6
100	3.040	530	10.6
150	3.670	630	12.5

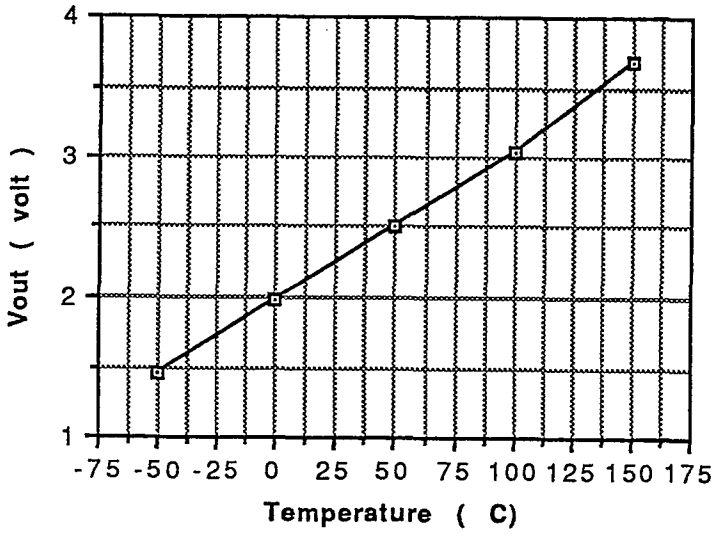


Fig (4-5-3) Simulated output voltage(V_{out}) vs. temperature

Chapter 5

Error Correction with EEPROM Scheme

In this chapter the error correction of gain and offset of the temperature sensor is described. As is conventional for error correction for a temperature sensor, the resistor trimming method is used. While the trimmimg method is irreversible, new error correction method can be programmed as often as necessary. This idea is based on EEPROM. The principle of new EEPROM, its applications and simulation data after implementing within the sensor are discussed.

5-1. Review of Floating Gate structure on silicon

The first EPROM was developed using a heavily doped polysilicon as the floating

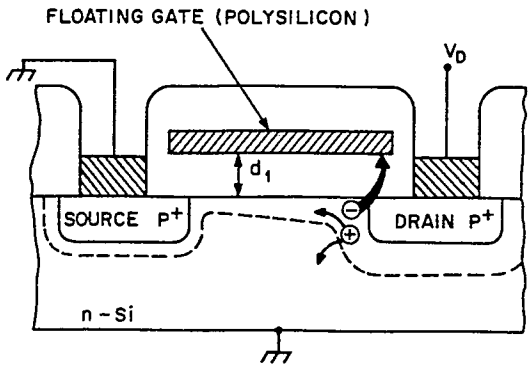


Fig (5-1-1) FAMOS structure.[5-1]

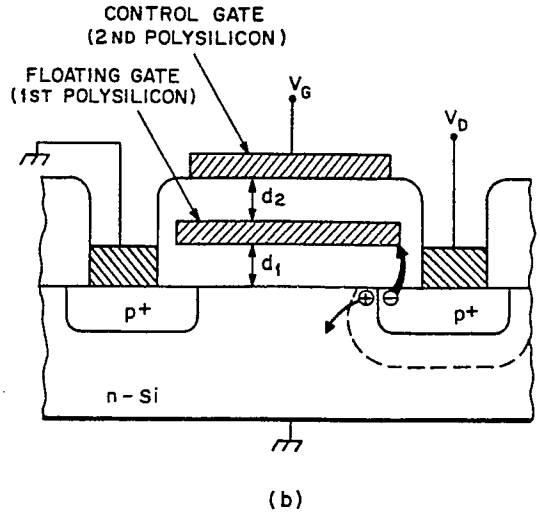
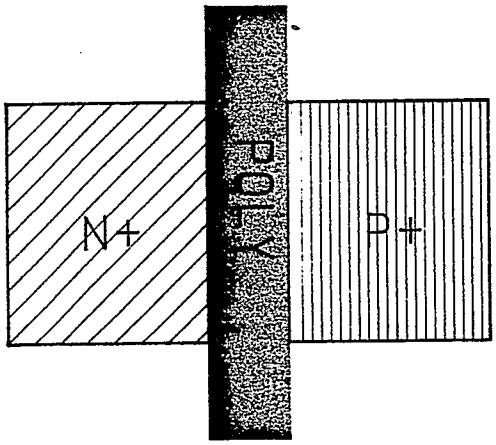
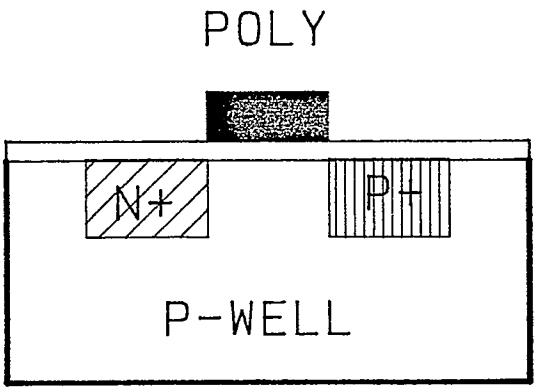


Fig (5-1-2) SAMOS structure.[5-4]



(a). Top view



(b). Cross section

Fig (5-2-1) New EEPROM structure.[5-5]

gate material. The vertical structure is shown in Fig (5-1-1). The device is known as a floating-gate avalanche injection MOS memory(FAMOS). To inject charge into the floating gate, the drain junction is biased to avalanche breakdown, and electrons in the avalanche plasma are injected from the drain region into the SiO_2. To erase the FAMOS memory, UV light or X-rays are used. For electrical erasing, the Stacked-gate Avalanche Injection MOS (SAMOS, EEPROM) memory with double level polysilicon gate has been proposed and is shown in Fig (5-1-2). The external control gate makes electrical erasing possible and improves the writing efficiency. Details are in [5-1], [5-2], [5-3] and [5-4].

5-2. The principle of the new EEPROM and its application

The new floating gate memory(EEPROM) uses hot-electron injection (Avalanche injection) to decrease the floating gate voltage and electron tunneling from the floating gate to increase its voltage.[5-5] This is similar to the approach used in many digital EEPROMs. Fig (5-2-1) shows the top and cross sectional views of the current injection structure.

The diode conducts an avalanche current at a reverse bias, hot electron injection onto the gate is accomplished by inducing avalanche breakdown in the diode and applying a bias voltage on the bootstrap capacitor which makes the voltage difference between the diode $N+$ region and the floating gate greater than 25Volts. Electrons are removed from the gate when the voltage between the gate and the $P+$ region is

below -11Volts. This is done by the Fowler-Nordheim tunneling mechanism.[5-6][5-7][5-8].

Fig (5-2-2) shows the circuit diagram of the new EEPROM. To see how it operates, we can draw the equivalent circuit of this structure shown in Fig (5-2-3). In this figure, C_B is much much bigger than C_{eq} and R_{eq} is ideally infinite while avalanche is off. When the avalanche current starts to flow into the floating gate, R_{eq} could be some high resistance. If we want to lower the floating gate voltage, it can be accomplished by applying a square pulse of 25Volts. By R-C circuit response, Fig (5-2-4) is understood. Because of high resistance RC time is so big that the voltage drop of the floating gate during the duration of 25Volts of input is very small. Actually by controlling the duration time of the input pulse (programming time) we can control the voltage drop of the floating gate.

If we want the floating gate voltage to be higher, applying the square pulse of -15 volts in the input makes the voltage on the floating gate change. Fig (5-2-5) shows the voltage increase on the floating gate.

The floating gate voltage does not change ideally forever before programming. However, there is a leakage to the passivation layer, or to the metal layer, or the other layers with a rate of 0.06%/decade at 25°C and 1%/decade at 80°C reported for FAMOS.[5-5]

One possible application of the EEPROM is shown in Fig (5-2-6). It is for trimming the offset voltage of an MOS op amp. The main cause of the offset voltage of

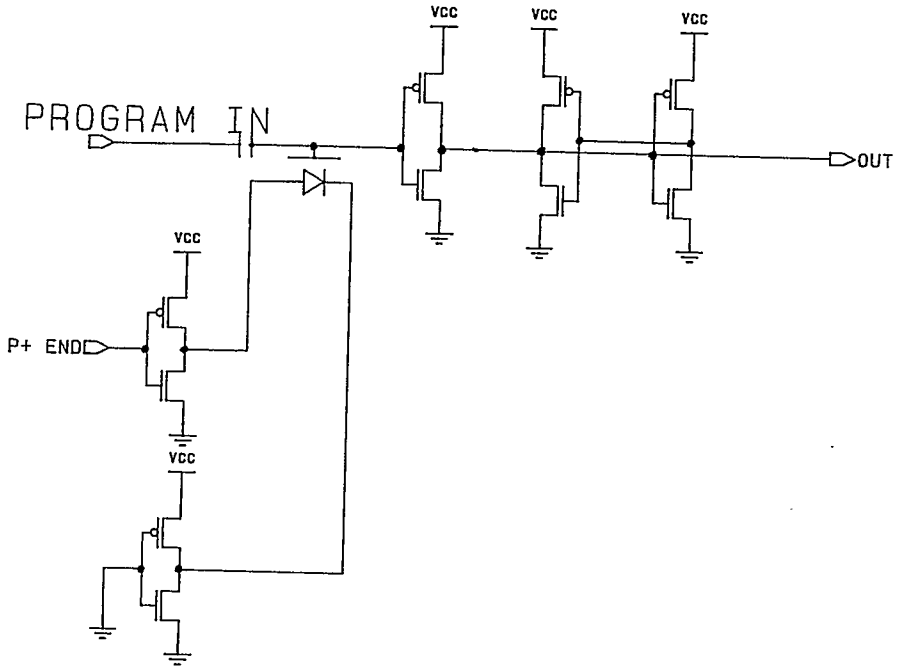


Fig (5-2-2) Circuit diagram of the new EEPROM.

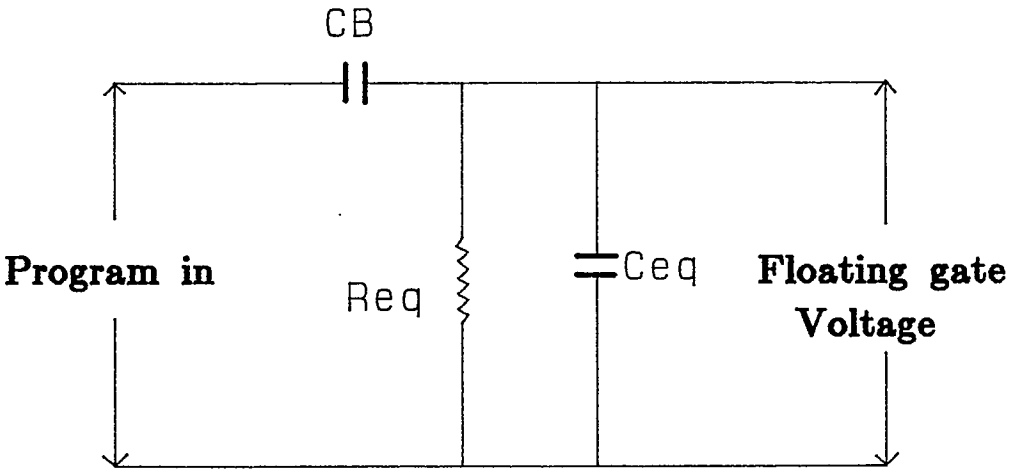


Fig (5-2-3) Equivalent circuit of the new EEPROM.

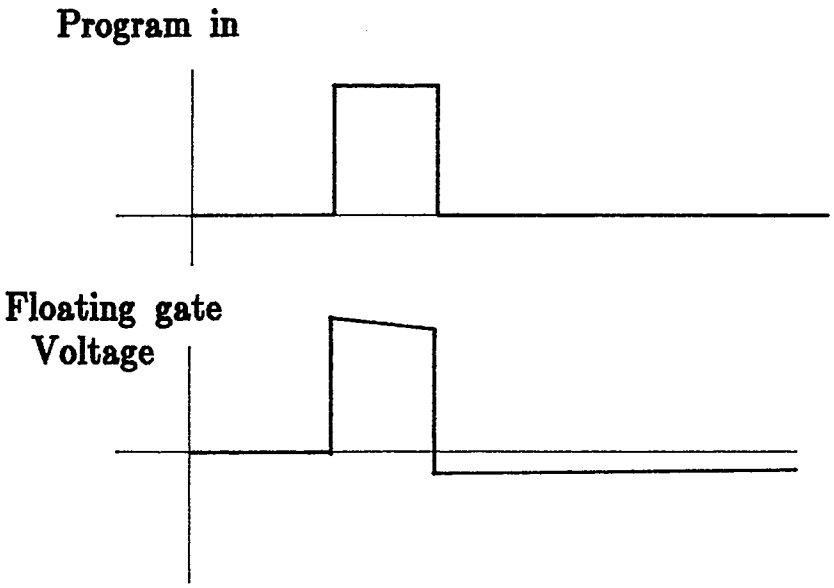


Fig (5-2-4) Programming I.

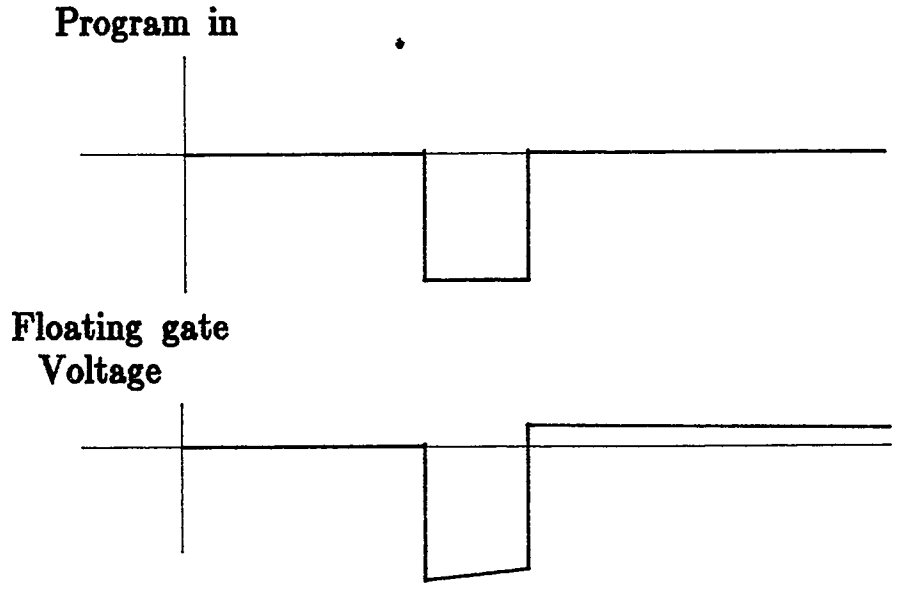


Fig (5-2-5) Programming II.

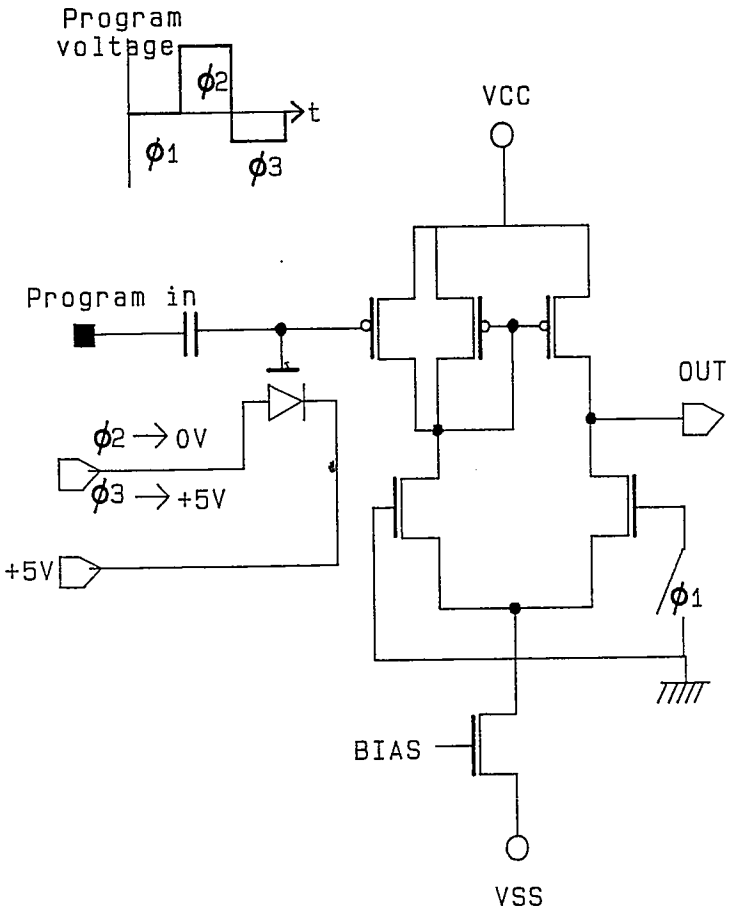


Fig (5-2-6) Application circuit for trimming offset voltage of an op amp.

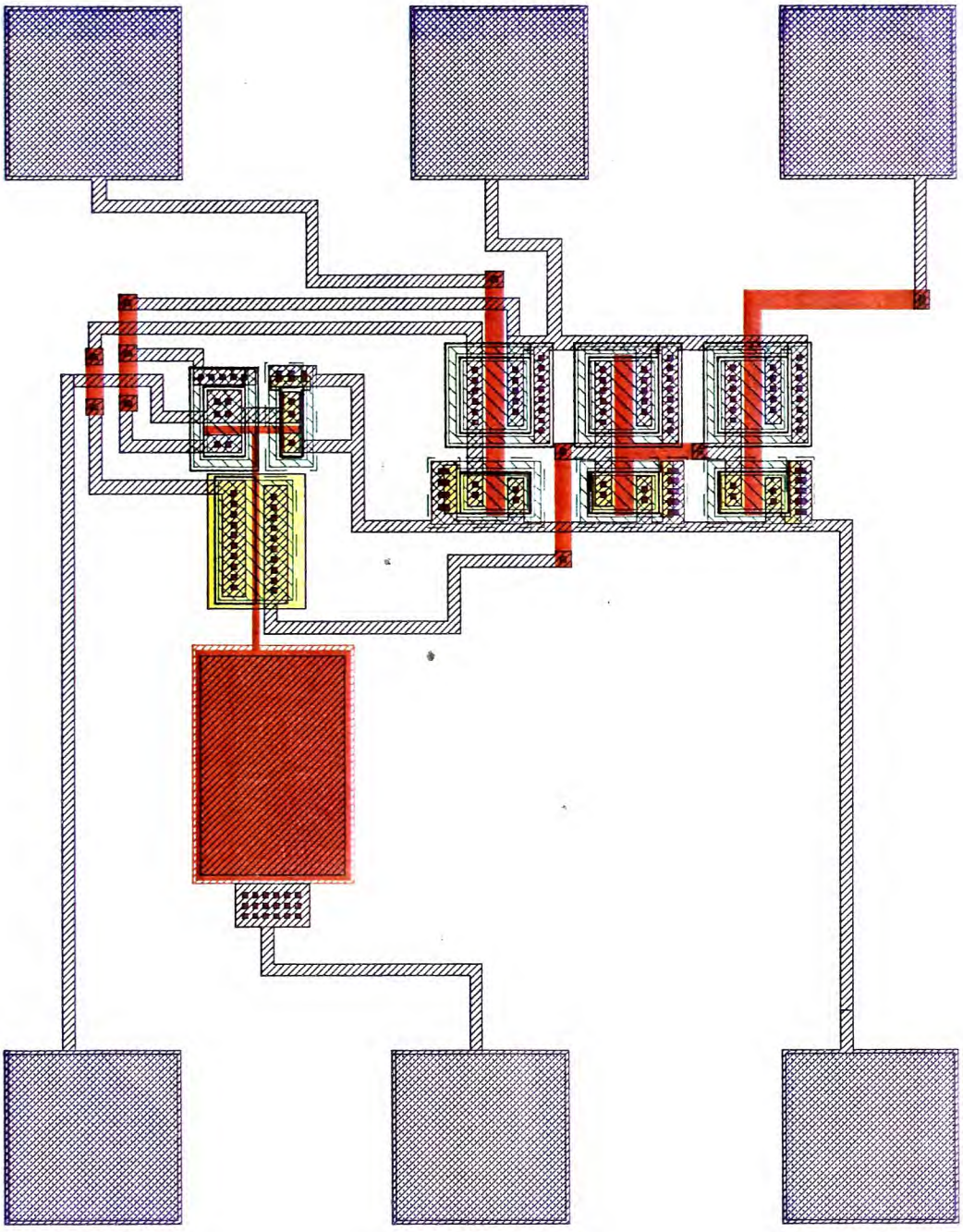


Fig (5-2-7) Layout of EEPROM.

the MOS op amp is the mismatches of the threshold voltage of the input stage transistors. By putting another transistor connected to the floating gate of the EEPROM, the offset voltage can be considerably reduced by the programming procedure. One experiment [5-5] shows that the offset voltage could be reduced to below 0.5mV from its initial value of 10mV. One of the advantages of this scheme is that it can be incorporated into a standard digital CMOS process without the additional processing steps typically needed for EEPROM fabrication. The layout of an EEPROM is shown in Fig (5-2-7).

5-3. Implementation of new EEPROM in Temperature sensor circuit

To control gain, offset and linearity, EEPROMs are placed in three different places of the temperature sensor circuit. The whole circuit diagram of the temperature sensor with EEPROMs is shown in Fig (5-3-1). EEPROM1 is for controlling the offset voltage of the temperature sensor to read 0 Volt at 0 degree. EEPROM2 is for controlling the gain of the output voltage; output voltage can be adjusted to the voltage level needed by the next stage. EEPROM 3 is for correcting the nonlinearity of the output voltage. Simulation data shows that if we program 0.5V on the EEPROM3 floating gate, a 100% linearity curve can be obtained. Fig (5-3-2) is the input file of the SPICE of temperature circuit with EEPROM3 and Fig (5-3-3) is the curve of the simulated output voltage vs. temperature. Fig (5-3-4) and Fig (5-3-5) show the effect of the EEPROM1(V_{FG}=5.0) and EEPROM2(V_{FG}=1.0), respectively.

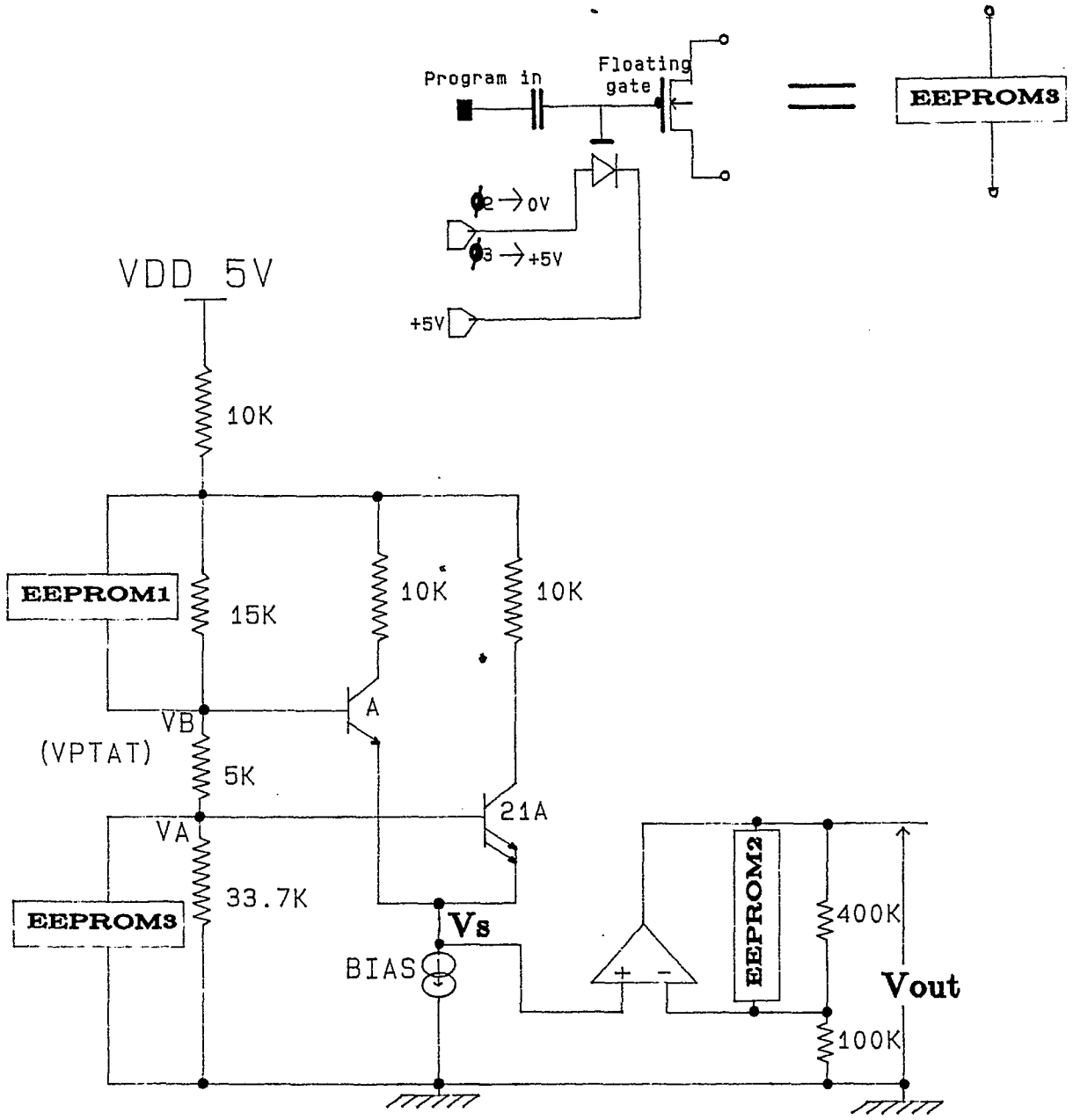


Fig (5-3-1) Circuit diagram of the temperature sensor with EEPROMs.

```
**TEMPERATURE SENSOR CIRCUIT WITH EEPROM**
VCC 1 0 5.0
**TRDESCRIPTION**
RJJ 1 11 10K
RKK 11 34 10K
RJ 11 13 10K
RK 11 12 10K
R1 34 35 5K
R2 35 36 5K
R3 36 0  33.7K
MK 36 88 0 0 N W=10U L=5U
V88 88 0 0.0
Q1 13 35 37 NP
Q2 12 36 37 NP 21
.OPTIONS ITL1=500 ITL5=0
.OPTIONS LIMPTS=500
**IBIAS CIRCUIT**
M31 133 132 1 1 P W=8U L=6U
M33 111 132 1 1 P W=8U L=6U
M134 132 132 1 1 P W=8U L=6U
M135 133 133 134 134 N W=4U L=36U
M136 132 133 135 135 N W=4U L=36U
D111 134 0 D1
D112 136 0 D1 10
R111 135 136 5K
M1 111 111 0 0 N W=4U L=36U
M2 37 111 0 0 N W=4U L=36U
.OPTIONS NOPAGE
.WIDTH OUT 80
.DC V88 0.0 0.5 0.05
.TEMP -50 0 50 100 150
.PRINT DC V(88) V(37)
**MODEL DEFINITION**
.MODEL D1 D IS=1.0E-14 VJ=0.8
.MODEL NP NPN IS=1.0E-14 BF=10
.MODEL N NMOS LEVEL=2.00000 RSH=20 TOX=520.000E-10
+ LD=0.280000U XJ=0.400000U CJ=4.5E-4 CJSW=6.0E-10
+ UO=200.000 VTO=0.587229 CGSO=5.2E-10 CGDO=5.2E-10
+ NSUB=4.575777E15 VMAX=10.E4 KP=3.848050E-05
+ MJ=0.5 MJSW=0.33 NFS=5.033532E11 GAMMA=0.922197
+ PHI=0.60000 UEXP=1.001000E-03 UCRIT=999000
+ DELTA=1.59123 LAMBDA=2.208002E-02 NEFF=1.001000E-02
+ NSS=0.000000E+00 TPG=1.00000 CGBO=8.0E-10 PB=0.700000
.MODEL P PMOS LEVEL=2.00000 RSH=55 TOX=520.000E-10
+ LD=0.280000U XJ=0.400000U CJ=3.6E-4 CJSW=6.0E-10
+ UO=100.000 VTO=-0.784085 CGSO=4E-10 CGDO=4E-10
+ NSUB=2.534947E14 VMAX=10.E4 KP=1.394594E-05
+ MJ=0.5 MJSW=0.33 NFS=8.870574E11 GAMMA=0.536443
+ PHI=0.600000 UEXP=0.171457 UCRIT=51857.9
+ DELTA=1.89818 LAMBDA=4.720123E-02 NEFF=1.001000E-02
+ NSS=0.000000E+00 TPG=-1.00000 CGBO=1.3E-09 PB=0.750000
.END
```

EEPROM3

Fig (5-3-2) SPICE input file of the temperature sensing circuit with EEPROM3(MK)

Temperature (°C)	V_{out} *without EEPROM3*	V_{out} *with EEPROM3*(V_{FG}=0.5V)
-50	1.450V	1.450V
0	1.980V Δ=530mV	1.980V Δ=530mV
50	2.510V Δ=530mV	2.510V Δ=530mV
100	3.040V Δ=530mV	3.040V Δ=530mV
150	3.670V Δ=630mV	3.570V Δ=530mV

Table (5-3-1) Simulated output voltage(V_{out}) with EEPROM3 vs. temperature(V_{FG} = 0.5V).

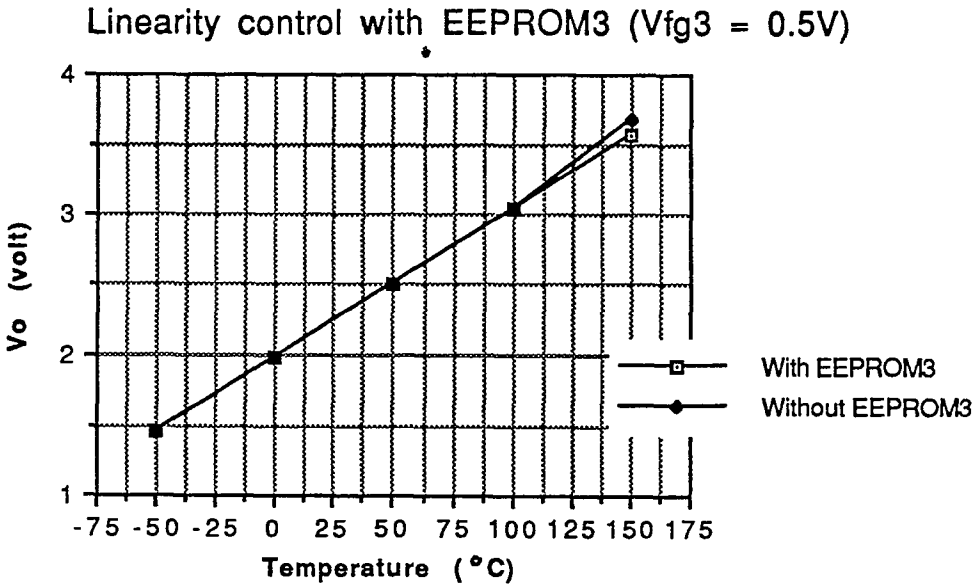


Fig (5-3-3) The simulated effect on output voltage(V_{out}) with EEPROM3 vs. temperature(V_{FG} = 0.5V).

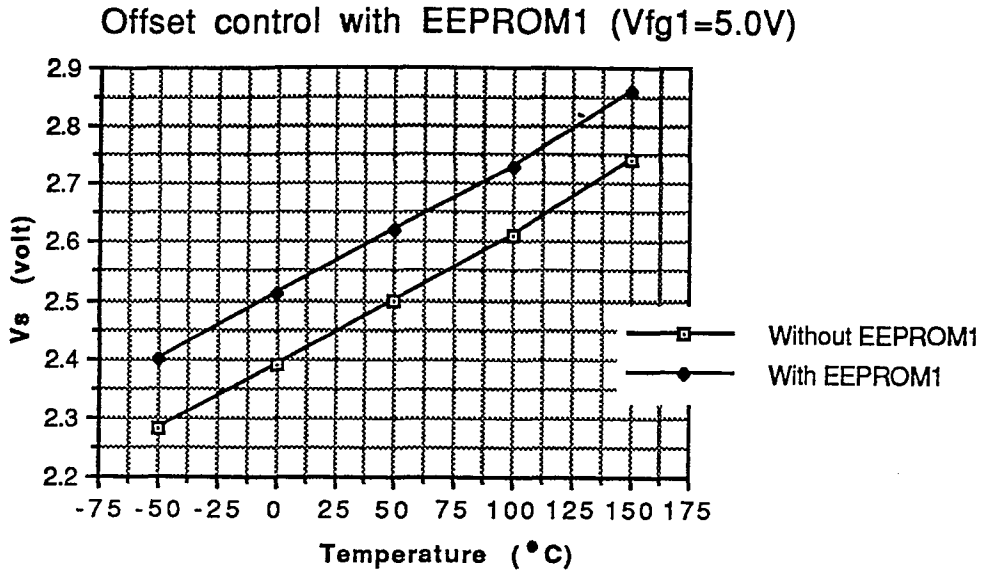


Fig (5-3-4) The simulated effect on V_S with EEPROM1

vs. temperature($V_{FG} = 5.0V$).

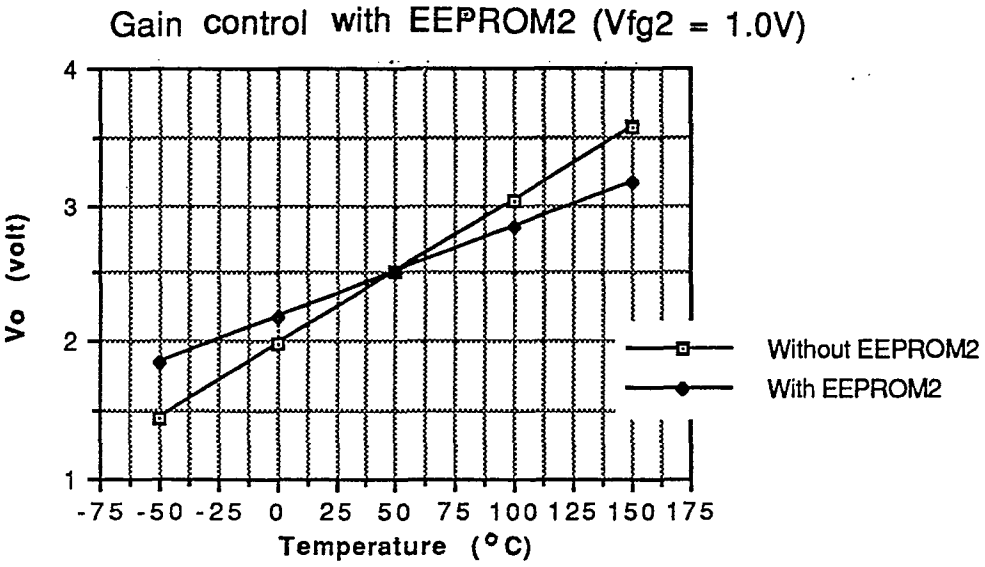


Fig (5-3-3) The simulated effect on (V_{out}) with EEPROM2

vs. temperature($V_{FG} = 1.0V$).

Chapter 6

Chip Design

This chapter covers the chip design of a CMOS temperature sensor. MOSIS scalable design rules are discussed.[6-1] The floor plan of chip design and the composite layout of the whole chip with 40 pins are illustrated. Finally, pin description and mesurement procedures are described.

6-1. Layout design rules

The design rules used in this temperature sensor IC design is based on the MOSIS 2μm P-well double poly and double metal CMOS design rule. Applying scalable design rule, $\lambda = 1.0$ μm. Details of the MOSIS scalable CMOS design rules are described as follows[6-1], and illustrated in Fig (6-1-1).

(1) P-well

1. minimum p-well width: 10λ
2. p-well to pwell spacing(different potential): 9λ
3. p-well to p-well spacing (same potential): 8λ

(2) active area

1. minimum active width: 3λ
2. P+ active area to P+ active area spacing: 3λ
3. N+ active area to N+ active area spacing: 3λ
4. P+ active area in N- region to P-well edge: 5λ
5. N+ active area in P- region to P-well edge: 3λ
6. N+ active area in P- well to P-well edge: 3λ
7. N+ active area to P+ active area spacing outside P-well: 3λ
8. N+ active area to P+ active area spacing inside P-well: 3λ

(3) poly I

1. minimum poly width: 2λ
2. poly to poly spacing: 2λ
3. field poly to active area spacing: 1λ
4. poly gate extension over field: 2λ
5. gate poly to active area spacing: 2λ

(4) P+ S/D select (N+ select)

1. P+ S/D overlap to active area: 2λ
2. P+ S/D overlap of poly in active area spacing: 2λ
3. P+ S/D to P+ S/D spacing: 1λ
4. P+ S/D to N+ active area spacing: 1λ
5. P+ S/D overlap of N+ S/D to achieve well contact: 1λ

(5) contact

1. contact size: $2\lambda \times 2\lambda$
2. contact to contact spacing: 2λ
3. poly overlap of contact: 1λ
4. contact to contact spacing between two different poly contacts: 5λ
5. poly contact to active area spacing: 2λ
6. contact to poly spacing: 2λ
7. active area overlap of contact: 1λ
8. active area to many poly contacts spacing: 3λ
9. poly to many active contacts spacing: 3λ
10. metal overlap of contact: 1λ

(6) metal 1

1. minimum metal 1 width: 3λ
2. minimum metal 1 spacing: 3λ

(7) via contact

1. via contact size: $2\lambda \times 2\lambda$
2. via to metal 1 contact spacing: 2λ(No Stacked via allowed)
3. metal 2 overlap of via: 1λ

(8) metal 2

1. minimum metal 2 width: 3λ
2. minimum metal 2 spacing: 4λ

(9) overglass

1. bonding pad size: $100\times100\ \mu m^2$
2. probe pad size: $75\times75\ \mu m^2$
3. metal 1 (unrelated) to pad spacing: 15μm
4. metal 2 (unrelated) to pad spacing: 30μm
5. via to pad edge spacing: 6μm

(10) guard ring for analog layout

1. minimum P+ guard bar width: 4 μm

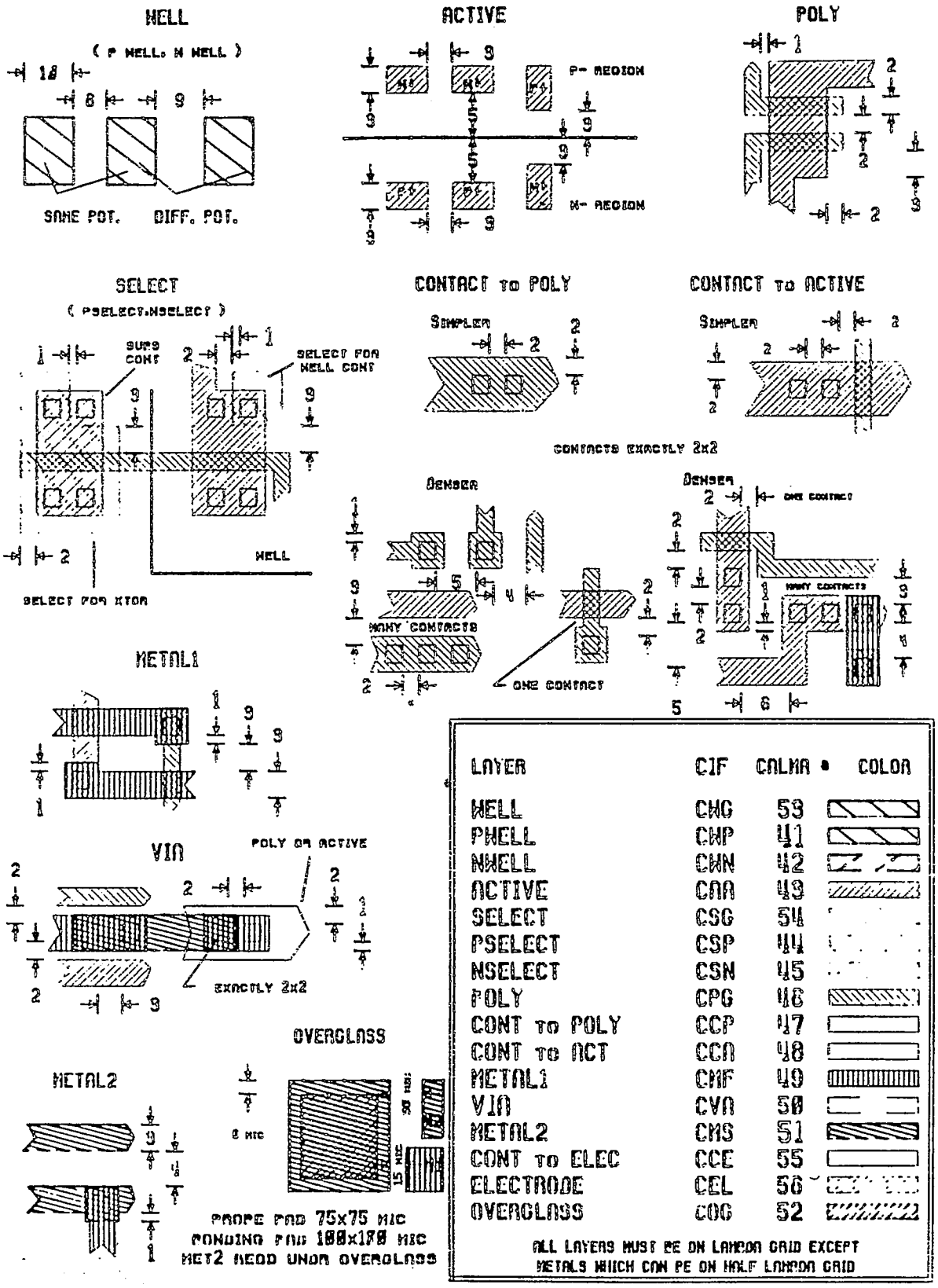


Fig (6-1-1) MOSIS scalable CMOS design rule.[6-1]

2. minimum N+ guard bar width: 4 μm

3. N+ guard guard bar outside P-well to P-well edge: 0μm

4. P+ guard bar to N+ outside P-well: 8μm

6-2. Floor plan of the chip

The floor plan of the temperature sensor is shown in Fig (6-2-1). The final chip size with 40 pins is 2200×2200 μm^2. The composite plot is shown in Fig (6-2-2).

6-3. Pin description and measurement procedure

As shown in Fig (6-2-1), this chip is comprised with six blocks: the temperature sensor with EEPROM correction circuit, the op amp test circuit, the MOS transistor test circuit, the bipolar junction transistor test circuit, the diode test circuit and EEPROM test circuit. All other blocks except the temperature sensor with EEPROM are designed to check the functioning of each unit of circuitry. Measurement procedures for each block are explained as follows.

6-3-1. Temperature sensor with EEPROM correction circuit

Pin # : 36, 37, 38, 17, 18, 19, 8, 9, 10 and 11 (Probe pins, if necessary: F+, L)

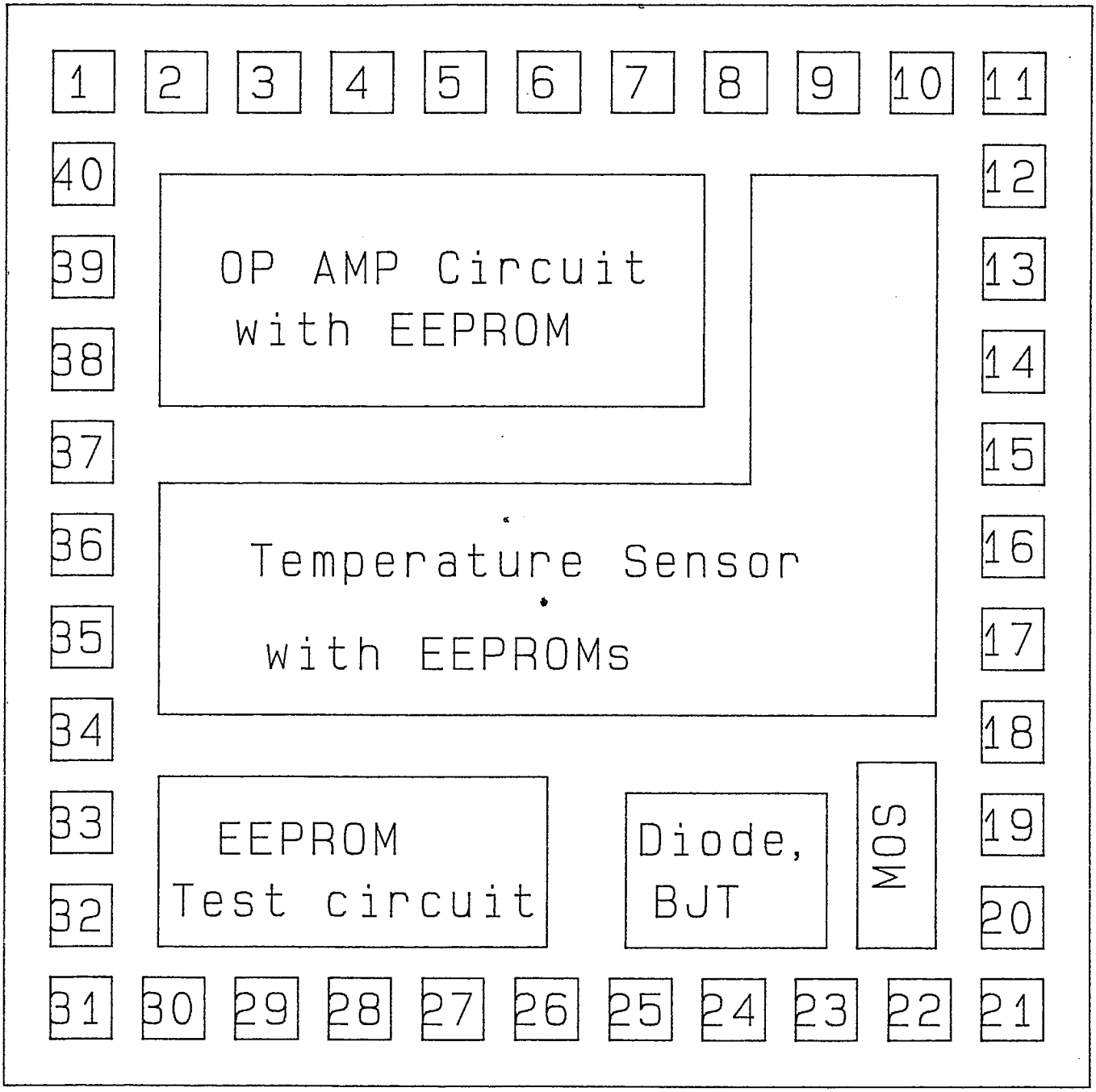


Fig (6-2-1) The floor plan of the chip including the DIP pin assignment.

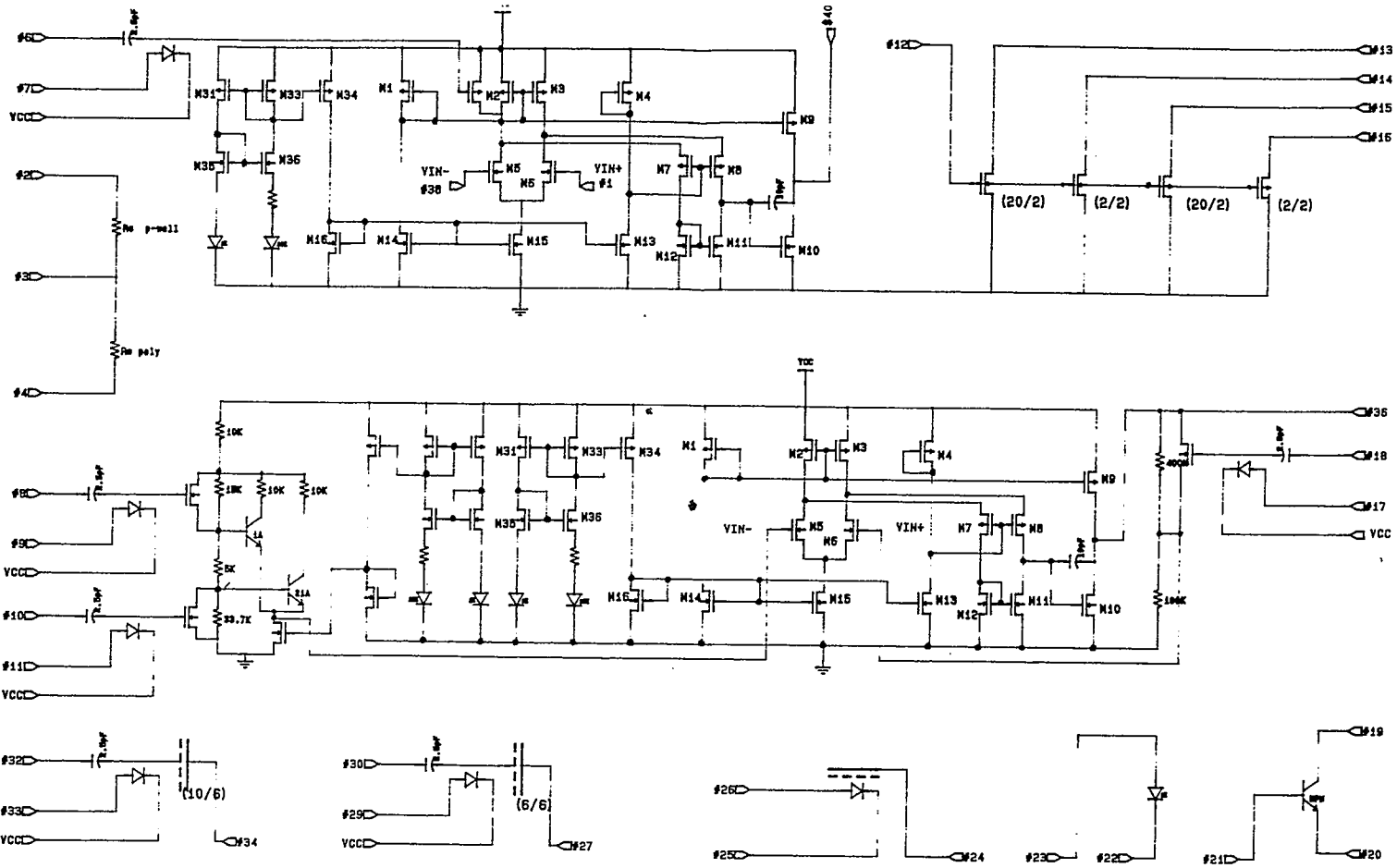


Fig (6-2-1A). Circuit schematic of the entire chip and pin assignment.

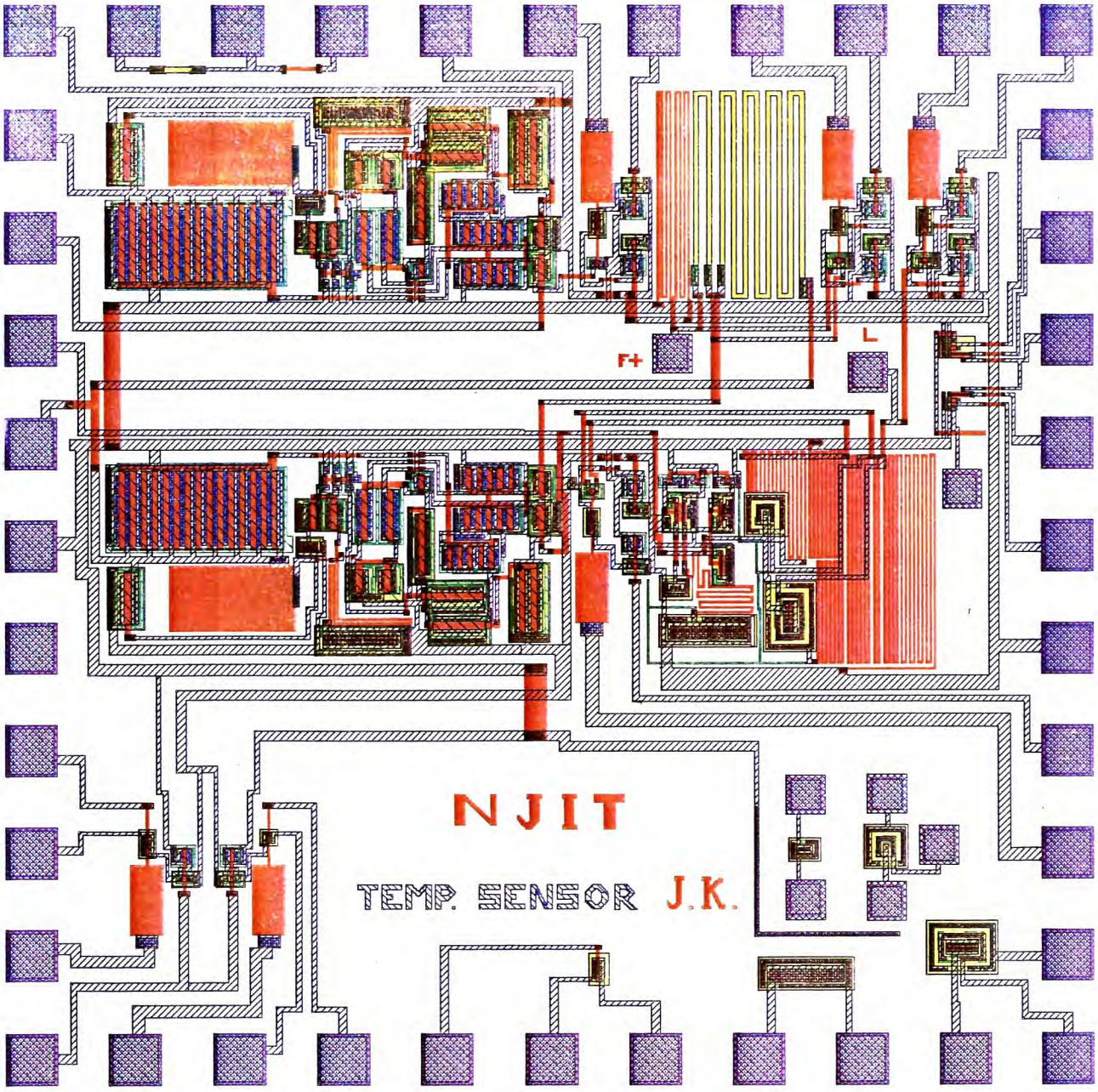


Fig (6-2-2) Composite plot of the chip.

VDD : #36

VSS : #17

Vout : #37

Temperature sensing output(before amplifying): #38

EEPROM control pins ;

EEPROM1 : # 7 and 8

EEPROM2 : # 9 and 10

EEPROM3 : # 18 and 19

Pin# 7, 9 and 18 are programming voltage pins, and 8, 10 and 19 are P+ voltage control pins.

6-3-2. Op amp test circuit

Pin # : 39, 40, 1, 5, 6, 7 and 36

VDD : #36

VSS : #5

OP amp out : #40

VIN+ : #39

VIN- : #1

EEPROM for offset voltage test: #6, 7.

Applying 0V to both VIN+ and VIN- pins, we can mesure the offset voltage of op

amp. By programming the EEPROM, we check how the offset voltage changes.

6-3-3. MOS transistor test circuit

Pin # : 12, 13, 14, 15, 16, 36, 17 and one probe pin, if necessary.

VDD : #36

VSS (common source) : #17

Commomn gate for transistor: #14

N-ch transistors(20/5, 20/2) drain : #12, 13

P-ch transistors(20/5, 20/2) drain : #15, 16

Check the operation of MOS transistor and characterize.

6-3-4. Bipolar junction transistor test circuit

Pin # : 20, 21, 22, 36, 17 and probe pins, if necessary.

VDD : #36

VSS : #17

Emitter, collector and base : #20, 21 and 22.

Check the operation of lateral bipolar junction transistor and characterize.

6-3-5. Diode test circuit

Pin # : 23, 24, 36, 17 and probe pins, if necessary.

VDD : #36

VSS : #17

P and N : #23 and #24

Check the operation of p-n diode and characterize.

6-3-6. EEPROM test circuit

Pin # : 25, 26, 27, 28, 29, 30, 31, 32, 33 and 34.

VDD : #36

VSS : #17

Electron tunneling charaterization : #25, 26 and 27.

EEPROM characterization : #28, 29, 30, 31, 32, 33, and 34.

6-3-7. Resistor test circuit

Pin # : 2, 3 and 4

P-well resistance (50/4) : # 2, 3

Poly resistance (50/4) : # 3, 4

In the temperature sensor circuitry, p-well and poly resistor are used. It is important

to check the real resistance value of these resistor for the evaluation of the chip.

Chapter 7

Experimental Results

A prototype of the circuit has been fabricated by MOSIS using a 2μm P-well double level poly and double level metal CMOS technology. Fig (7-1-1) shows the die photograph of the chip. Fig (7-1-2) shows the photomicrograph of the temperature sensing cell. The op amp circuit is shown in Fig (7-1-3) and the EEPROM error correction circuit is shown in Fig (7-1-4). The op amp of this prototype is not working so that we could not get the experimental results of the op amp characteristics. The measurement data (V_S) of the temperature sensing cell for four test chips are presented in Table (7-1-1). Fig (7-1-5) shows the comparison between the simulated data and the measured data of the V_S.

The characteristic of EEPROM has been measured as follows.

(1) we measured the output voltage of the temperature sensing cell(V_S) as the programming time applied to the EEPROM3 with -15V changes. This programming

is to increase the floating gate voltage of EEPROM3. In other words electrons are being removed from the floating gate. As shown Fig (7-1-6) the V_S starts to change from around 20min after applying -15V to EEPROM3. This explains that it takes about 20min to change the floating gate voltage to about the threshold voltage of the NMOS transistor(about 0.6V). From the equation $I_{inj} = C \times \Delta V / \Delta t$, where C is the total capacitance at the floating gate. With ΔV=0.6V and Δt=20min, we can calculate the injection current I_{inj}= 1fA if C is 2pF. The drawn capacitance value is about 2.5pF. There is trade-off between the resolution for programming the floating gate voltage and the total time for programming. If C_B is increased, the resolution will be finer , but a longer total time will be required for programming.

(2) Fig (7-1-7) shows the programming of the EEPROM1 to control the offset voltage. As shown in the figure it takes a little longer time to program the EEPROM1 because it needs 5V of the floating gate voltage.

(3) Finally, Fig (7-1-8) illustrates the characteristic of the EEPROM3 when we apply -15V and +15V for 30 min alternately.

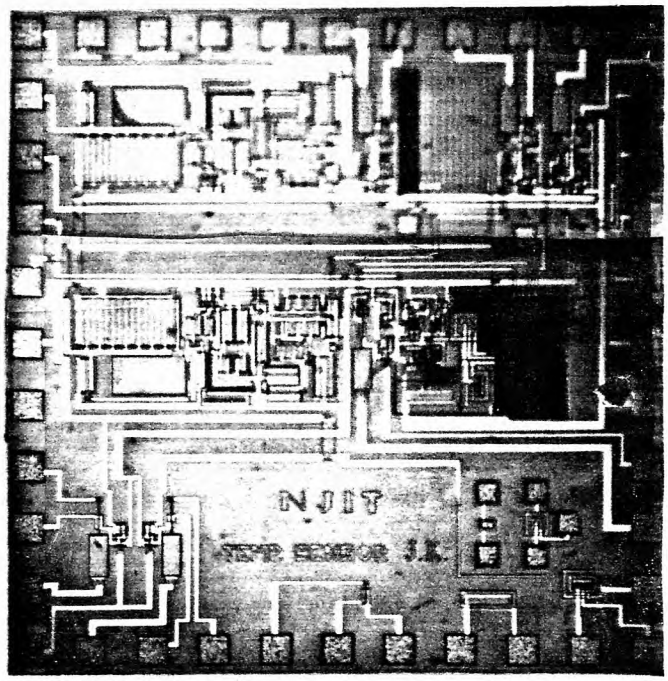


Fig (7-1-1) Die photo of the entire chip.

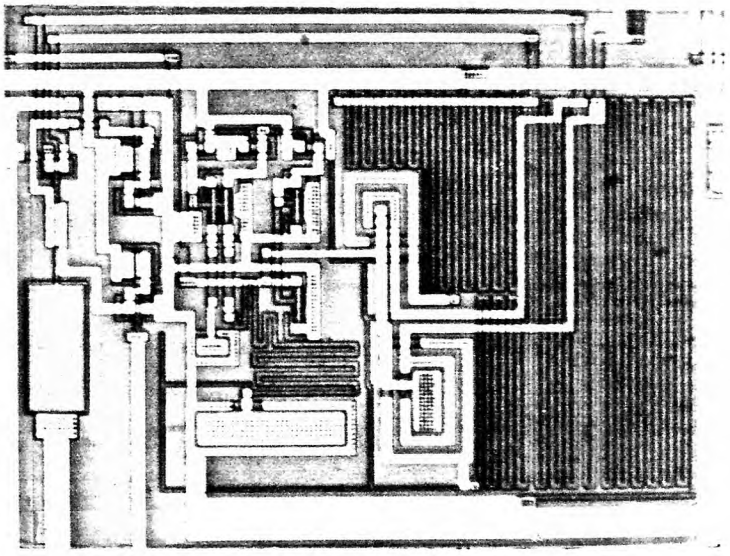


Fig (7-1-2) Photomicrograph of the temperature sensing cell.

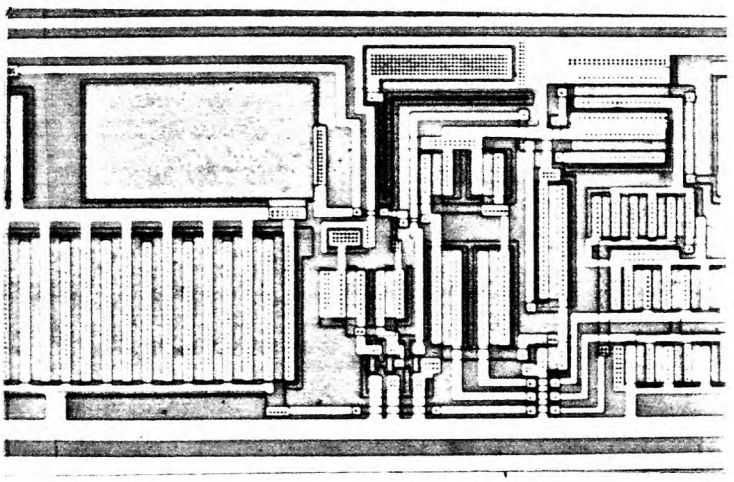


Fig (7-1-3) Photomicrograph of the op amp cell.

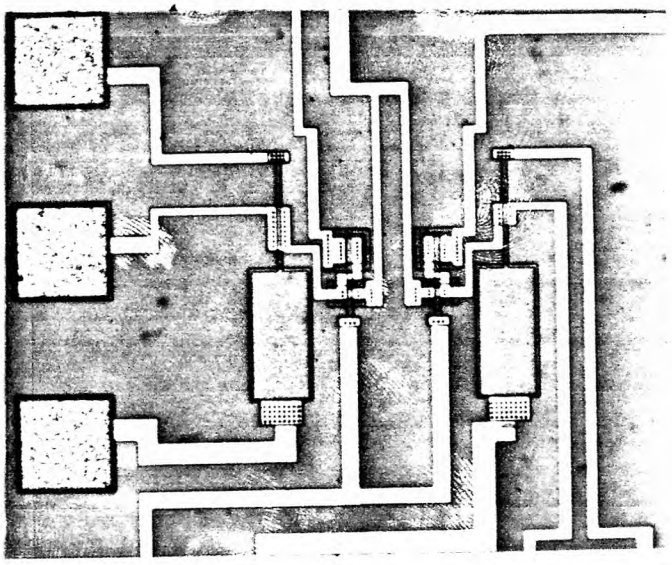


Fig (7-1-4) Photomicrograph of the EEPROM correction cell.

Temp.(°C)	*Chip#1(volt)*	*Chip#2*	*Chip#3*	*Chip#4*	*Average*	*Simulated data*
-50	2.220	2.210	2.220	2.240	2.223±0.019	2.280
-25	2.260	2.270	2.260	2.300	2.273±0.019	2.335
0	2.310	2.330	2.330	2.350	2.330±0.017	2.390
25	2.370	2.390	2.380	2.410	2.388±0.017	2.445
50	2.420	2.450	2.440	2.470	2.445±0.019	2.500
75	2.480	2.500	2.500	2.520	2.500±0.018	2.555
100	2.530	2.560	2.550	2.580	2.558±0.018	2.610

Table (7-1-1) Measured data of the temperature sensing cell

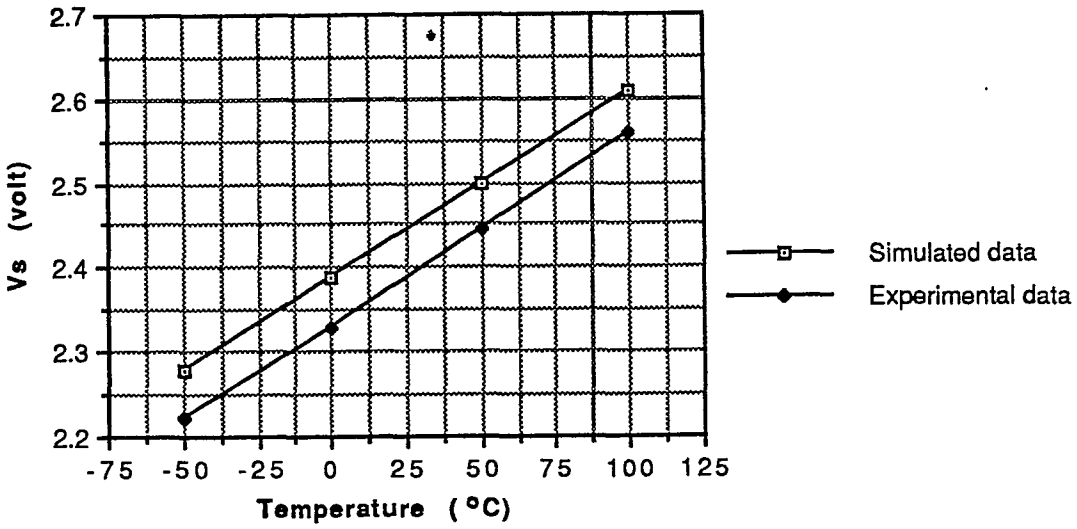


Fig (7-1-5) Comparison between the simulated data and the measured data of the temperature sensing cell.

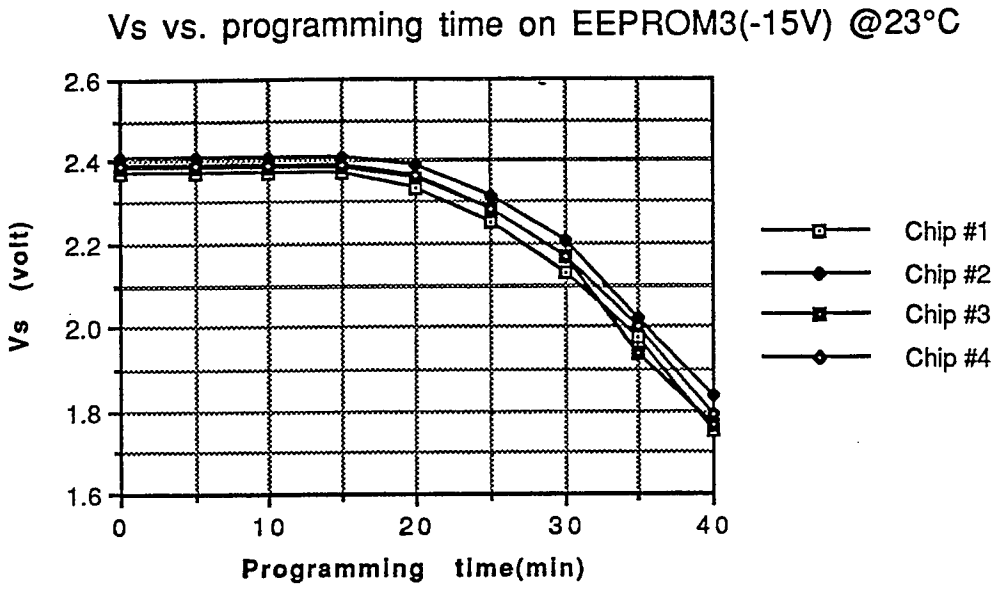


Fig (7-1-6) V_S vs. programming time on EEPROM3

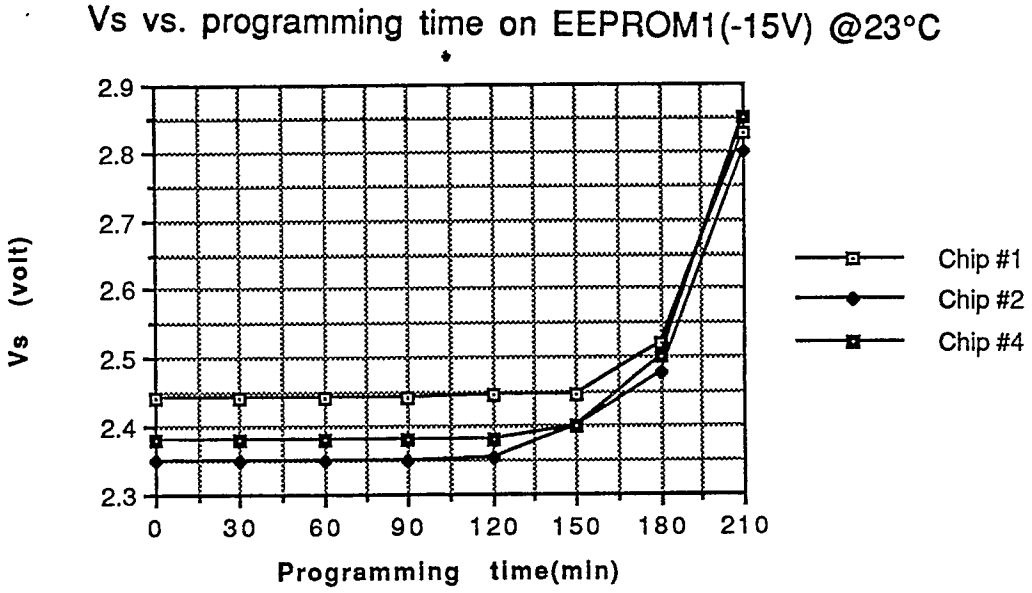


Fig (7-1-7) V_S vs. programming time on EEPROM1

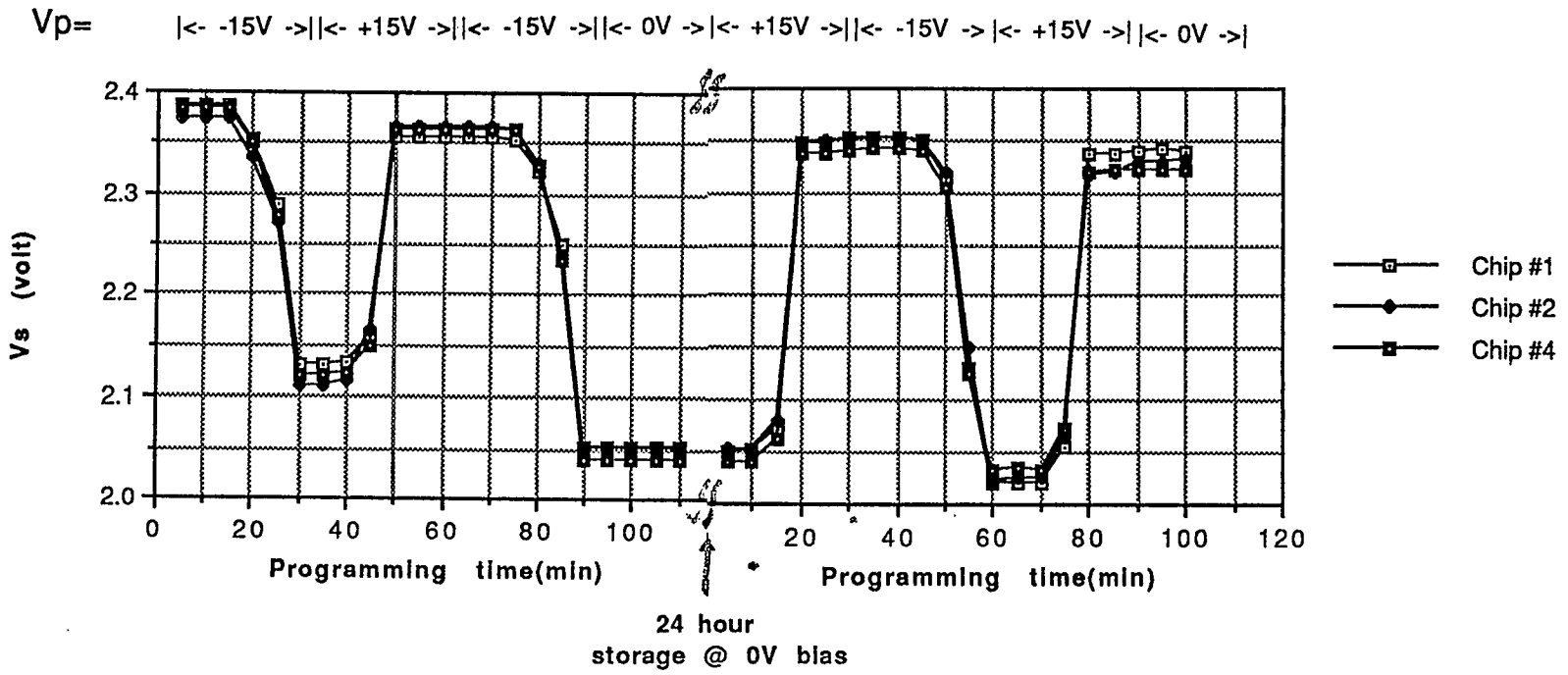


Fig (7-1-8) V_S vs. programming voltage polarity change on EEPROM3 in every 30 minutes.

Chapter 8

Summary and conclusion

We have designed a CMOS temperature sensor operating at low power with an EEPROM error correction scheme. The temperature sensing cell is designed with the V_{PTAT} method, consisting of two different emitter area bipolar junction transistors, resistors and a current source. Simulation data shows that the average voltage from the sensing cell is about 2.2mV/°C with nonlinearity over a 120°C range. A micropower CMOS cascode op amplifier is designed for amplification of the output voltage of the sensing cell. A non-inverting closed loop amplifier circuit increases the final output voltage 10.6mV/°C.

For correction of the nonlinearity and control of the offset voltage and gain, we introduced a new EEPROM structure error correction scheme. This structure uses hot electron injection from avalanche phenomenon to decrease the floating gate voltage and an electron tunneling mechanism to increase the floating gate voltage. The

new structure EEPROMs are used in three different places in the temperature sensor. With the error correction circuit, simulation data shows that very good linearity of voltage vs. temperature could be obtained.

The SPICE simulation results show that the total power consumption of the temperature sensor with 5V single power is 0.875mW to 1mW. This device is designed with some test circuits with 40 pins and size of 2200×2200 μm^2. Circuit layout has been done by MOSIS CMOS design rule and circuit simulation has been done by SPICE 2G.5 with MOSIS process parameters.

A prototype of the chip has been fabricated by MOSIS 2μm CMOS P-well double level poly and double level metal process. The sensitivity of the temperature sensing cell is 2.3mV/°C. The normal operation of the EEPROMs implemented on the chip was confirmed so that the offset and the nonlinearity of the temperature sensing cell and the gain of the op amp could be controlled by programming them.
The measured power dissipation is 0.776mW at 23°C. This device could be applied to the biomedical area or to optically powered sensor systems requiring low power consumption. The operation at a power supply of 2.5V is also confirmed by simulation.

APPENDIX

This section presents the MOSIS parametric test results and SPICE LEVEL 2 parameters of the chip. The typical I-V characteristic curves of the bipolar junction transistor, p-n diode, NMOS and PMOS transistor implemented in the prototype chip are also presented.

MOSIS PARAMETRIC TEST RESULTS

RUN: N05E / ESTHER
TECHNOLOGY: SCPE

VENDOR: ORBIT
FEATURE SIZE: 2.0um

I. INTRODUCTION. This report contains the lot average results obtained by MOSIS from measurements of the MOSIS test structures on the selected wafers of this fabrication lot. The SPICE LEVEL 2 and BSIM parameters obtained from similiar measurements on these wafers are also attached.

COMMENTS: This looks like a typical Orbit Semiconductor 2.0um run.

II. TRANSISTOR PARAMETERS:	W/L	N-CHANNEL	P-CHANNEL	UNITS
Vth (Vds=.05V)	3/2	1.079	-.843	V
Vth (Vds=.05V)	18/2	.989	-.821	V
Idss (Vgds=5V)	18/2	2502.0	-1285.0	uA
Vpt (Id=1.0uA)	18/2	16.12	-15.25	V
Vth (Vds=.05V)	50/50	.970	-.838	V
Vbkd (Ij=1.0uA)	50/50	16.2	-16.2	V
Kp (Uo*Cox/2)	50/50	23.1	11.07	uA/V^2
Gamma (2.5v,5.0v)	50/50	1.110	.457	V^0.5
Delta Length		.621	.344	um
Delta Width (Effective=Drawn-Delta)		.227	.093	um

COMMENTS: These parameters seem normal.

III. FIELD OXIDE TRANSISTOR PARAMETERS:	GATE	SOURCE/DRAIN N + ACTIVE	SOURCE/DRAIN P + ACTIVE	UNITS
Vth (Vbs=0,I=1uA)	Poly	17.2	-13.1	V
Vth (Vbs=0,I=1uA)	Metal1	17.3	-23.3	V
Vth (Vbs=0,I=1uA)	Metal2	17.2	-25.7	V

COMMENTS: These parameters seem normal.

IV. PROCESS PARAMETERS:	N POLY	P POLY	N DIFF	P DIFF	METAL 1	METAL 2	POLY 2	UNITS
Sheet Resistance	21.7	22.6	22.1	74.5	.050	.025	19.3	Ohm/sq
Width Variation (Measured - Drawn)	-.278	-.257	.400	.296	-.191	.338	-.273	um
Contact Resist. (Metal1 to Layer)	9.02	10.46	17.42	33.85	----	.030	8.68	Ohms
Gate Oxide Thickness:	----	----	399.	----	----	----	----	Angst.

COMMENTS: These parameters seem normal.

V. CAPACITANCE PARAMETERS:	POLY	N DIFF	P DIFF	METAL 1	METAL 2	POLY 2	UNITS
Area Cap (Layer to subs)	.068	.422	.209	.032	.021	----	fF/um^2
Area Cap (Layer to Poly)	----	----	----	.045	.022	.463	fF/um^2
Area Cap (Layer to Metall)	----	----	----	----	.038	.045	fF/um^2
Fringe Cap (Layer to subs)	----	.520	.279	----	----	----	fF/um

COMMENTS: These parameters seem normal.

VI. CIRCUIT PARAMETERS:

Vinv,	K = 1	2.19	V
Vinv,	K = 1.5	2.39	V
Vlow,	K = 2.0	0.00	V
Vhigh,	K = 2.0	4.99	V
Vinv,	K = 2.0	2.53	V
Gain,	K = 2.0	-10.78	
Ring Oscillator Frequency		31.51	MHz (31 stages @ 5.0V)

COMMENTS: The ring oscillator frequency is typical.

N05E SPICE LEVEL 2 PARAMETERS

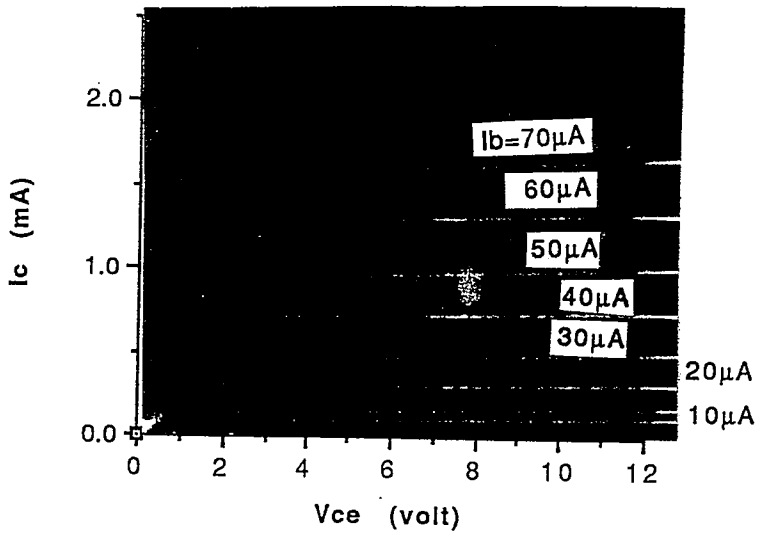
```
.MODEL CMOSN NMOS LEVEL=2 LD=0.218757U TOX=412.000000E-10
+ NSUB=2.240587E+16 VTO=0.988057 KP=4.984000E-05 GAMMA=1.029
+ PHI=0.6 UO=594.7 UEXP=0.243024 UCRIT=142404
+ DELTA=3.23333 VMAX=81664.1 XJ=0.250000U LAMBDA=2.779413E-02
+ NFS=2.635596E+12 NEFF=1 NSS=1.000000E+10 TPG=1.000000
+ RSH=22.200000 CGDO=2.750240E-10 CGSO=2.750240E-10 CGBO=5.921737E-10
+ CJ=4.125000E-04 MJ=0.473800 CJSW=5.311000E-10 MJSW=0.377600 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.26 um
.MODEL CMOSP PMOS LEVEL=2 LD=0.250000U TOX=412.000000E-10
+ NSUB=5.042106E+15 VTO=-0.883034 KP=2.053000E-05 GAMMA=0.4881
+ PHI=0.6 UO=244.945 UEXP=0.162903 UCRIT=7707.01
+ DELTA=1.36921 VMAX=37257.1 XJ=0.250000U LAMBDA=5.622673E-02
+ NFS=7.164748E+11 NEFF=1.001 NSS=1.000000E+10 TPG=-1.000000
+ RSH=74.500000 CGDO=3.143031E-10 CGSO=3.143031E-10 CGBO=6.262755E-10
+ CJ=2.205000E-04 MJ=0.442200 CJSW=2.594000E-10 MJSW=0.268500 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -0.12 um
```

```
N05E  SPICE BSIM PARAMETERS

NM1 PM1 DU1 DU2 ML1 ML2
*
*PROCESS=orbit
*RUN=n05e
*WAFER=11
*Gate-oxide thickness= 412.0 angstroms
*Geometries (W-drawn/L-drawn, units are um/um) of transistors measured were:
* 3.0/2.0, 6.0/2.0, 18.0/2.0, 18.0/5.0, 18.0/25.0
*Bias range to perform the extraction (Vdd)=5 volts
*DATE=06-22-90
*
*NMOS PARAMETERS
*
-8.10747E-01, 1.43723E-02, 3.86842E-02
 7.60841E-01, 0.00000E+00,-1.88687E-23
 1.10838E+00, 8.29834E-02, 4.43931E-01
-6.01460E-03, 8.73214E-02, 4.01414E-02
-5.30635E-03, 1.03794E-02, 1.32459E-02
 5.66398E+02,8.02317E-001,-2.62722E-001
 5.12103E-02, 4.39206E-02,-2.39412E-02
-1.80067E-03, 5.86226E-01,-1.25492E-01
 1.43066E+01,-2.96373E+01, 5.77484E+01
-3.08282E-04,-5.07086E-03,-7.30013E-03
 2.57615E-04,-1.28067E-03,-2.80901E-03
 1.90184E-03,-1.34887E-02, 3.38737E-02
-3.12657E-03, 7.19306E-03, 2.77314E-02
 5.52136E+02, 3.52142E+02, 1.61677E+02
 4.21291E+00,-2.65411E+01, 1.26348E+02
-1.82458E+00, 6.96110E+01,-2.18820E+01
 2.83784E-03, 6.67848E-02,-2.25437E-02
4.12000E-002, 2.70000E+01, 5.00000E+00
5.04342E-010,5.04342E-010,5.92531E-010
1.00000E+000,0.00000E+000,0.00000E+000
1.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
* Gate Oxide Thickness is 412 Angstroms
*
*
*PMOS PARAMETERS
*
-4.67062E-02,-2.42658E-01, 2.18770E-01
 6.53221E-01, 0.00000E+00,-4.68211E-24
 3.28495E-01, 2.55371E-01,-1.43256E-01
-4.55177E-02, 1.11710E-01,-7.07840E-02
-3.86229E-03, 4.62126E-02, 1.30494E-02
 2.27845E+02,5.88225E-001,-2.66152E-001
 1.23220E-01, 3.06948E-02,-8.04019E-02
 7.23161E-03, 2.65037E-01, 5.37089E-02
 9.78627E+00,-5.27661E+00, 6.39495E+00
 1.29008E-03,-6.41329E-03,-3.53751E-04
 3.00274E-04,-3.27344E-03,-1.60923E-03
 6.48694E-03,-3.84013E-03, 2.77905E-03
-2.12138E-03, 7.29997E-03, 1.59959E-02
 2.17716E+02, 1.32708E+02, 6.82681E+01
 6.36827E+00, 4.45088E+00, 1.47555E+01
-1.80963E+00, 1.36984E+01, 3.32685E+00
-1.87957E-02, 3.63753E-03, 1.19021E-02
4.12000E-002, 2.70000E+01, 5.00000E+00
3.69762E-010,3.69762E-010,5.91702E-010
1.00000E+000,0.00000E+000,0.00000E+000
```

```
1.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
0.00000E+000,0.00000E+000,0.00000E+000
*
*N+ diffusion::
*
22.2,    4.125000e-04,    5.311000e-10,    0,    0.8
0.8,    0.4738,    0.3776,    0,    0
*
*P+ diffusion::
*
74.5,    2.205000e-04,    2.594000e-10,    0,    0.7
0.7,    0.4422,    0.2685,    0,    0
*
*METAL LAYER -- 1
*
5.050000e-02,    0,    0,    0,    0
0,    0,    0,    0,    0
*
*METAL LAYER -- 2
*
2.570000e-02,    0,    0,    0,    0
0,    0,    0,    0,    0
```

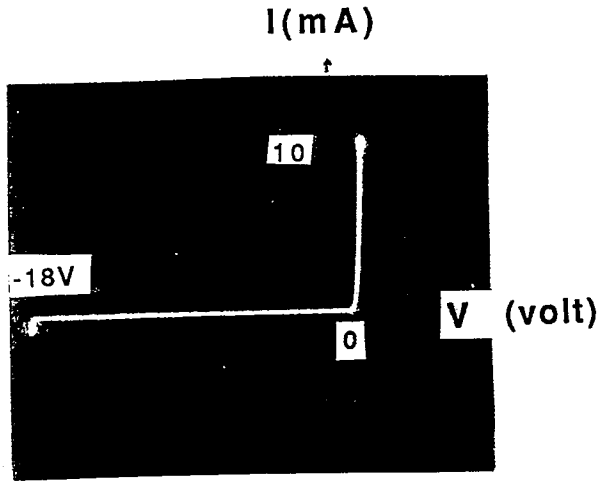
BJT I-V curve



Bipolar Junction Transistor

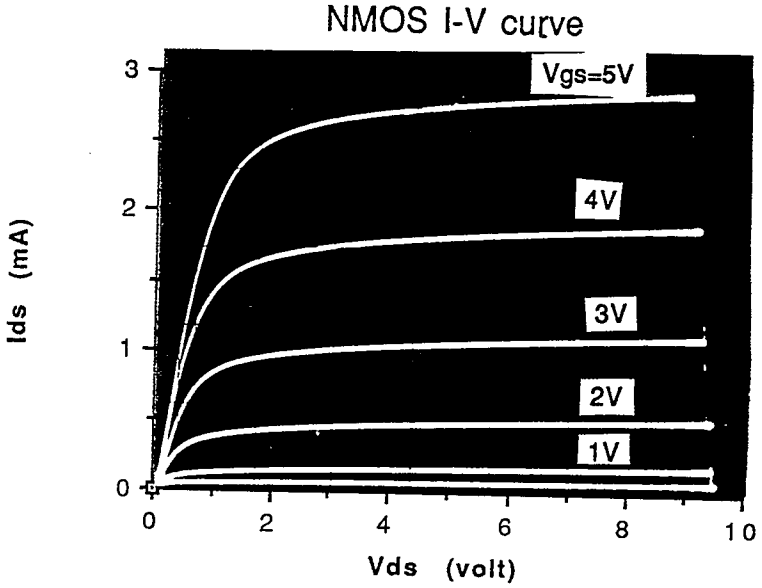
Pin number: Base;#21, Collector;#20, Emitter;#22

Diode I-V Curve



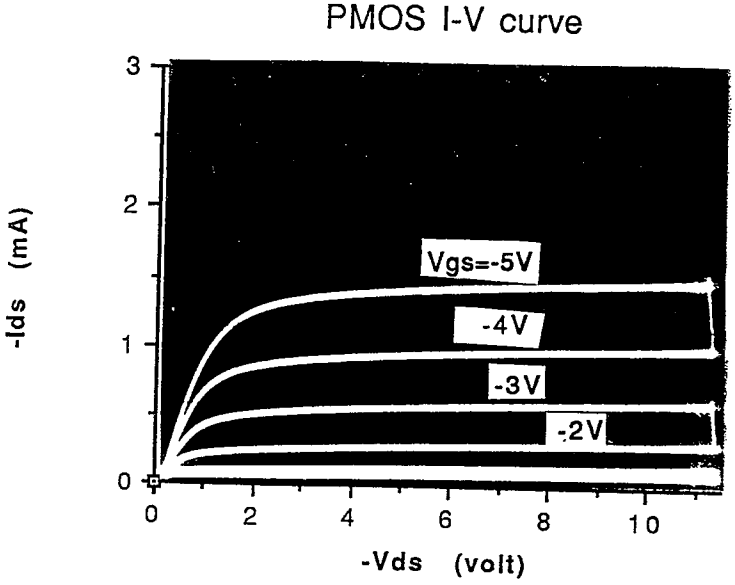
Diode

Pin number: P+;#24, N;#23



NMOS Transistor(20/2)

Pin number: Source;#17, Gate;#14, Drain;#12,13



PMOS Transistor(20/2)

Pin number: Source;#17, Gate;#14, Drain;#15,16

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