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Design of a temperature sensor for gallium arsenide ic applications

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2) DESIGN OF A TEMPERATURE SENSOR FOR GALLIUM ARSENIDE IC APPLICATIONS

by

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ABSTRACT

DESIGN OF A TEMPERATURE SENSOR FOR

GALLIUM ARSENIDE IC APPLICATIONS. (December 1988)

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Thesis Advisor: Dr. William N. Carr

This thesis presents the design of a temperature sensor circuit including sensor, differential amplifier, and a memory element for gallium arsenide IC standard cell applications. A standard 1-um depletion-mode GaAs MESFET technology has been used for the design of the circuit. The circuit is intended to be used as a standard cell in GaAs ICs providing an alarm when the sensor temperature reaches 125 °C. The circuit includes a NAND latch which is set when the chip cell temperature reaches 125 °C. The output of the latch can be sensed by additional circuits (on or off the GaAs chip) which initiate systems-level cooling or shut down. For sensing the temperature, a GaAs diffused diode pair is employed in which diode areas are ratioed (8 to 1). This enables the diodes to provide a differential voltage which is proportional to absolute temperature. The circuit simulation was done using SPICE3B.1 software installed on VAX station II/GPX hardware in Ultrix V2.0 environment. The Valid Logic Systems CAE software has been used for the schematic capture and GaAs physical layout. The photolithography mask set utilizes 8 layers - active area(N-), source & drain(N+), ohmic contact, Schottky gate metal, metal 1, metal 2, intermetal via and passivation. The total area of the sensor cell is 195x195 square microns. The worst case error demonstrated by the sensor circuit due to the cumulative effect of ±5% variations in the MESFET threshold voltage, diode junction potential, power supply voltage, resistor layout mismatch and ±10% variation in the MESFET transconductance was found to be 7.7 °C.

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DEFINITION OF SYMBOLS

V_T	MESFET threshold voltage
b	Doping tail extending parameter
β	MESFET transconductance parameter
α	Saturation voltage parameter
λ	Channel length modulation parameter
ϵ	Dielectric permittivity
μ	Electron mobility
ϕ_{Bn}	Diode junction potential
N_d	Channel doping density
N_c	Density of states in the conduction band
V_{bi}	Gate junction potential
C_{gso}	Zero-bias gate-source junction capacitance
C_{gdo}	Zero-bias gate-drain junction capacitance
v_s	Electron saturation velocity
A	Channel thickness
W_g	Gate width
L	Gate length
A^*	1.2 x Richardson constant.

CHAPTER I

INTRODUCTION

This thesis presents the design, simulation and physical layout of a temperature sensor circuit for Gallium Arsenide IC applications. The circuit design includes diode sensors, a differential amplifier and an output latch, and is based on 1-um gate length depletion mode GaAs MESFET technology. When a GaAs IC chip gets too hot, there is a rapid degradation in the device performance and eventual catastrophic failure. The design of this thesis permits an external circuit to initiate cooling or shut down procedures if the chip gets too hot. The sensor circuit sets a latch when the temperature reaches 125 °C. A GaAs diffused diode pair has been used to sense the temperature in which, diode areas are ratioed (8 to 1). This enables the diodes to provide a differential voltage which is proportional to absolute temperature. The following discussion gives a brief outline of the chapters of the thesis that follow.

Chapter two, is a discussion of GaAs MESFET. The discussion begins with a historic perspective of the device. Then, the two kinds of MESFET logic viz., enhancement and depletion modes are studied. Commonly used logic circuit approaches employed for GaAs MESFET ICs are summarized. The chapter ends with a discussion of the relative advantages and disadvantages of the different logic circuit approaches for MESFET ICs.

Chaper three begins with a summary of process methodology including the basic masking steps for a GaAs digital IC process. Three state of the art MESFET technologies-(1) SAINT (Self Aligned Implantation N+ Technology) (2) Stable Gate Self-alignment MESFET technology and (3) the conventional planar structure process, are detailed. At the end of the chapter,

the fabrication sequence of a self-aligned gate planar structure process selected for design in the thesis is described with figures illustrating the process flow.

Chapter four begins with the p-n junction theory, followed by a discussion of the I-V curves of a forward-biased GaAs diffused diode. Three references are included here showing GaAs diffused and Schottky diode forward I-V curves. Two models for MESFET device simulation are described along with some quantitative study. The MESFET model is used by the SPICE 3B.1 package for simulating a GaAs MESFET.

Chapter five details the design, simulation and the physical layout of the temperature sensor circuit. It begins with the discussion of basic principle used in the sensor design, followed by the SPICE simulation results of the differential amplifier and the latch. The circuit schematics are captured using the VALID Graphics Editor (GED). The sensitivity of the GaAs circuit to errors in MESFET transconductance (β), mismatch in diode junction potentials (ϕ_{Bn}), mismatch in resistor layout mismatch (R_m), to power supply voltage (V_{dd}), and MESFET threshold voltages (V_T) are briefly discussed. The design procedure for the diode, MESFET, and resistor dimensions is described. The chapter ends with discussion of the physical layout obtained using the VALID Layout Editor (LED). The total area of the GaAs sensor circuit is 195x195 square microns.

The thesis ends with an Appendix which includes the layout mask key, design rules for cell layout, minimum digitized feature sizes for the different layers and the electrical parameter specifications. The Appendix also describes briefly the VALID CAE software used for the schematic capture and physical layout of the temperature sensor circuit.

CHAPTER II

GALLIUM ARSENIDE MESFET

A. Development of the MESFET

The MEtal-Semiconductor Field-Effect Transistor was first proposed by C.A. Mead in 1966. The operation of a MESFET is similar to that of a Junction Field-Effect Transistor, JFET. The MESFET, however, has a metal-semiconductor junction instead of a diffused p-n junction for a gate electrode. Practical MESFETs are fabricated by using epitaxial layers on semi-insulating substrates to minimize parasitic capacitances. A perspective view of a MESFET is shown in fig 2.1 [S.M. Sze, 1985], where 'z' is the channel width, 'L' the channel length and 'a' the channel depth. These devices were first used as discrete devices for microwave applications in the late sixties. These applications were mainly aimed at microwave amplification for both low noise and moderately high power.

For two reasons, most MESFETs are made of n-type III-V compound semiconductors: their high electron mobilities help to minimize series resistances, and their high saturation velocities result in increased cut-off frequencies. Among the various III-V compounds, GaAs turned out to be an excellent candidate for high-performance digital applications because of its wide energy band gap, high electron mobility and saturation velocity, and the availability of a semi-insulating (SI) GaAs substrate.

Semi-insulating GaAs substrates allow one to decrease the parasitic capacitances and simplify the fabrication process. Also SI GaAs substrates offer a natural electrical isolation between active devices. Moreover, they remain

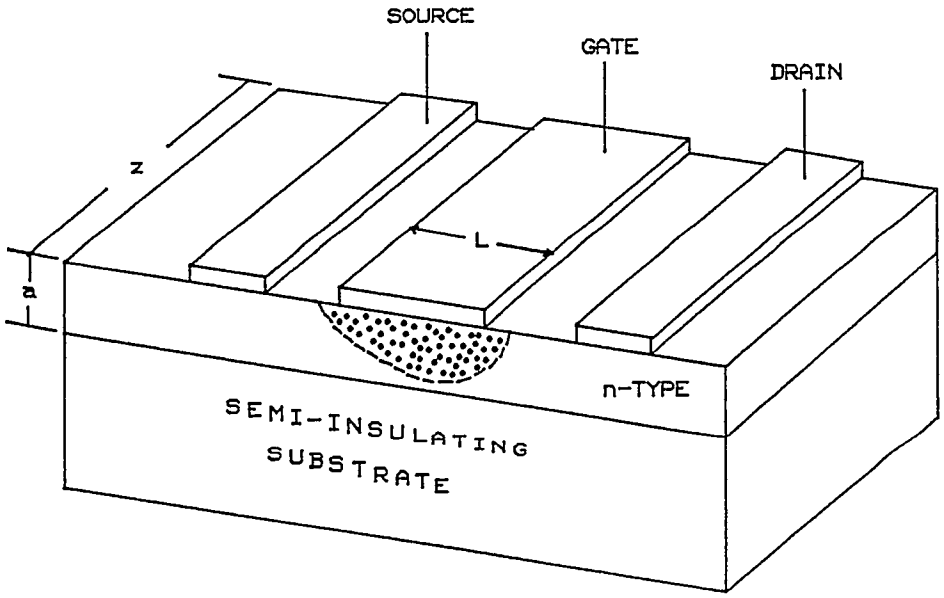

FIG 2.1 PERSPECTIVE VIEW OF A MESFET

semi-insulating, even after being bombarded with fast neutrons or gamma rays, which is of prime importance for military applications. The high electron mobility (six times higher in n-type GaAs than in n-type silicon) and poor hole mobility (about 15 times lower), along with the easy fabrication of Schottky barriers on n-type GaAs, have led to the selection of n-channel MESFETs as the most appropriate active devices for the first generation of GaAs digital ICs.

B. GaAs MESFET Logic

The ideal logic element in a logic circuit is a switch with infinitely fast response time, infinite resistance when it is open and zero resistance when it is closed. It should consume infinitesimally small power, be very small in size and be capable of being made with absolute reproducibility in vast numbers on a suitable integration medium. No semiconductor device can meet these requirements. While the GaAs MESFET is better than the conventional silicon devices in many respects, it is worse in others.

The GaAs MESFET can be used as a switch in two different modes of operation. First, in the depletion mode or normally-on operation, the channel is open with zero bias on the gate. In this state, the device has a relatively low drain-source on resistance, and maximum saturation current flows through the device. To "switch" the device off, a negative voltage is applied to the Schottky barrier gate, thereby expanding the depletion layer to the point where it meets the semi-insulating substrate. In this state, the device has a relatively high drain-source resistance and hence a very small current flows through the device. The gate voltage required to turn the device current "off", the pinch-off voltage, is a function of the thickness and the channel doping which, for most

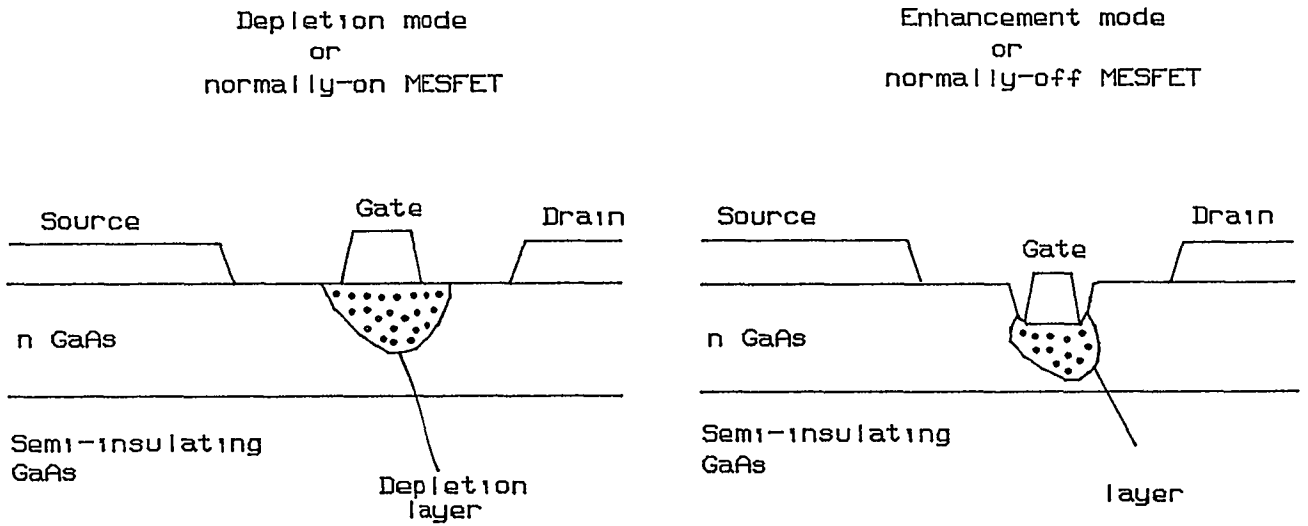

Fig 2.2 Basic MESFET cross sections

logic applications using Depletion mode FETs (DFETs), is between -0.5 and -2.5v.

The second mode of operation is called enhancement mode or normally-off operation. It can be seen that if the product of the initial channel thickness and doping level (the NxD product) is reduced, the channel will be pinched off by the built-in potential of the Schottky barrier gate, and the pinch-off voltage will be positive. To open the channel, in order to allow the current to flow between the drain and the source, a positive voltage must be applied to the gate. Maximum channel opening is therefore determined by the maximum forward voltage that can be applied to a Schottky barrier gate, usually approximately 0.8V. The enhancement mode FET (EFET) has therefore a smaller maximum on current than the depletion mode FET, and so takes less power for the same gate geometry. Fig 2.2 [Joseph Mun, 1986] shows the basic DFET and EFET cross sections.

C. Circuit Approaches for GaAs ICs

There are different kinds of circuit approaches for designing GaAs MESFET logic. The most widely used approaches are described below:

Direct Coupled FET Logic (DCFL) : DCFL circuits employ enhancement mode FETs for drive and depletion mode FETs or resistors for pull-up loads. This approach has the smallest number of circuit components per gate among all the GaAs IC circuit approaches. Fig 2.3a [Howes, 1985] shows a DCFL NOR gate using a resistor as the load. Fig 2.3b [Shur, 1987] shows a DCFL NOR gate that employs a depletion FET as the load. The disadvantages of DCFL approach are high propagation delay and high noise margin.

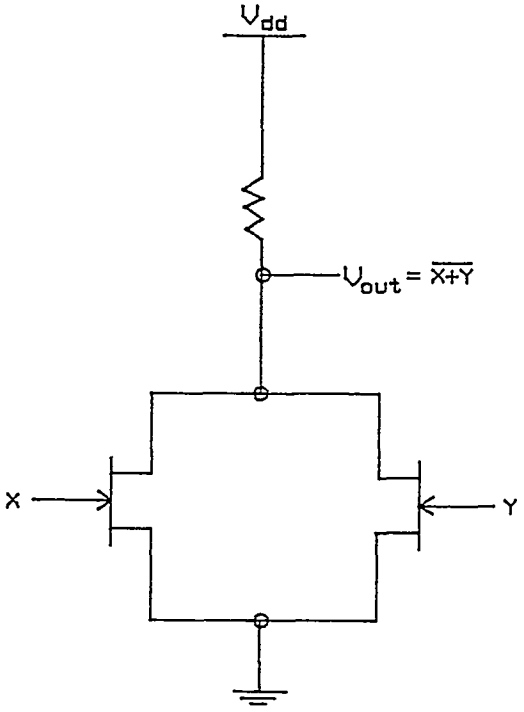

Fig 2.3a
DCFL NOR gate
with
resistor as load

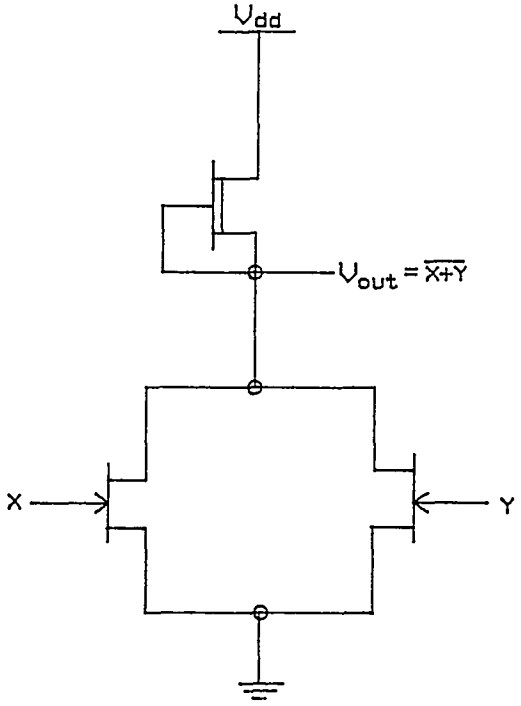

Fig 2.3b
DCFL NOR gate
with
depletion FET as load

Low Pinch-off Voltage FET Logic (LPFL) : LPFL circuits use three enhancement mode MESFETs and a Schottky diode as a switch in a two-stage design. Because of larger pinch-off voltages (compared to the DCFL), LPFL circuits are more tolerant to the variations in the threshold voltages than DCFL circuits. Fig 2.4 [Nuzillat, 1980] shows a NOR gate circuit configured in the LPFL.

Source Coupled FET Logic (SCFL) : SCFL circuits employ differential amplifiers and buffer stages with diode level shifters similar to bipolar ECL circuits. The transfer characteristics of SCFL OR/NOR gate circuits are nearly independent of the threshold voltage of the switching FETs since the critical level of the transfer characteristics is the externally applied reference voltage, Vref. This allows for wider variation of pinch-off voltage Vp. Fig 2.5 [Shur, 1987] shows an SCFL OR/NOR gate.

Buffered FET Logic (BFL) : BFL circuits employ Depletion FETs and Schottky diodes for level shifting in order to make the input and voltage levels of the logic gates compatible. The required number of diodes is determined by the pinch-off voltage of the switching transistor and in turn determines the magnitude of the logic swing. Circuits utilizing MESFETs with smaller pinch-off voltages have fewer level-shift diodes and exhibit smaller power consumption, smaller logic swing, and smaller noise margins. An example of BFL NOR gate is shown in fig 2.6 [Abdel-Motaleb, 1987].

Capacitive Coupled Logic (CCFL or CCL) : CCFL circuits employ depletion mode FETs and a reverse-biased diode that serves as a capacitor. The basic CCFL structure is similar to the BFL structure. An advantage is that the CCFL circuits use a diode capacitor to eliminate the requirement of level

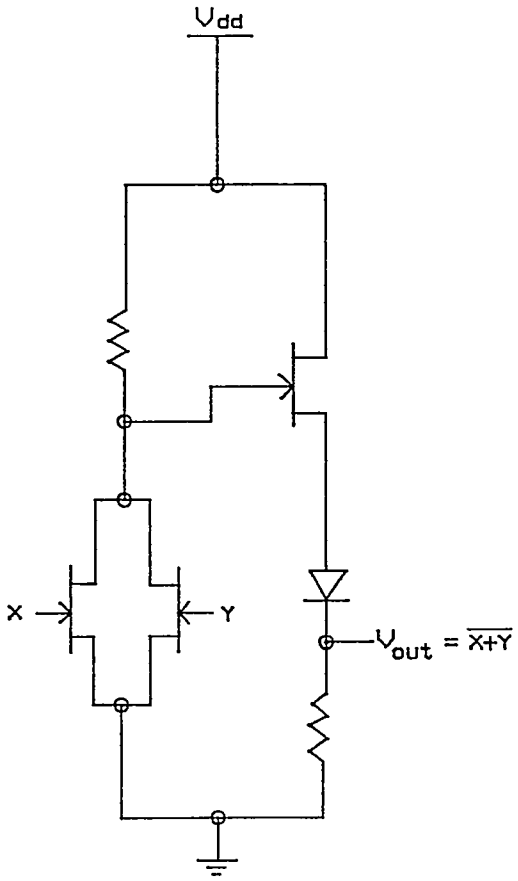

Fig 2.4

LFPL NOR gate

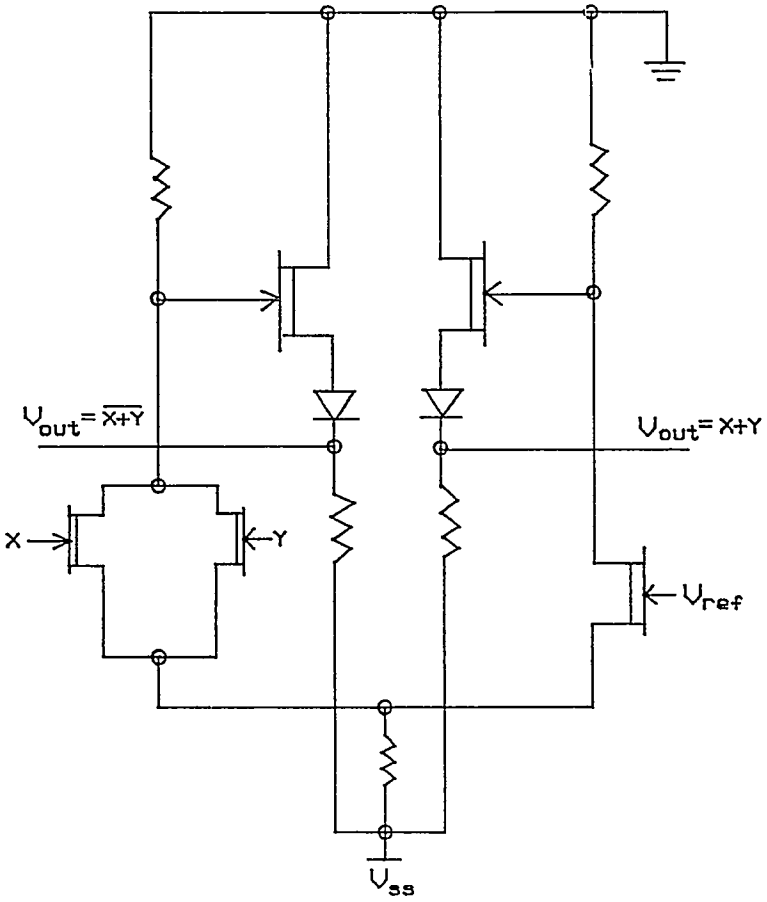

Fig 2.5

SCFL NOR/OR gate

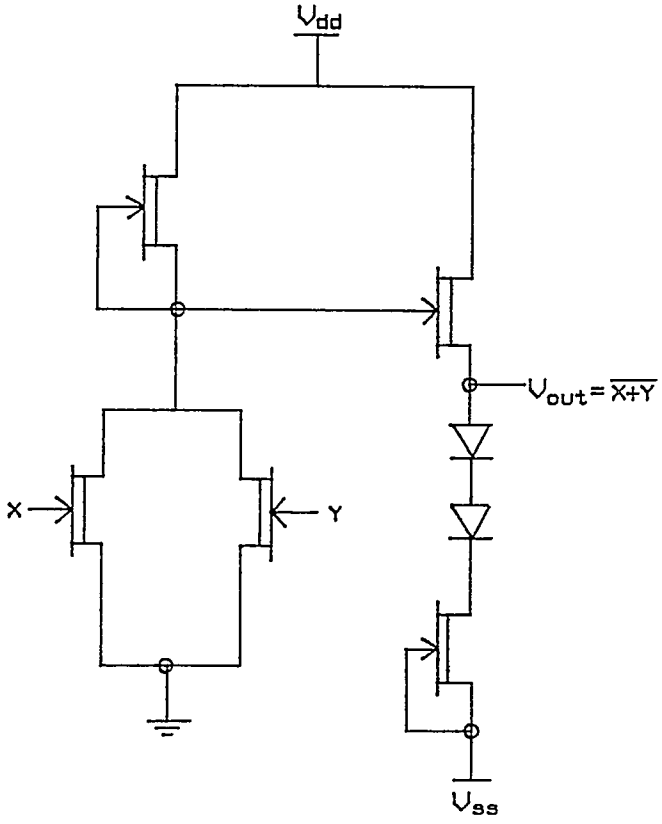

Fig 2.6
BFL NOR gate

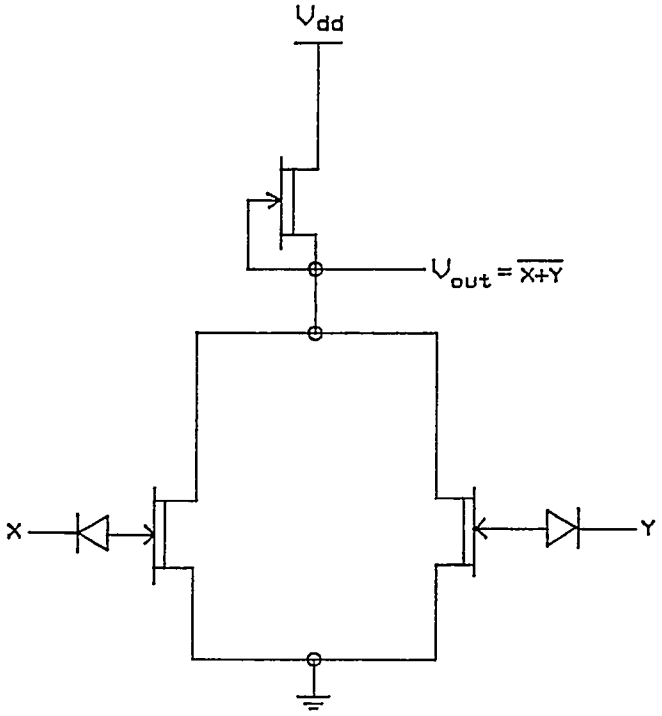

Fig 2.7
CCFL NOR gate

shifting components that are needed in the BFL circuits. A BFL NOR gate is shown in the fig 2.7 [Welbourn, 1982]. The illustrated diode is used as a capacitor to provide a dc isolation that results in a lower CCFL power dissipation as compared to that of the BFL approach. However, this kind of circuit will not function in a static logic situation and is not convenient for many applications.

Capacitor Diode FET Logic (CDFL) : CDFL circuits offer some improvements over the CCFL circuits, employing some additional components to let the capacitance of the reverse-biased diode charge by a very small current flowing through the chain of several small Schottky diodes. Therefore, CDFL circuits may work as static logic gates. A CDFL NOR gate is shown in fig 2.8 [Warlick, 1987].

Schottky Diode FET Logic (SDFL) : SDFL circuits employ depletion mode FETs and Schottky diodes. The normally-on switching transistors used in the SDFL circuits leads to a larger voltage swing and noise margins and, as a consequence, leads to a higher yield and better reliability at the penalty of higher power consumption. Also, a larger number of transistors and diodes per gate may lead to a somewhat smaller speed compared to DCFL circuits. A NOR gate circuit configured in SDFL is shown in fig 2.9 [Einspruch,1985].

A summary of the relative advantages and disadvantages of the above mentioned circuit approaches follows. The DCFL approach has the lowest power dissipation (of the order of few hundred microwatts per gate) because it eliminates level shifting circuits and has a very low logic swing. The elimination of level shifting circuits also helped to simplify significantly the circuit layout and, consequently, further to increase the packing density. This approach has

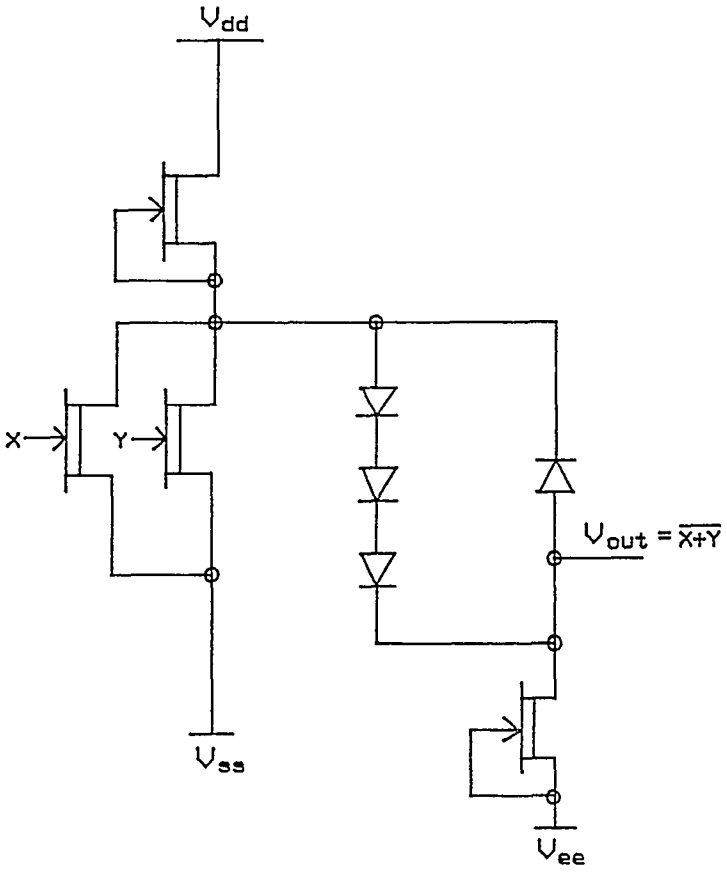

Fig 2.8
CDFL NOR gate

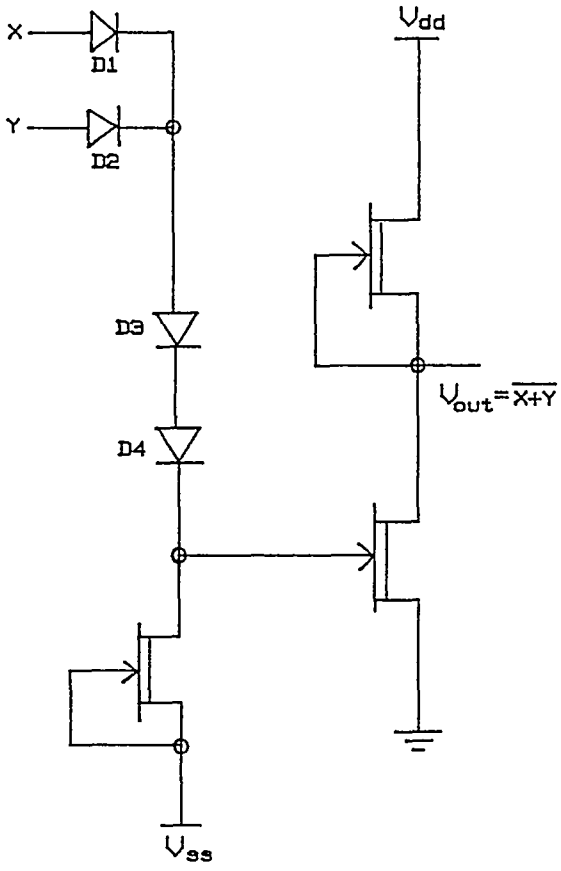

Fig 2.9
SDFL NOR gate

been used to obtain circuit complexities up to VLSI levels. There are two major weaknesses to this approach: the high propagation delay and difficulty in fabrication. The second weakness is caused by the stringent requirement on the active-layer doping and thickness that are necessary in order to maintain uniformity in pinch-off voltage. Also, multiple ion implants are required when the enhancement mode driver is employed.

The LPFL approach is faster, and has better fabricability, but dissipates more power than the DCFL approach. The BFL approach is fastest, but dissipates most power thereby limiting the achievable circuit complexity to MSI level. Another disadvantage of this approach is the, requirement of two power supplies. The SCFL circuits, which allow more Vp variation than all other circuit approaches, have a dc level compatible with the bipolar ECL circuits. The drive capability is better than the SDFL and DCFL circuit approaches. The disadvantages of the SCFL approach are its high power dissipation and poor circuit density. CCFL circuits have lower power dissipation than BFL circuits because they use the diode to provide a dc isolation. However this approach doesn't work where only dc is applied. This is very inconvenient for many applications; therefore CCFL is rarely used. The CDFL circuit, an improvement over the CCFL circuit, is faster and has better drive capability and lower power dissipation. Thus, this approach is suitable for SSI and MSI levels. However, the CDFL circuit needs more chip area than does the commonly used BFL circuit, so the the achievable circuit complexity is limited to the LSI level.

Finally, the SDFL approach is suitable for achieving both speed and lower power dissipation. Though this approach does not have the fastest speed and lowest power dissipation, it is acceptable for most applications. Circuits

employing the SDFL approach are relatively easier to fabricate. Table 2.1 shows the comparison of the above discussed MESFET logic types.

LOGIC TYPE	POWER DISSIPATION PER GATE [mW]	DELAY TIME PER GATE [PS]	PACKING DENSITY [gates/mm^2]	LOGIC SWING [Volts]	NOISE MARGIN
BFL	1-2	75	100-500	0.6	LARGE
SDFL	2-10	100	100-200	0.8-1	MEDIUM
DCFL	0.2-0.5	200	500-1000	0.5	SMALL
SCFL	2-10	50-80	10-100	0.4-0.8	MEDIUM
CDFL	2-10	100	100-200	0.8-1	MEDIUM

Table 2.1 Comparison of GaAs MESFET Logic types

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CHAPTER III

GALLIUM ARSENIDE DIGITAL IC FABRICATION

A. Basic Masking Steps

The starting point of any process is the GaAs substrate, as shown in the flow chart in the fig 3.1 [Joseph Mun, 1986]. Sample substrates, i.e. wafers after being brought in from specialist substrate manufacturers, go through a rigorous assessment procedure. Their quality is checked for, among other things, diameter and thickness tolerances, flatness, edge roundness, surface finish. The assessed electrical properties include resistivity, activation and mobility. As a result of these qualification tests, a batch of substrates are either passed or rejected for the actual IC fabrication. The first step of fabrication is the formation of an active layer of n-type material. For digital circuits based on, for example, 1v pinch-off DFETs, this layer is approximately 100 nm thick, with a carrier concentration of approximately 10^{17}/ cc. In the last few years, practically all manufacturers are using ion implantation to produce this layer. Ion implantation has the advantage of very high throughput, good uniformity across the wafers and excellent reproducibility from wafer to wafer. Before ion implantation technology matured, the active layer was usually grown by vapor or liquid phase epitaxy. The epitaxial layer technology served the very useful purpose of helping to demonstrate the advantages of GaAs digital ICs during the early stages of their development, but it is rather a difficult technology to implement for production. Si is widely used as the implantation species to form the donor atom in the active layer. The implantation layer is electrically inactive as the Si atoms are randomly located in GaAs crystal lattice.

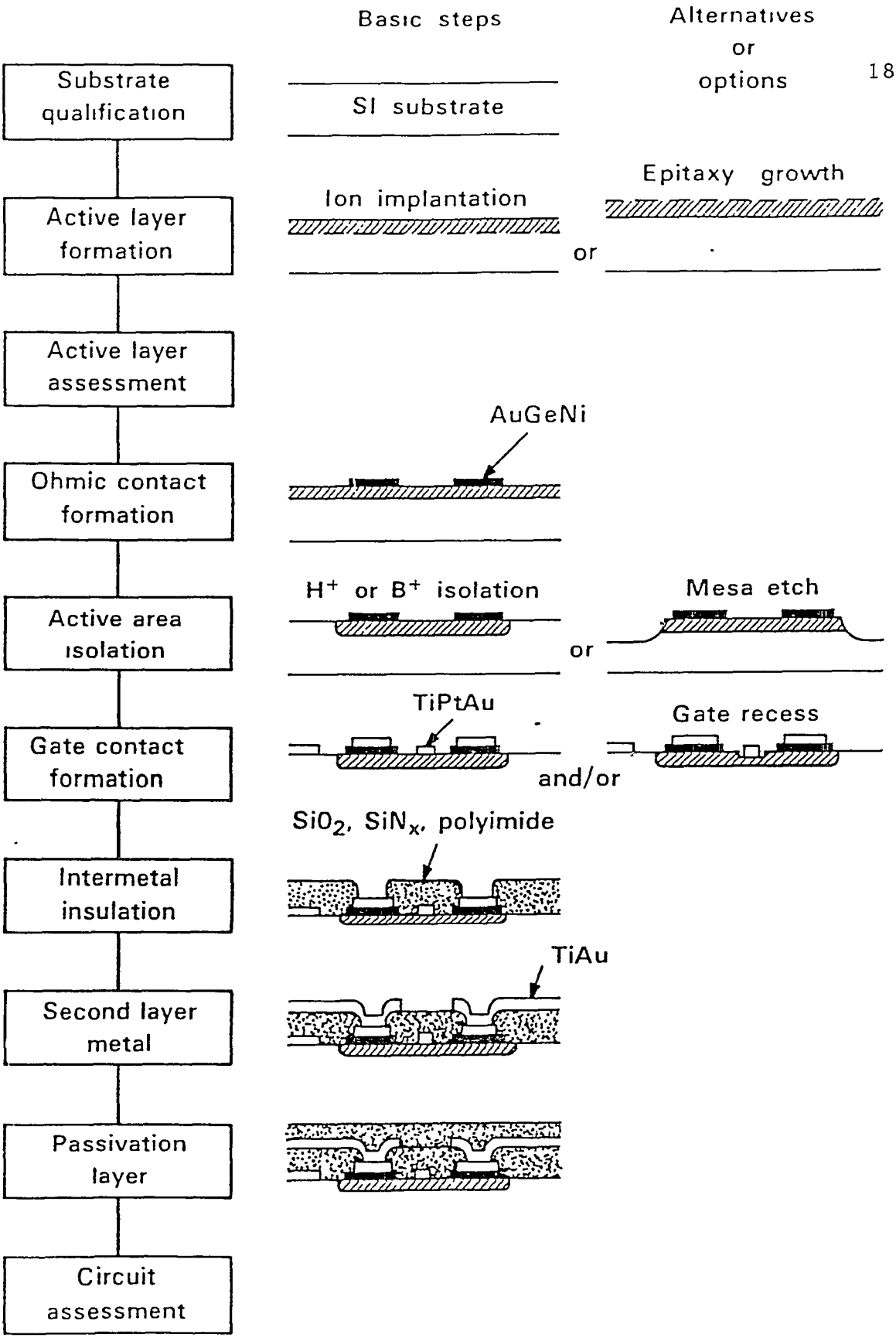


Fig 3.1 Basic digital IC process flow chart

[Mun, 1986]

The next step is to electrically activate these atoms by annealing the wafer, usually at 850 °C for 10 to 30 minutes. To prevent GaAs from dissociating at this temperature, the wafer is enclosed in an arsenic-rich atmosphere or capped with a dielectric layer such as silicon nitride or oxide. Sometimes, two dielectric layers are used to prevent arsenic from escaping from the wafer surface. After the active layer is formed, the doping profile must be determined by CV measurement, before proceeding to MESFET and diode fabrication.

B. Basic MESFET Fabrication

There are three steps necessary for fabricating a MESFET: ohmic contacts, isolation and Schottky gate contact. Both types of metal contacts are normally formed by vacuum deposition and lift-off. The lift-off technique is a pattern transfer process which is capable of high resolution and hence extensively used for discrete devices. In this technique, a positive resist is used to form the resist pattern on the substrate. The film is deposited over the resist and the substrate; the film thickness must be smaller than that of the resist. Those portions of the film on the resist are removed by selectively dissolving the resist layer in an appropriate liquid etchant so that the overlaying film is lifted off and removed. Various recipes are used for ohmic contacts, the most widely used one being AuGeNi, where AuGe is evaporated from a eutectic of 88% Au and 12% Ge by weight to a thickness of 100 nm to 200 nm, followed by a thin layer of Ni of 20 nm to 50 nm. Other combinations, such as InGeAu, AuGeNiAu, etc. can also be used. Post-deposited ohmic metal on GaAs is, in fact, a rectifying junction. In the case of InGeAu, for example, the wafer is heated to about 450 °C for 60 to 90 seconds for the diffusion of Ge into GaAs to take place. Ge

diffuses to a depth of about 50 nm to 100 nm and forms a heavily doped n+ layer under the metal layer, thus producing a low resistivity metal layer. The two ohmic contacts which form the source and drain of the finished MESFET are usually approximately 4 microns apart. Once the ohmics are formed, the next step is to isolate the active areas of all of the MESFETs from each other. At one time this was achieved by etching away the doped GaAs from all unwanted areas with a chemical wet etch to about 0.7 to 1.0 micron depth, leaving the active areas as little mesas but the disadvantage of this technique is that it results in a non-planar surface which can reduce the yield of the subsequent process steps. Now, alternatively, the active areas can be isolated by implanting protons, boron or oxygen, to a 0.7 to 1.0 micron depth. These implants destroy the conductivity of the unwanted active areas by damaging the crystal lattice, which behaves as capture centers for the electrons. It will be seen later that isolation can be eliminated entirely through more advanced processes like selective ion implantation.

The next step in the MESFET fabrication is the deposition of the Schottky gate electrode. Its electrical requirements are the opposite of the ohmic contacts. The contact must have a good stable Schottky barrier height, with a low ideality factor, and preferably low electrode metal resistivity. The ideality factor is related to the voltage dependence of the Schottky barrier height. These parameters can be achieved by using Al, although this metal tends to prove unreliable when subsequently interconnected with Au-based ohmic contacts elsewhere in the circuit, unless care is taken to introduce a suitable barrier layer between all Al and Au interfaces. Apart from Al, most gate contacts are made up of multi-layer metallization, like TiPtAu, TiPdAu and MoAu, where

the lower metal layer which contacts the GaAs, which is chosen for its Schottky barrier properties, may not be easy to deposit or have sufficiently low resistivity. This layer is usually very thin, around 50 nm to 100 nm, and is usually topped up with Au to about 200 nm to 500 nm, according to applications. Au has very low resistivity but it is a fast diffuser and so for reliability purposes, a thin refractory barrier layer like Pt or Pd about 50nm thick is placed between the Schottky barrier layer and the Au layer. Prior to the actual gate metal deposition, a light etch is sometimes carried out on the GaAs, either to control the overall final pinch-off voltage of the MESFETs or, on selected MESFETs, to result in both enhancement mode and depletion mode devices on the same wafer. The gate electrode, usually 1 micron wide, is normally positioned closer to the source contact at about 1 micron separation. This procedure calls for good photolithography control and considerable operator skill.

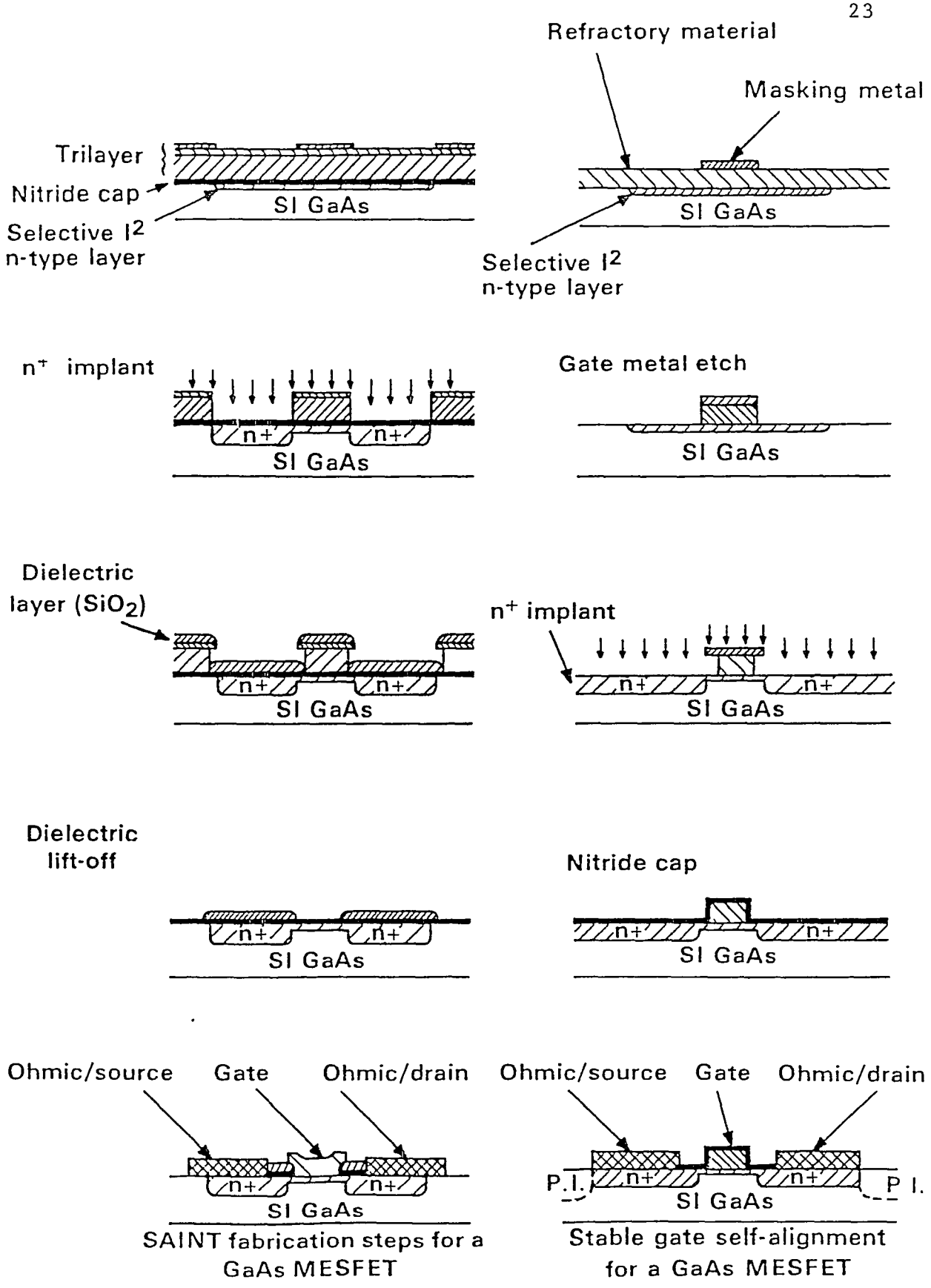
Having isolated the FETs on the wafer, the next step is to interconnect them to form circuits by using multiple layers of metallization, spaced with suitable dielectric insulation layers. For process simplicity, the gate metal is generally used as the lower interconnection layer, is formed at the same time as the gate deposition. Insulation between this layer and the next level metal is by either polyimide, SiO_2 or Si_3N_4, usually of 0.5 to 1 micron thickness. A number of methods can be used for the deposition of these dielectrics, like spin-on, evaporation, sputtering or CVD, but care should be taken that the process temperature is kept low, to avoid damaging both the Schottky barrier gate contact and the active GaAs surface between the electrodes. Windows in the dielectric insulation are then opened by either a chemical wet etch or a dry etch, the latter being more universally used today. The second metal

layer for the final interconnection is then deposited, thus completing the circuit. Because of its slightly large dimensional tolerance, it can be delineated either by evaporation/lift-off or sputter-ion beam milling. The latter is rapidly gaining popularity because of its batch process capability and its ability to produce thicker metals, up to 1 micron, preferred for the second metal. The second metal is usually Au over a thin, adhesion-promoting lower layer like Ti or Mo. The final dielectric passivation though similar to the insulating layer, is however, optimal since the FETs are already passivated by the first insulating layer. The final passivation layer is, in fact, an anti-scratch layer to protect the second level metal.

C. State-of-the-art Digital IC Technologies

The most significant recent developments in the technology are the self-alignment processes. Indications are that they will form the future standard technologies for GaAs digital ICs. The purpose of the technologies is to bring the ohmic, and usually the n+, contacts to as near the gate contacts as possible, without sacrificing yield or producing undesirable electrical effects such as short channels. There are two important advantages of the self-aligned processes. First, the device performance is significantly improved by minimizing parasitics to the practical limit. This enables MESFET performances close to the intrinsic values to be obtained. Second, the critical positioning of the gate contact relative to ohmic/n+ is eliminated. Improvement in performance also brings a simultaneous improvement in yield, two parameters which usually work against rather than for, each other.

Two self-alignment techniques are currently in production. The first is



SAINT fabrication steps for a GaAs MESFET

Stable gate self-alignment for a GaAs MESFET

Fig 3.2 Two state of the art self-alignment technologies

[Mun, 1986]

known as SAINT, for Self Aligned Implantation N+ Technology [K.Yamasaki, Feb.1982]. Its key features are shown in fig 3.2. It relies on a series of dielectric masking layers to control the fine spacing required, usually between 0.1 and 0.2 microns, between the edge of the n+ ohmic and gate contacts. The gate contact is self aligned by these dielectric layers during the n+ stage and critical alignment is eliminated. The process, though lengthy in terms of the steps involved for the deposition and etching of these dielectric layers is, in fact, the least compromising in terms of device parameters. Conventional low resistance gate metallurgy can be used, due to which, gate breakdown and short channel effects are well controlled.

The second self-alignment is a totally different approach [M. Abe, July 1982]. In the basic process, which is simple and elegant, the gate metal electrode is used as the n+ implantation mask so that the n+ contacts are automatically aligned to the gate in one simple step. The gate contact must, however, meet a very stringent stability requirement for the high temperature n+ anneal. The most promising ideal contacts are currently co-sputtered AlW, TiW silicide, Ti silicide, etc. Most high temperature stable metallizations also have much higher resistivity than conventional Au overlayed gate metallisations, usually by an order of magnitude, and prevents them from being used in circuits requiring long gate widths. Such a closeness between the n+ and gate electrodes also creates leakage and breakdown problems. These can be overcome by additional masking steps and overlays and so that the final process may not differ a great deal from the SAINT in terms of complexity.

D. Conventional Planar Structure Process

The fabrication sequence of a conventional planar structure process for MESFET fabrication shown in fig 3.3 [Einspruch, 1985], employs multiple localized ion implantations directly into semi-insulating GaAs substrate. This fabrication technology is often used by SDFL circuits. In SDFL circuits, the depletion mode MESFET is used. Since any region of the source-drain channel except the region directly under the gate is conductive for a DFET, it is not necessary to use precise gate alignment for avoiding parasitic resistance that is used in enhancement mode MESFET. Though the conventional planar structure process performs well for SDFL circuits, the self-aligned gate results in size reduction.

E. Self-aligned Gate Planar Process

The fabrication sequence of a Self-aligned gate planar process is shown in fig 3.4 [Williams, 1984]. When processing enhancement mode MESFET by conventional planar structure process, the thinness of the undepleted n-layer greatly raises the source and drain resistance and hence, results in poor transconductance. Therefore, when a process with a self-aligned gate is employed, the n+ layer is expected to prevent the extension of surface and interface layers so that the undepleted n+ layer considerably reduces parasitic resistance. This process also allows a higher integration density. Therefore, enhancement mode MESFET could perform better when the self-aligned gate process is employed for its fabrication. Since most DCFL circuits use enhancement mode MESFET for load, most DCFL circuits are fabricated by a self-aligned gate process [Nakayama, 1982] [N.Yokoyama, 1984].

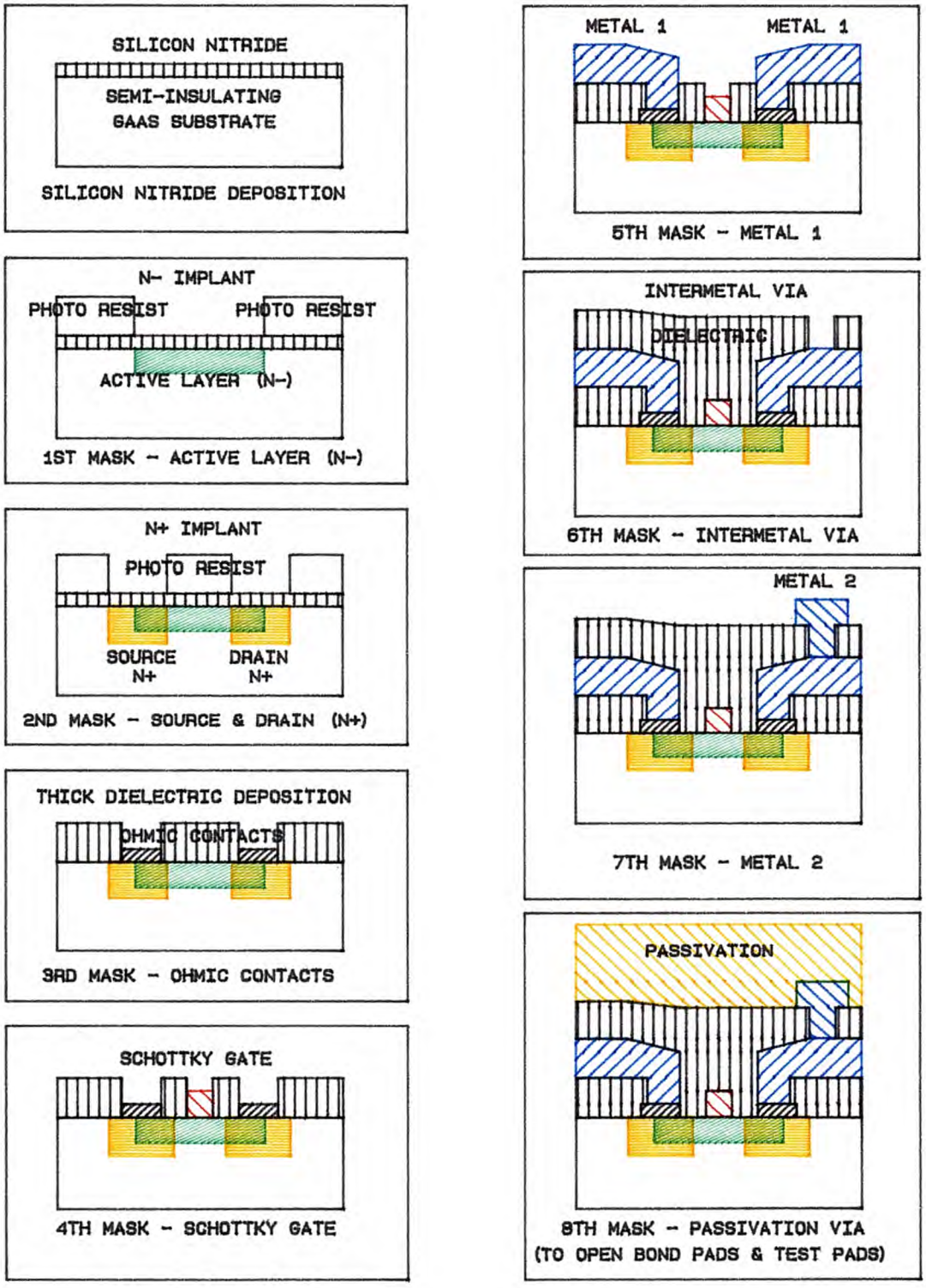


FIG 3.3 FABRICATION SEQUENCE OF A CONVENTIONAL PLANAR STRUCTURE PROCESS
[EINSPRUCH, 1985]

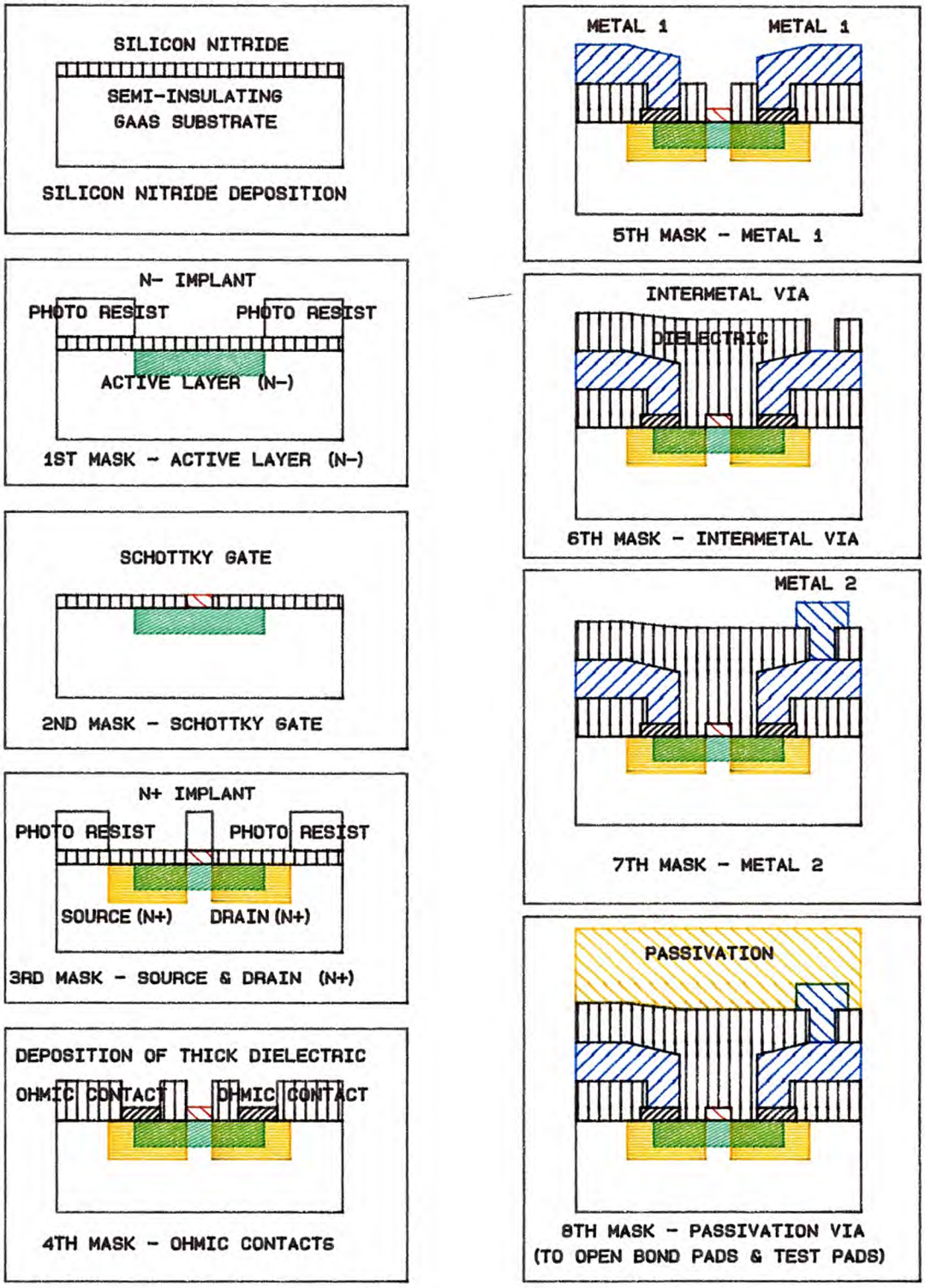


FIG 3.4 FABRICATION SEQUENCE OF A SELF-ALIGNED GATE PLANAR STRUCTURE PROCESS [WILLIAMS, 1984]

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CHAPTER IV

TEMPERATURE DEPENDENT PARAMETERS IN GAAS

A. P-n Junction Theory

A p-n junction is formed at the interface on an n-type and a p-type semiconductor brought into intimate contact; it is defined as a sharp boundary within a semiconductor crystal with predominantly donor impurities on one side and predominantly acceptor impurities on the other side. If there is no external voltage applied between the two sides, then the Fermi level exists at a single energy value throughout the crystal. At the p-n junction, conduction and valence bands are warped in such a way that the two majority carrier distributions are confined to their own areas, the warping being just sufficient to establish that no net current flows across the junction. In equilibrium the current flow across the junction is composed of two equal components of opposite sign (no net current in the transition region); one component is due to the carrier diffusion and the other is due to carrier drift as a result of the built-in electric field as shown in fig 4.1 [S.M. Sze, 1985].

If an external voltage V is applied to a p-n junction, this equilibrium is distributed. If a forward bias is applied, the Fermi levels on both sides of the junction are different by an amount qV. The barrier to the flow of majority carriers is thus lowered so that more carriers are above the top of the barrier and a current can flow which increases exponentially with voltage. Holes are flowing through the p-type region and recombine with electrons which have crossed the junction or move over into the n-type region and recombine there. The behavior of electrons is analogous.

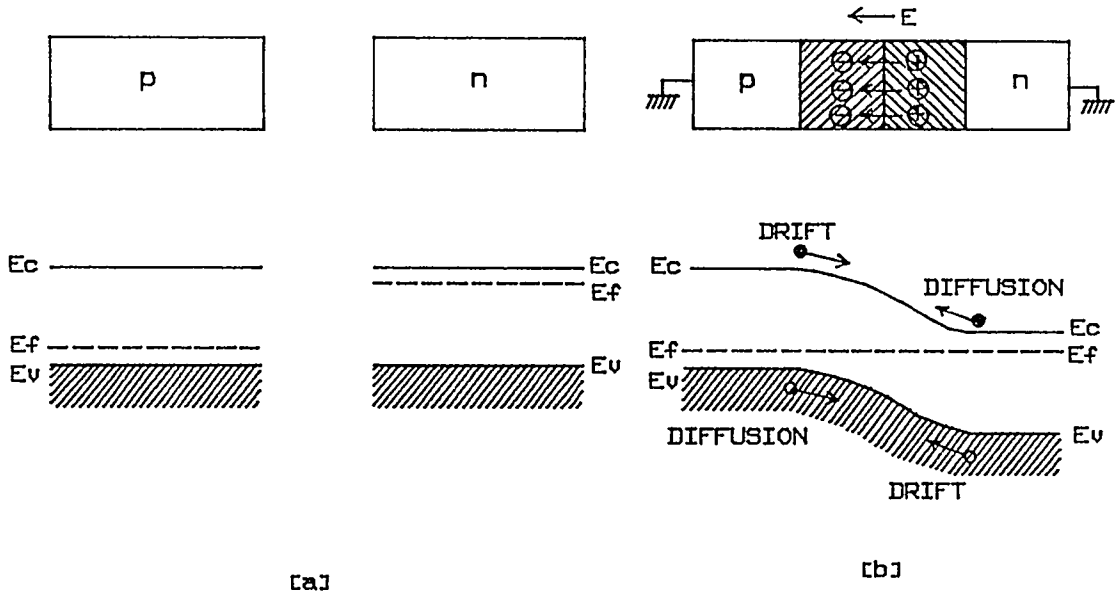


Fig 4.1

[a] Uniformly doped p-type & n-type semiconductors before junction is formed

[b] The electric field in the depletion region & the energy band diagram of a p-n junction in thermal equilibrium

If a reverse voltage is applied, the barrier is raised so that fewer majority carriers are above the top of the barrier and the flow of carriers across the junction is restricted and reaches, in the ideal case, a saturating value. The only current is carried by minority carriers which are easily swept across the region of the accelerating field. The magnitude of this current is ideally independent of the applied voltage, and only determined by the abundance of minority carriers in the two regions. It results from the thermal generation of carriers and is, therefore, a function of temperature. At a high reverse voltage avalanche breakdown sets in.

In the transition region between n-type and p-type regions a charge dipole region or depletion layer is created by the carriers diffusing out of the regions and leaving the ionized impurity atoms on either side unneutralized. The sum of built-in and applied voltage- the total voltage across the junction- charges the layer by repelling more majority carriers away from the junction and by exposing more impurity ions on both sides. Thus the depletion layer widens with voltage and behaves like a voltage-dependent capacitance. Essentially the entire drop of the applied voltage occurs across the depletion layer.

A voltage applied to p-n junction will disturb the precise balance between the diffusion current and drift current of electrons and holes. Under forward bias, the applied voltage reduces the electrostatic potential across the depletion region. The drift current is reduced in comparison to the diffusion current. We have an enhanced hole diffusion from the p-side to the n-side and electron diffusion from the n-side to the p-side. Therefore, minority carrier injections occur, that is electrons are injected into the p-side, while holes are injected into the n-side.

B. Forward-Biased GaAs Diode

The first metal-semiconductor contact was in the form of a point contact rectifier, that is, a metallic whisker pressed against the semiconductor surface. Fig 4.2 [S.M. Sze, 1985] shows a perspective view of a metal-semiconductor contact. This device found many applications as early as 1904. In 1938, Schottky suggested that the rectifying behaviour could arise from a potential barrier as a result of stable space charges in the semiconductor. The structure arising from this consideration is known as the Schottky diode. Metal-semiconductor contacts can also be non-rectifying; that is, the contact has a negligible resistance regardless of the polarity of the applied voltage. Such a contact is known as the ohmic contact. All semiconductor devices as well as integrated circuits need ohmic contacts to make connections to other devices in an electronic system. In order to understand the effect of a Schottky barrier, the boundary of an n-type semiconductor is considered as shown in fig 4.3 [Shur, 1987]. The potential energy of the electrons in the crystal is smaller because the electrons are attracted by the positive ions of the crystal lattice. However, owing to the thermal motion some electrons have energy higher than $E_c + X_{so}$ may leave the crystal.

The behavior of the current-voltage characteristics of a Schottky barrier can be explained in terms of either the diode or the diffusion theory. The choice of either one depends upon the width of the depletion region with respect to the mean free path of electrons scattered by acoustical phonons. When usual approximations are made, both derivations result in essentially the same I-V dependence:

$$I = I_s \, [\exp (qV / kT) - 1],$$

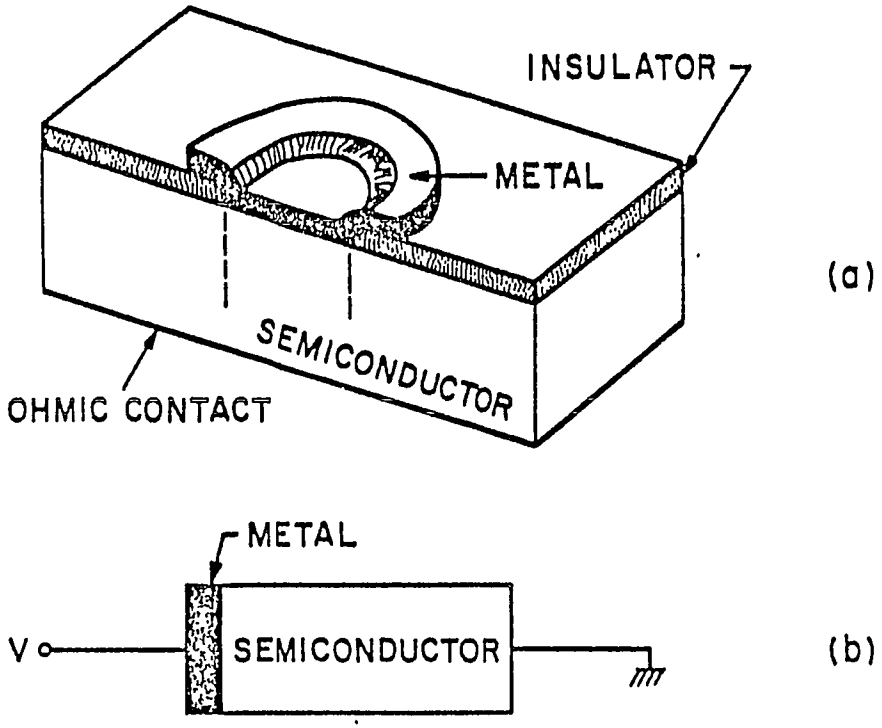


Fig 4.2 (*a*) Perspective view of a metal–semiconductor contact fabricated by the planar process. (*b*) One-dimensional structure of a metal–semiconductor contact.

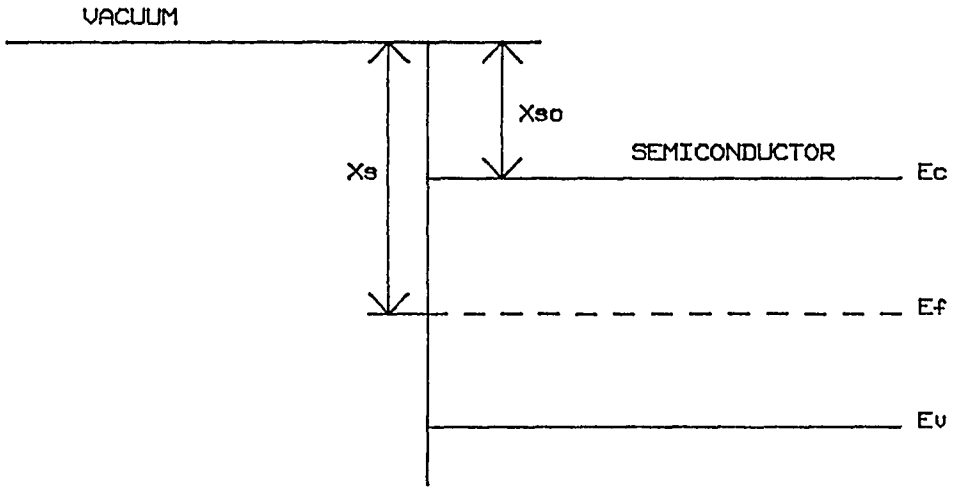


Fig 4.3 Potential distribution at the semiconductor surface

Ec = bottom of the conduction band

Ev = top of the valence band

Ef = Fermi level

Xs = work function

Xso = electron affinity

CURRENT		10 UA	1UA	100NA	10NA	1NA	100PA	10PA	1PA
T	25C	0.922V	0.809V	0.691V	0.563V	0.445V	0.321V	0.200V	0.090V
E									
M	50C	0.868V	0.745V	0.618V	0.500V	0.326V	0.236V	0.105V	0.000V
P	100C	0.736V	0.591V	0.450V	0.304V	0.154V	0.041V	0.000V	0.000V
E									
R	150C	0.636V	0.481V	0.325V	0.163V	0.041V	0.000V	0.000V	0.000V
A									
T	200C	0.527V	0.350V	0.172V	0.045V	0.000V	0.000V	0.000V	0.000V
U									
R	250C	0.400V	0.220V	0.063V	0.009V	0.000V	0.000V	0.000V	0.000V
E	300C	0.291V	0.100V	0.013V	0.000V	0.000V	0.000V	0.000V	0.000V

TABLE 4.1

GaAs DIFFUSED DIODE VOLTAGES AT DIFFERENT TEMPERATURES

[AFTER GROVE, 1967]

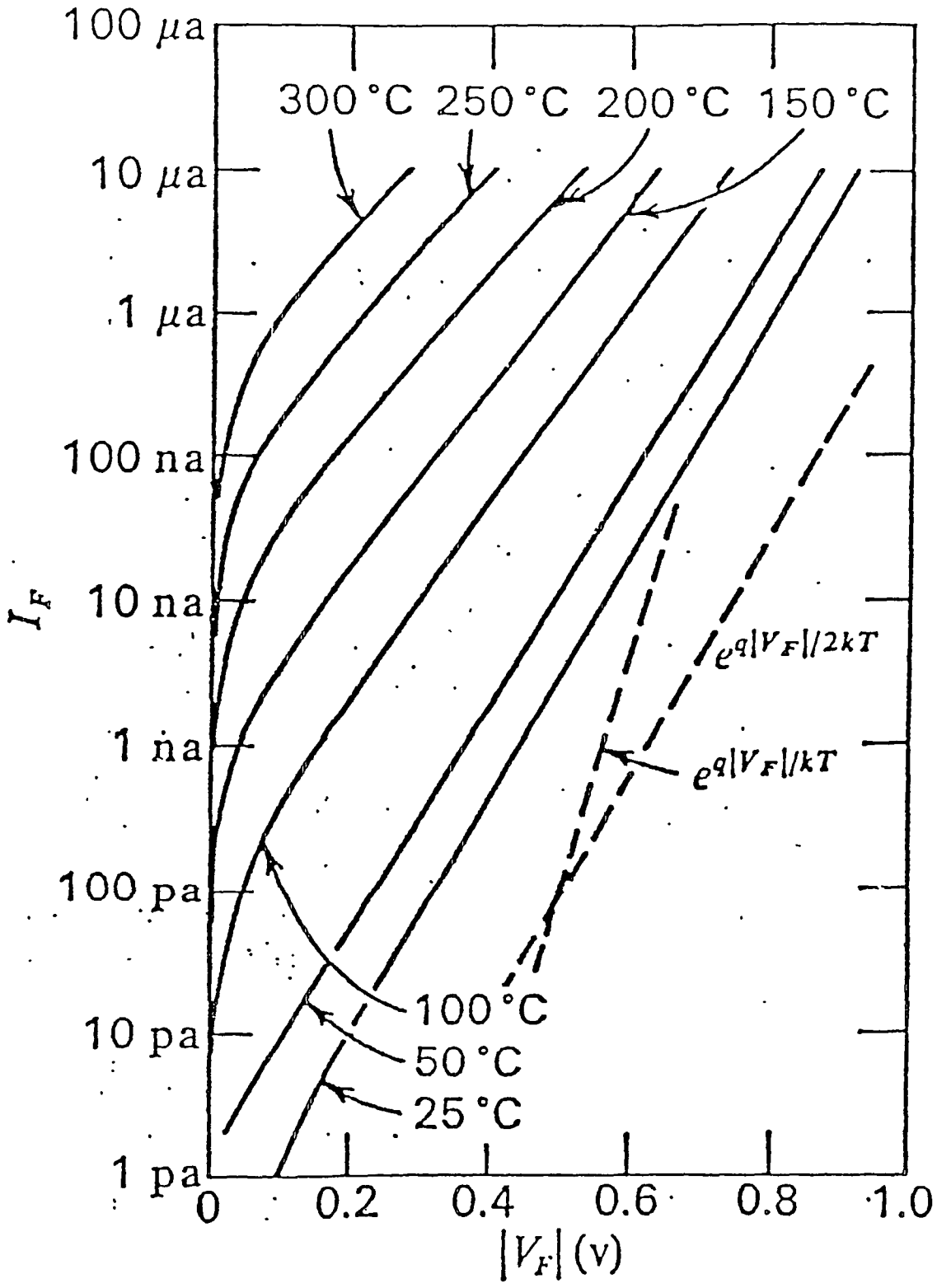
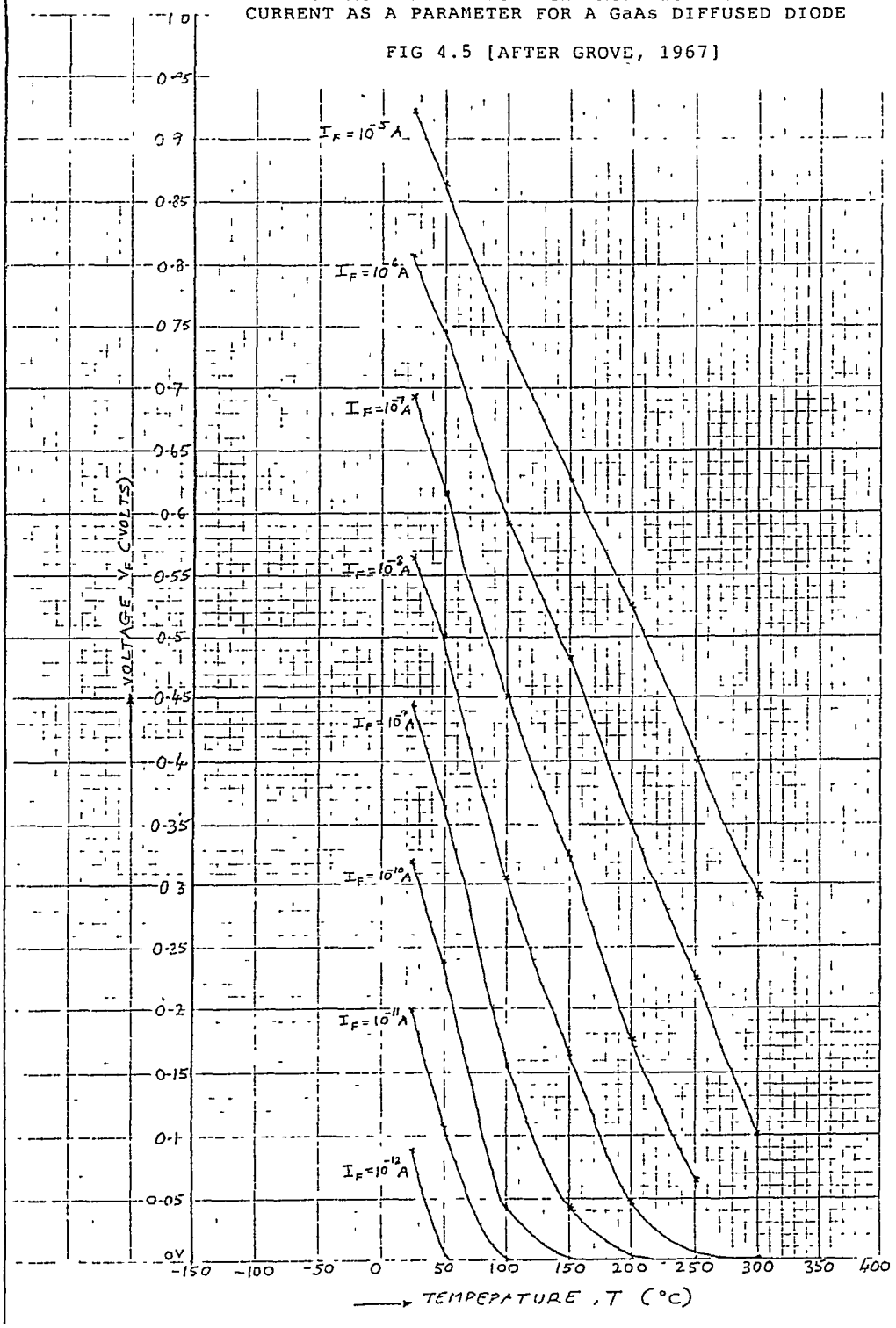


FIG 4.4

CURRENT-VOLTAGE CHARACTERISTICS WITH TEMPERATURE AS PARAMETER FOR A GaAs DIFFUSED DIODE [GROVE, 1967]

VOLTAGE-TEMPERATURE CHARACTERISTICS WITH CURRENT AS A PARAMETER FOR A GaAs DIFFUSED DIODE

FIG 4.5 [AFTER GROVE, 1967]



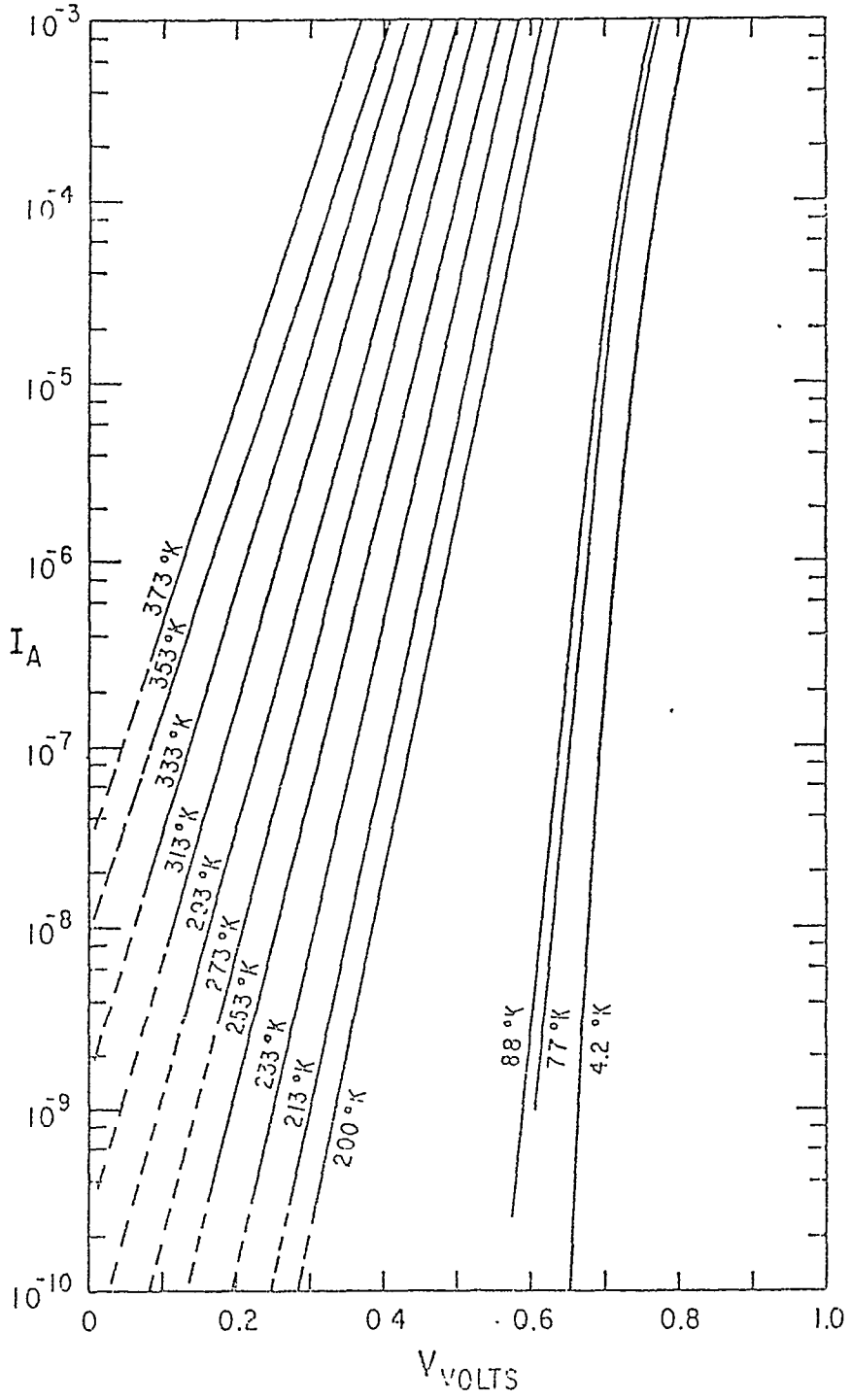


FIG 4.6a

FORWARD I-V CHARACTERISTICS AT DIFFERENT TEMPERATURES OF A TYPICAL Au-GaAs SCHOTTKY DIODE [PADOVANI & SUMNER, 1965]

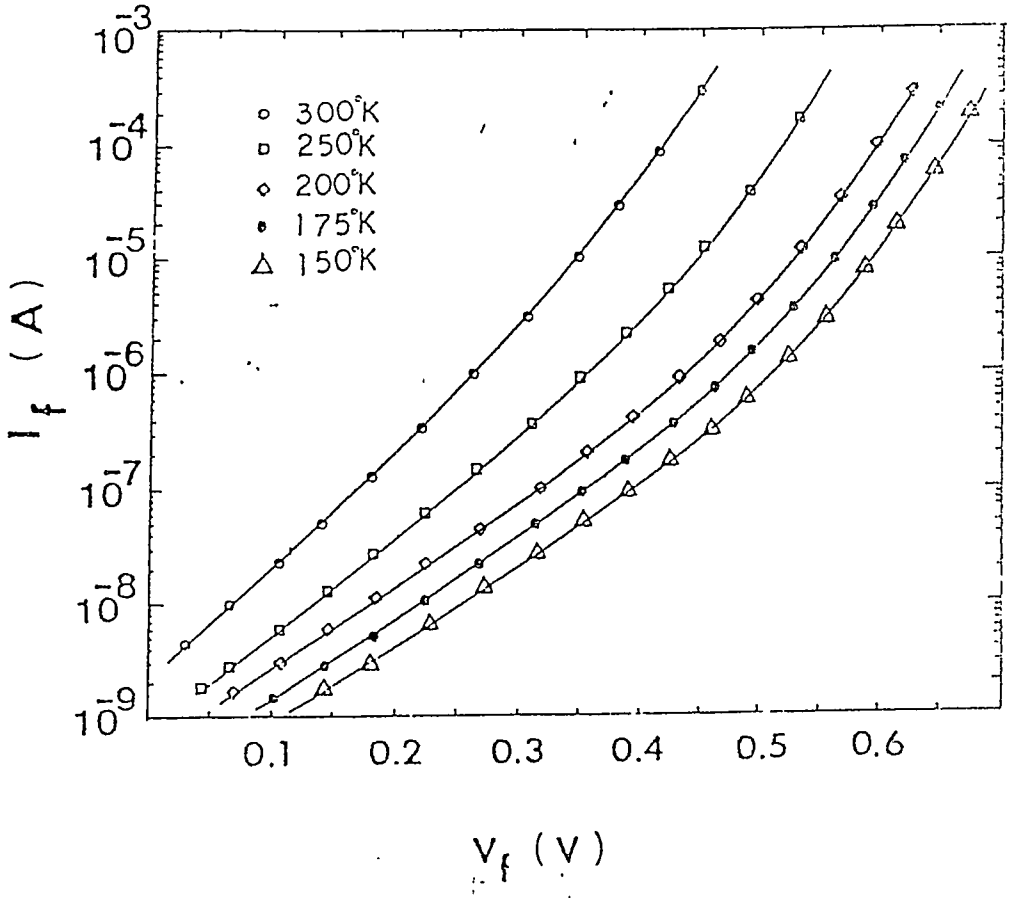


FIG 4.6b

FORWARD I-V CHARACTERISTICS AT DIFFERENT TEMPERATURES FOR AN Au-GaAs SCHOTTKY DIODE

[CHEN & WIE, 1988]

Grove	Chen & Wie	Padovani & Sumner
$J = 31.25\ A/cm^2$	$J = 0.00127\ A/cm^2$	$J = 0.0155\ A/cm^2$
$\frac{\delta V_d}{\delta T} = 2.25\ mV/^\circ C$	$\frac{\delta V_d}{\delta T} = 1.5\ mV/^\circ C$	$\frac{\delta V_d}{\delta T} = 1.96\ mV/^\circ C$
Ideality factor = 1.48	Ideality factor = 1.0 $V_d > 0.3\ V$ Ideality factor = 1.428 $V_d < 0.3\ V$	Ideality factor = 3.27

Table 4.2

Comparison of three references

for GaAs diode I-V curves

[At 300°K]

where the saturation current I_s depends only on temperature and barrier height in the diode theory. In the diffusion theory, I_s also depends slightly on the applied voltage. A slight deviation from such an ideal behavior was reported which was due to recombination in the space charge layer and, by analogy with the p-n junction, the experimental results fit the following expression:

$$I = I_s \left[\exp (qV / nkT) - 1 \right],$$

where n is a dimensionless number usually not too different from unity at room temperature.

Table 4.1 [after A.S. Grove, 1967], lists the GaAs diffused diode voltages at different temperatures for each given current. In fig 4.4 [Grove, 1967] experimentally obtained V-I curves for a GaAs diode are shown at different temperatures. These have been transformed into those shown in fig 4.5a, where the relationship between voltage applied and temperature is obtained at different values of the diode currents. Fig 4.6a shows the forward I-V characteristics of a typical Au-GaAs Schottky diode over a temperature range of 4.2 °K to 373 °K [Padovani and Sumner, 1965]. Fig 4.6b shows the forward I-V characteristics for a Au-GaAS Schottky diode with an Indium concentration of 6.54×10^{19} cm^{-3}, over a temperature range of 150 °K to 300 °K [Chen and Wie, 1988]. Table 4.2 gives a comparative study of the three sets of forward I-V curves from the above mentioned three references. It is found that the curves shown in fig4.5a [after Grove, 1967] are best suited for the sensor design because of the availability of I-V curves at higher temperatures i.e., upto 300 °C. Hence these curves are chosen as the reference in the design of the temperature sensing diode pair.

C. MESFET Characteristics & Models for Simulation

A typical GaAs MESFET structure has an active layer, two ohmic contacts and a Schottky gate. Ohmic contacts are made to the source and the drain. The Schottky gate which is located between the source and the drain, performs a channel modulation function. In fig 4.7, we see the device profile of a non-self-aligned GaAs MESFET biased at Vdd=0. Fig 4.8 shows the device profile for a self-aligned GaAs MESFET. In the figures shown, MESFETs are of n-channel type, L(gate length) = 1um, Y(Source-drain length)= 5um, gate width= 50 um, doping density = 10^{17}/ cm. The depletion layer beneath the gate is symmetric and the depletion depth depends on Vgs. When Vgs is negative compared to the threshold voltage, the channel will be turned off. The non-self-aligned MESFET has an extended depletion region beyond the gate which is not there in the self-aligned MESFET. In the self-aligned MESFET, the high doping n+ region i.e., the source and the drain region, prevents the depletion region from extending and hence substantially reduces the parasitic resistance.

When a positive drain-source bias voltage is applied, the depletion layer becomes asymmetric and the depletion depth increases along the source to the drain. This can be seen for a non-self-aligned GaAs MESFET in fig 4.9, and for a self-aligned GaAs MESFET in fig 4.10. It can be also observed that, the depletion depth is highest near the drain because of a larger reverse bias near the drain. When a positive drain-source bias is applied, electrons will flow from the source to the drain and result in current (Ids) flow from the drain to the source. The gate-source voltage Vgs, performs a channel current modulation.

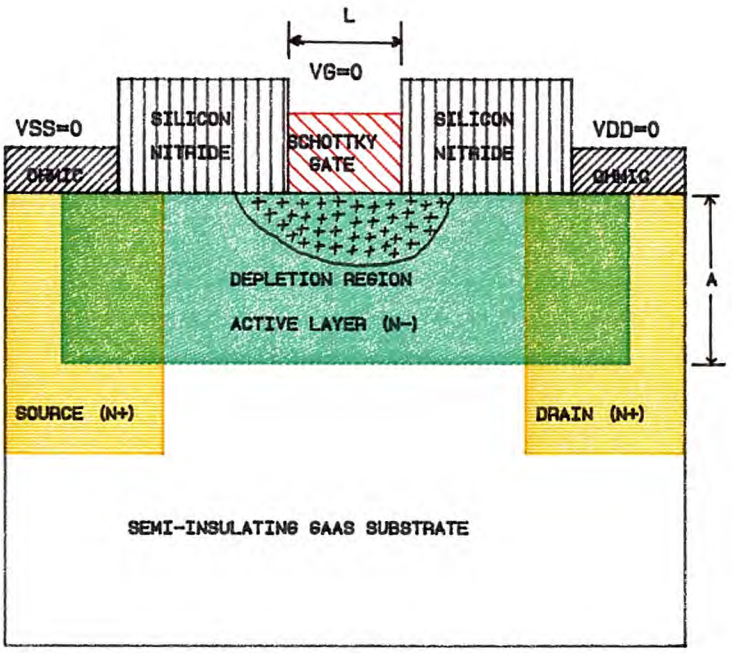


FIG 4.7
DEVICE PROFILE FOR A NON-SELF-ALIGNED
GAAS MESFET AT VDD=0

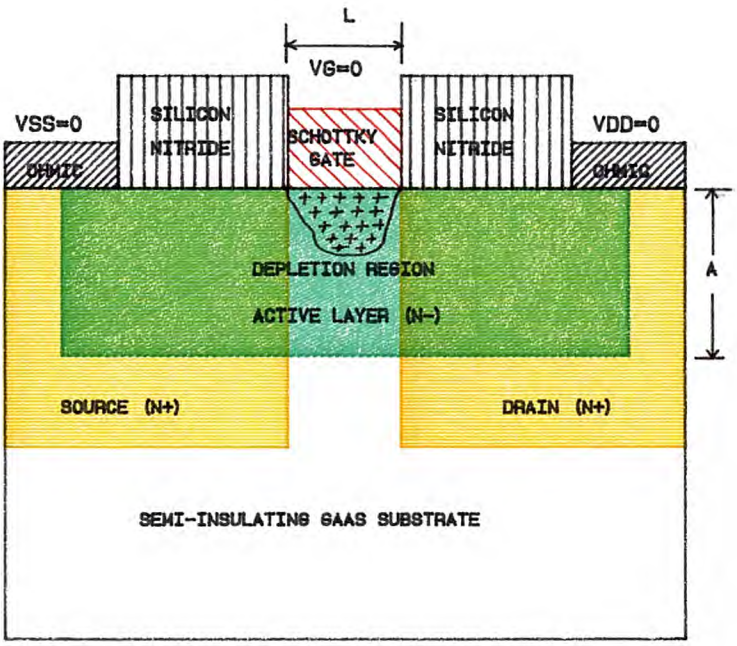


FIG 4.8
DEVICE PROFILE FOR A SELF-ALIGNED
GAAS MESFET AT VDD=0

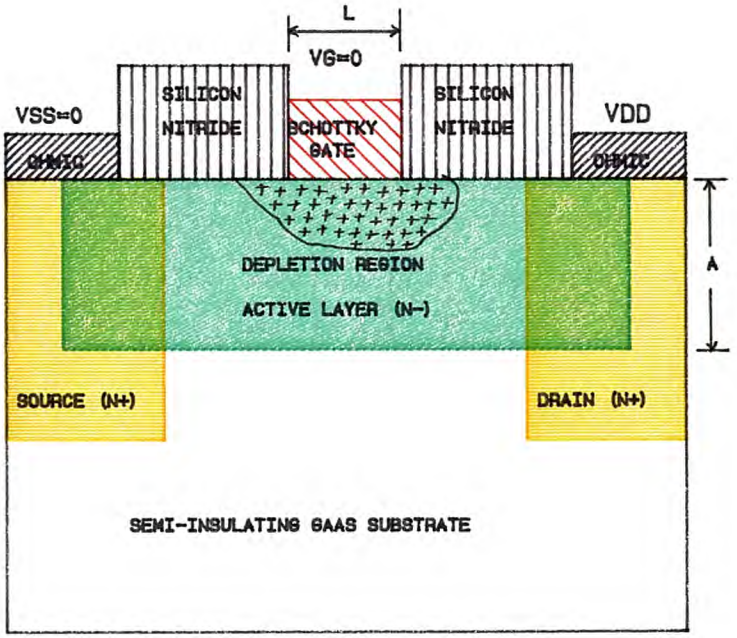


FIG 4.9
DEVICE PROFILE FOR A NON- SELF-ALIGNED
GAAS MESFET WITH VDS APPLIED

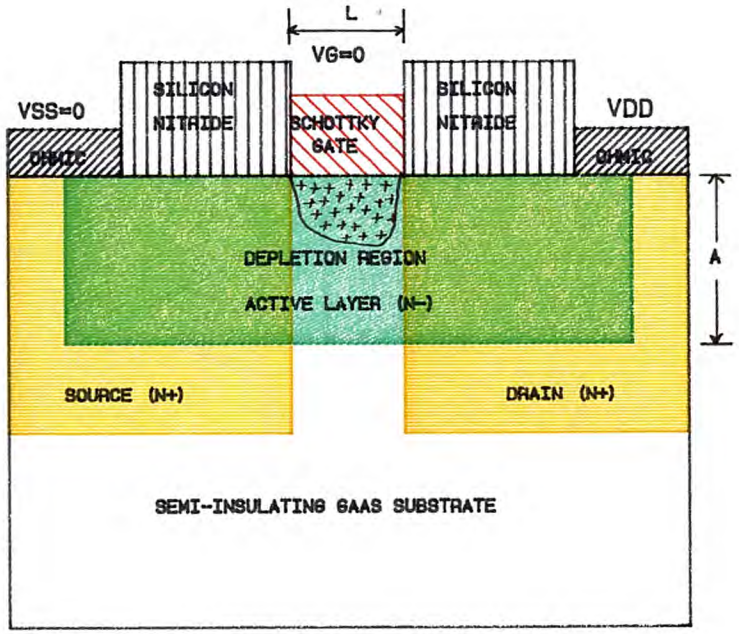


FIG 4.10
DEVICE PROFILE FOR A SELF-ALIGNED
GAAS MESFET WITH VDS APPLIED

When Vgs is smaller compared to the threshold voltage, then, irrespective of the value of Vds, the channel current (Ids) is small. When the Vgs is equal to or greater than the threshold voltage, the channel turns on and the channel current increases with increase in Vds. The device is said to reach saturation when Ids ceases to increase with further increase in Vds. In the MESFET structures shown above, the extended depletion region beyond the gate is existing in the non-self-aligned MESFET but not in the case of a self-aligned MESFET.

JFET Model : The GaAs MESFET is modeled similar to the Silicon JFET model used originally in the SPICE program. Since the transfer characteristics of a Si JFET are very similar to those of a GaAs MESFET, the JFET model has been often used to simulate a MESFET. The JFET model is shown in fig 4.11 and the equations below describe the model [Curtice, 1980]:

Drain current, $I_d = 0, \quad for \quad V_{gs} - V_T < 0$

$$I_d = \beta(V_{gs} - V_T)^2(1 + \lambda V_{ds}), \quad for \quad 0 < V_{gs} - V_T < V_{ds}$$

$$I_d = \beta V_{ds}[2(V_{gs} - V_T) - V_{ds}](1 + \lambda V_{ds}), \quad for \quad 0 < V_{ds} < V_{gs} - V_T$$

Where, β is the transconductance parameter

λ is the channel length modulation parameter.

GaAs MESFET Model : Although many GaAs MESFET simulations have used the JFET model, a number of problems remain unsolved. The JFET model is in error at the drain current-voltage relationships below the current saturation [Curtice, 1980]. The physical reason being that in Gallium Arsenide the electron velocity saturates at a rather low electric field of $3x10^3$ v/cm,

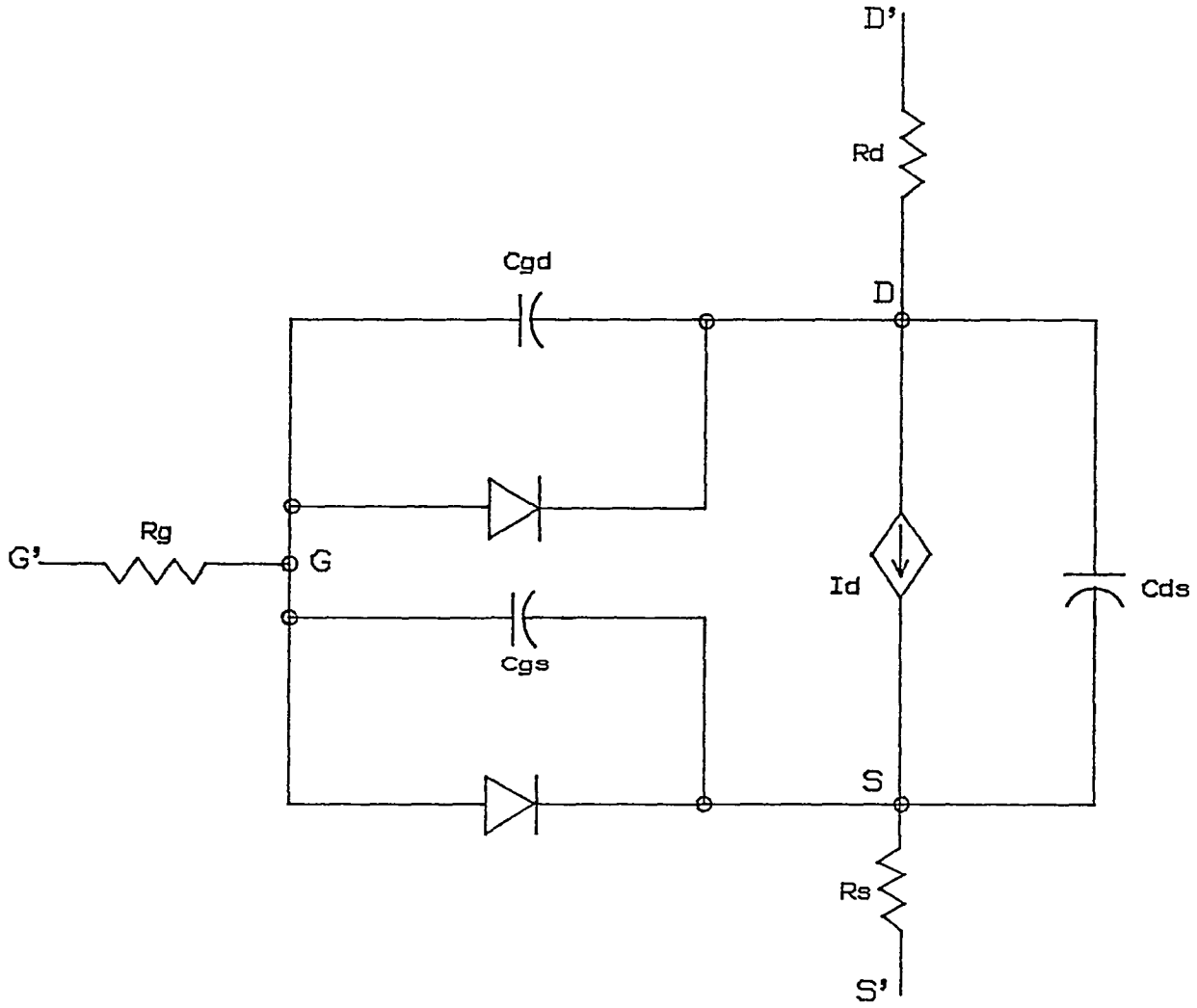


Fig 4.11 JFET Model for n-channel GaAs MESFET

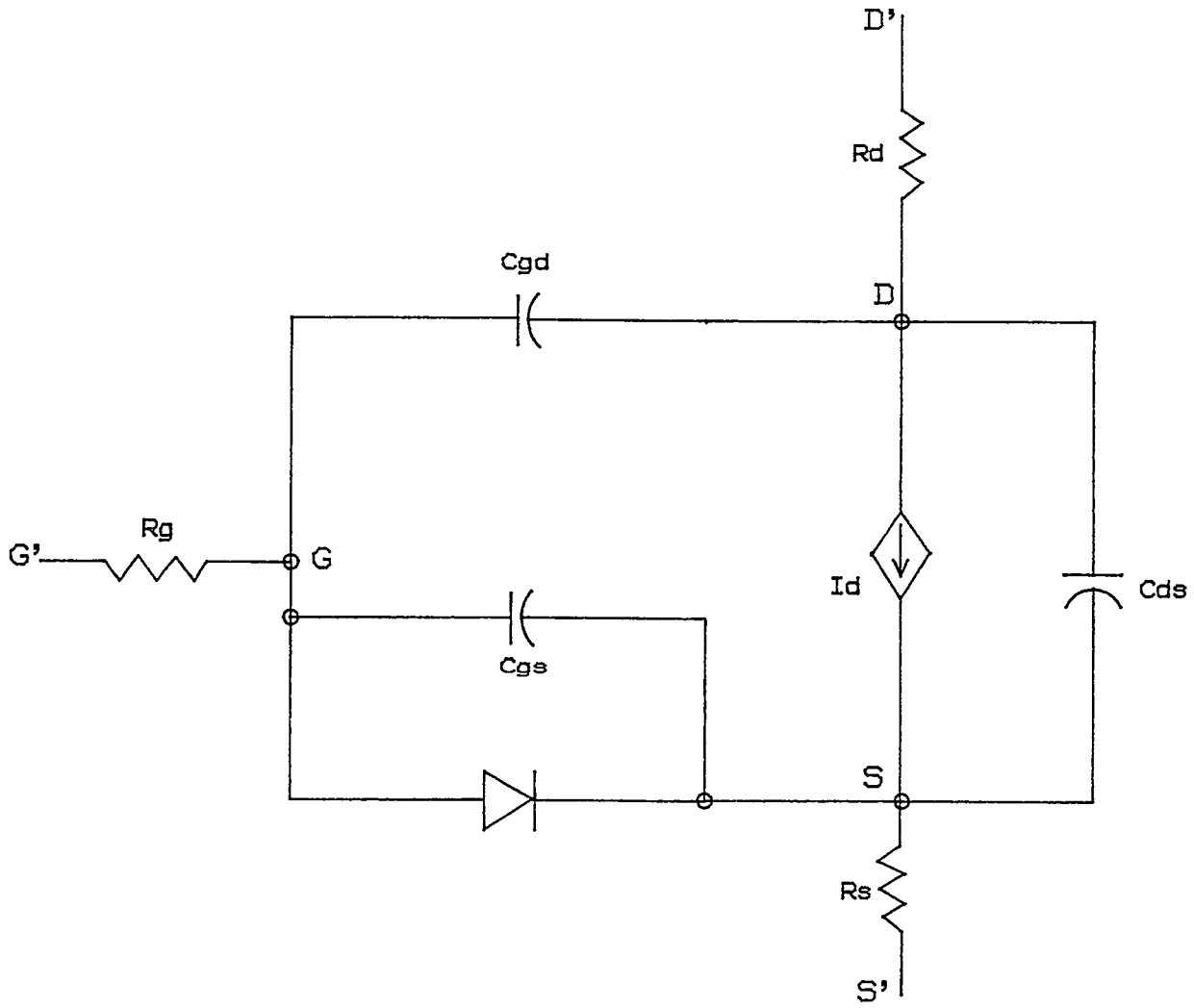


Fig 4.12 Model for n-channel GaAs MESFET

whereas Si exhibits ohmic behaviour to an order of magnitude over GaAs. In GaAs the saturation of drain current with increasing drain to source voltage is caused by carrier velocity saturation, whereas in Si it is the channel pinch-off that causes the drain current to saturate. The MESFET model was proposed by W.R. Curtice in 1980. The simulation results using the MESFET model were found to be more accurate than those obtained using the JFET model. Later on the model proposed by Curtice was adopted for MESFET simulation in SPICE 3B.1. The n-channel MESFET model used in SPICE 3B.1 is shown in fig 4.12 and is described by the following equations [Statz, 1987]:

$$I_d = \frac{\beta(V_{gs}-V_T)^2}{1+b(V_{gs}-V_T)}[1-[1-\alpha\frac{V_{ds}}{3}]^3](1+\lambda V_{ds}), \quad for \quad 0 < V_{ds} < \frac{3}{\alpha}$$

$$I_d = \frac{\beta(V_{gs}-V_T)^2}{1+b(V_{gs}-V_T)}(1+\lambda V_{ds}), \quad for \quad V_{ds} > \frac{3}{\alpha}$$

$$I_{ds} = \frac{\beta(V_{gs}-V_T)^2}{1+b(V_{gs}-V_T)}$$

$$Q_g = 2C_{gso}V_{bi}[1-(1-\frac{V_{gs}}{V_{bi}})^{\frac{1}{2}}]+C_{gdo}V_{gd}, \quad for \quad V_{ds} >> 0 \; or \; -V_{gd} >> -V_{gs}$$

$$Q_g = 2C_{gso}V_{bi}[1-(1-\frac{V_{gd}}{V_{bi}})^{\frac{1}{2}}]+C_{gdo}V_{gs}, \quad for \quad V_{ds} << 0 \; or \; -V_{gd} << -V_{gs}$$

$$C_{gs} = \frac{dQ_g}{dV_{gs}} = \frac{C_{gso}}{[1-\frac{V_{gs}}{V_{bi}}]^{\frac{1}{2}}}, \quad for \quad V_{ds} > 0$$

$$C_{gd} = \frac{dQ_g}{dV_{gd}} = C_{gdo}, \quad for \quad V_{ds} > 0$$

$$C_{gd} = \frac{dQ_g}{dV_{gd}} = \frac{C_{gso}}{[1-\frac{V_{gd}}{V_{bi}}]^{\frac{1}{2}}}, \quad for \quad V_{ds} < 0$$

$$C_{gs} = \frac{dQ_g}{dV_{gs}} = C_{gdo}, \quad for \quad V_{ds} < 0$$

Where,

V_T = threshold voltage

β = transconductance parameter

b = doping tail extending parameter

α = saturation voltage parameter

λ = channel length modulation parameter

V_{bi} = gate junction potential

C_{gso} = zero-bias Gate-Source junction capacitance

C_{gdo} = zero-bias Gate-Drain junction capacitance.

The MESFET dc characteristics are defined by the parameters V_T, b and β, which determine the variation of drain current with gate voltage. α determines the saturation voltage, and λ determines the output conductance. Charge storage is modeled by the total gate charge as a function of gate-drain and gate-source voltages and is defined by the parameters C_{gso}, C_{gdo} *and* V_{bi}.

D. References

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CHAPTER V

TEMPERATURE SENSOR CELL SIMULATION AND PHYSICAL LAYOUT

A. Design of the Sensor Circuit

The temperature sensor circuit has been designed using 1 um gate length depletion mode GaAs MESFETs. The sensor circuit can be used as a standard cell in GaAs ICs to safeguard the chip when it gets too hot. The precise temperature at which the circuit rings a bell can be set easily by suitably adjusting the aspect ratios of the MESFETs in the circuit. The principle on which the circuit has been built is described below.

The temperature is sensed by a pair of GaAs diffused diodes having different areas. The following is the standard current-voltage relationship for a GaAs diode-

$I_d = I_s\ A_d\ exp(qV/nkT)$

Hence, $V = \frac{nkT}{q}\ ln[\frac{I_d}{I_s\ A_d}]$

where, I_s is the saturation current, I_d is the current flowing through the diode, q is the electronic charge (1.602 x 10^{-19} Coul), A_d is the area of the diode, k is the Boltzmann constant (1.3806 x 10^{-23} Joules/^{o}K), T is the absolute temperature in degrees Kelvin, V is the voltage across the diode and n is a dimensionless constant.

If V_1 and V_2 are the voltages across the two temperature sensing diodes,

$V_1 = \frac{nkT}{q}\ ln[\frac{I_1}{I_s\ A_1}]$

$V_2 = \frac{nkT}{q}\ ln[\frac{I_2}{I_s\ A_2}]$

Hence, $V_2 - V_1 = \frac{nkT}{q}\ ln[\frac{I_2\ A_1}{I_1\ A_2}]$.

If the same current is flowing in both the diodes, then the ratio $\frac{I_2}{I_1}$ is unity. hence, $(V_2 - V_1)$ is proportional to the product $T\ ln[\frac{A_1}{A_2}]$. Thus, the differential voltage tapped across the diodes is a function of the temperature and the ratio of the diode areas. Since the diode areas are fixed, the differential voltage is a function of the temperature sensed by the diodes. To get substantial differential voltage across the diodes the ratio of the diode areas has been fixed at 8.

SPICE3B.1 program, which is used for the simulation of the circuit does not have the temperature variation implemented for a GaAs MESFET. Hence, MESFET I-V curves obtained experimentally [Joseph Mun, 1988] at 25 °C and 125 °C have been taken as the reference and a spice model obtained for the MESFET which fits the curves. The SPICE simulation results are shown in the fig 5.1. The MESFET model parameters thus obtained have been used in the sensor circuit for all the transistors in order to simulate the circuit at 125 °C.

Fig 5.2 shows the temperature sensing diode pair. The number shown against each MESFET is its gate width in microns. The gate length which is defined by the process, is common and critical for all the MESFETs and is equal to 1 micron. The numbers shown against the diodes give the diode areas in square microns. From the SPICE results shown in fig 5.3, the diode pair generates a differential voltge of 8 mV. When simulated at 125 °C the diode pair generates 50mV of differential voltage, as can be seen from the SPICE results (fig 5.4).

The differential voltage obtained across the diodes is amplified by using a differential amplifier circuit whose schematic is shown in fig 5.5.

```
i-v characteristics of gaas mesfet at 25 C

vdd 1 0
vgs 2 0 0.5v
vids 3 0 0v

z1 1 2 3 dfet

.model dfet nmf(vto=-1.0 beta=.00037
+rd=10 rs=10 pb=.75 alpha=1.5 b=0.3)

.width out=80
.option node

.dc vdd 0.0 2.5 0.05

.print dc v(1) v(2) i(vids)
.plot dc v(1) v(2) i(vids)

.end
```

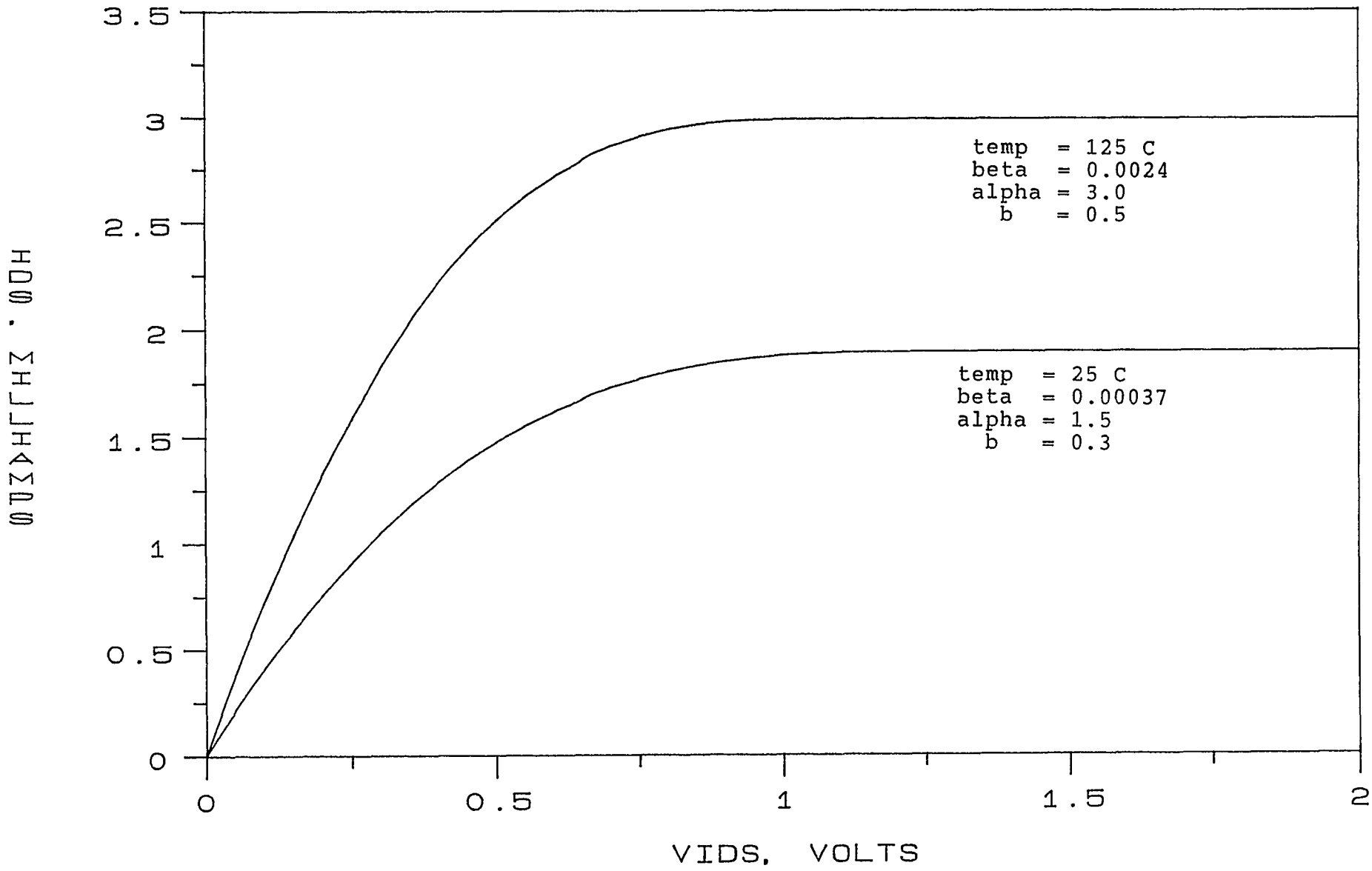
SPICE INPUT FILE FOR THE SIMULATION OF
GaAs MESFET CHARACTERISTICS AT 25 C

FIG 5.1(a)

```
i-v characteristics of gaas mesfet at 125 C

vdd 1 0
vgs 2 0 0.5v
vids 3 0 0v

z1 1 2 3 dfet

.model dfet nmf(vto=-1.0 beta=.0024 b=0.5
+rd=10 rs=10 pb=.75 alpha=3.0)

.width out=80
.option node

.dc vdd 0.0 2.5 0.05

.print dc v(1) v(2) i(vids)
.plot dc v(1) v(2) i(vids)

.end
```

SPICE INPUT FILE FOR THE SIMULATION OF
GaAs MESFET CHARACTERISTICS AT 125 C

FIG 5.1(b)



GaAs MESFET CHARACTERISTICS AT 25 C & 125 C

FIG 5.1c [AFTER MUN, 1988]

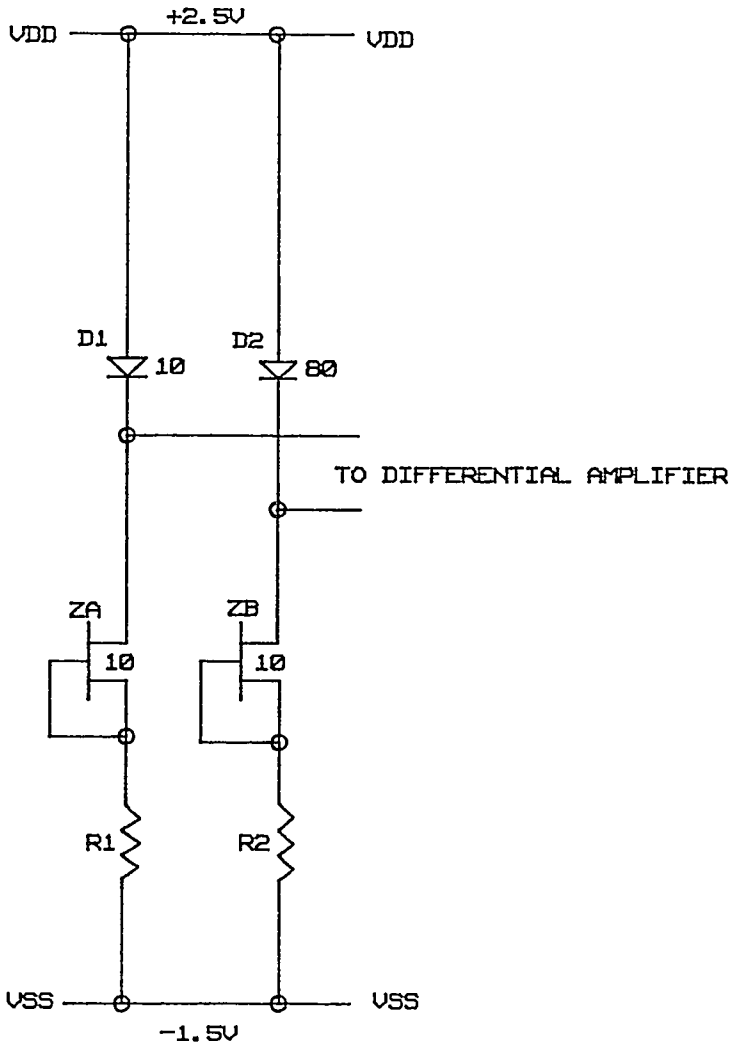


FIG 5.2
TEMPERATURE SENSING DIODE CIRCUIT

```
temperature sensing diodes at 25 C

vdd 1 0 2.5v
vss 6 0 -1.5v

z1 2 4 4 dfet area=10
z2 3 5 5 dfet area=10

d1 1 2 gaad area=10
d2 1 3 gaad1 area=80

r1 4 6 10k
r2 5 6 10k

.model dfet nmf(vto=-1.0v beta=1e-6 pb=0.75
+alpha=1.5 b=0.5 lambda=0.3 rd=10 rs=10)
.model gaad d(is=0.803e-21 vj=0.9 m=0.5 rs=10)
.model gaad1 d(is=0.137e-21 vj=0.9 m=0.5 rs=10)

.width out=80
.op
.option node
.end
```

SPICE INPUT FILE FOR THE SIMULATION OF
TEMPERATURE SENSING DIODE CIRCUIT AT 25 C

FIG 5.3(a)

```
Title: temperature sensing diodes at 25 C
Date: Sun Nov 27 17:08:14 EST 1988
Plotname: DC Operating point analysis.
Flags: real
No. Variables: 15
No. Points: 1
Variables: 0 ground voltage
 1 v(1) voltage
 2 v(2) voltage
 3 v(3) voltage
 4 v(4) voltage
 5 v(5) voltage
 6 v(6) voltage
 7 d1#internal voltage
 8 d2#internal voltage
 9 vdd#branch current
 10 vss#branch current
 11 z1#internal#drain voltage
 12 z1#internal#source voltage
 13 z2#internal#drain voltage
 14 z2#internal#source voltage
Values:
 0       0.000000000000000e+00
         2.500000000000000e+00
         1.595009107772528e+00 --- V(D1)
         1.603033391677879e+00 --- V(D2)
         -1.373957129907501e+00
         -1.373799798031932e+00
         -1.500000000000000e+00
         2.499987395712991e+00
         2.499998422497475e+00
         -2.522430720574752e-05
         2.522430720605663e-05
         1.594996503485518e+00
         -1.373944525623561e+00
         1.603020771657682e+00
         -1.373787178014812e+00
```

The differential voltage across diodes = (1.603-1.595) V = 8 mV

SPICE OUTPUT DATA FOR THE SIMULATION OF TEMPERATURE SENSING DIODE CIRCUIT AT 25 C

FIG 5.3(b)

```
temperature sensing diodes at 125 C

vdd 1 0 2.5v
vss 6 0 -1.5v

z1 2 4 4 dfet area=10
z2 3 5 5 dfet area=10

d1 1 2 gaad area=10
d2 1 3 gaad1 area=80

r1 4 6 11.3k
r2 5 6 11.3k

.model dfet nmf(vto=-1.0v beta=1.7e-6 b=0.4
+pb=0.8 alpha=3.0 rd=11.3 rs=11.3)
.model gaad d(is=1.62e-17 vj=0.94 m=0.5 rs=11.3)
.model gaad1 d(is=1.4e-17 vj=0.94 m=0.5 rs=11.3)

.width out=80
.op
.option node
.end
```

SPICE INPUT FILE FOR THE SIMULATION OF
TEMPERATURE SENSING DIODE CIRCUIT AT 125 C

FIG 5.4(a)

```
Title: temperature sensing diodes at 125 C
Date: Sun Nov 27 17:10:06 EST 1988
Plotname: DC Operating point analysis.
Flags: real
No. Variables: 15
No. Points: 1
Variables: 0 ground voltage
 1 v(1) voltage
 2 v(2) voltage
 3 v(3) voltage
 4 v(4) voltage
 5 v(5) voltage
 6 v(6) voltage
 7 d1#internal voltage
 8 d2#internal voltage
 9 vdd#branch current
 10 vss#branch current
 11 z1#internal#drain voltage
 12 z1#internal#source voltage
 13 z2#internal#drain voltage
 14 z2#internal#source voltage
Values:
 0       0.000000000000000e+00
         2.500000000000000e+00
         1.851445779611342e+00 --- V(D1)
         1.901466301539844e+00 --- V(D2)
         -1.357946279115859e+00
         -1.357946278550481e+00
         -1.500000000000000e+00
         2.499985794627912e+00
         2.499998224328482e+00
         -2.514225153390910e-05
         2.514225153395224e-05
         1.851431574239254e+00
         -1.357932073747510e+00
         1.901452096167700e+00
         -1.357932073182132e+00
```

The differential voltage across diodes = (1.851-1.901) V = 50 mV

SPICE OUTPUT DATA FOR THE SIMULATION OF TEMPERATURE SENSING DIODE CIRCUIT AT 25 C

FIG 5.4(b)

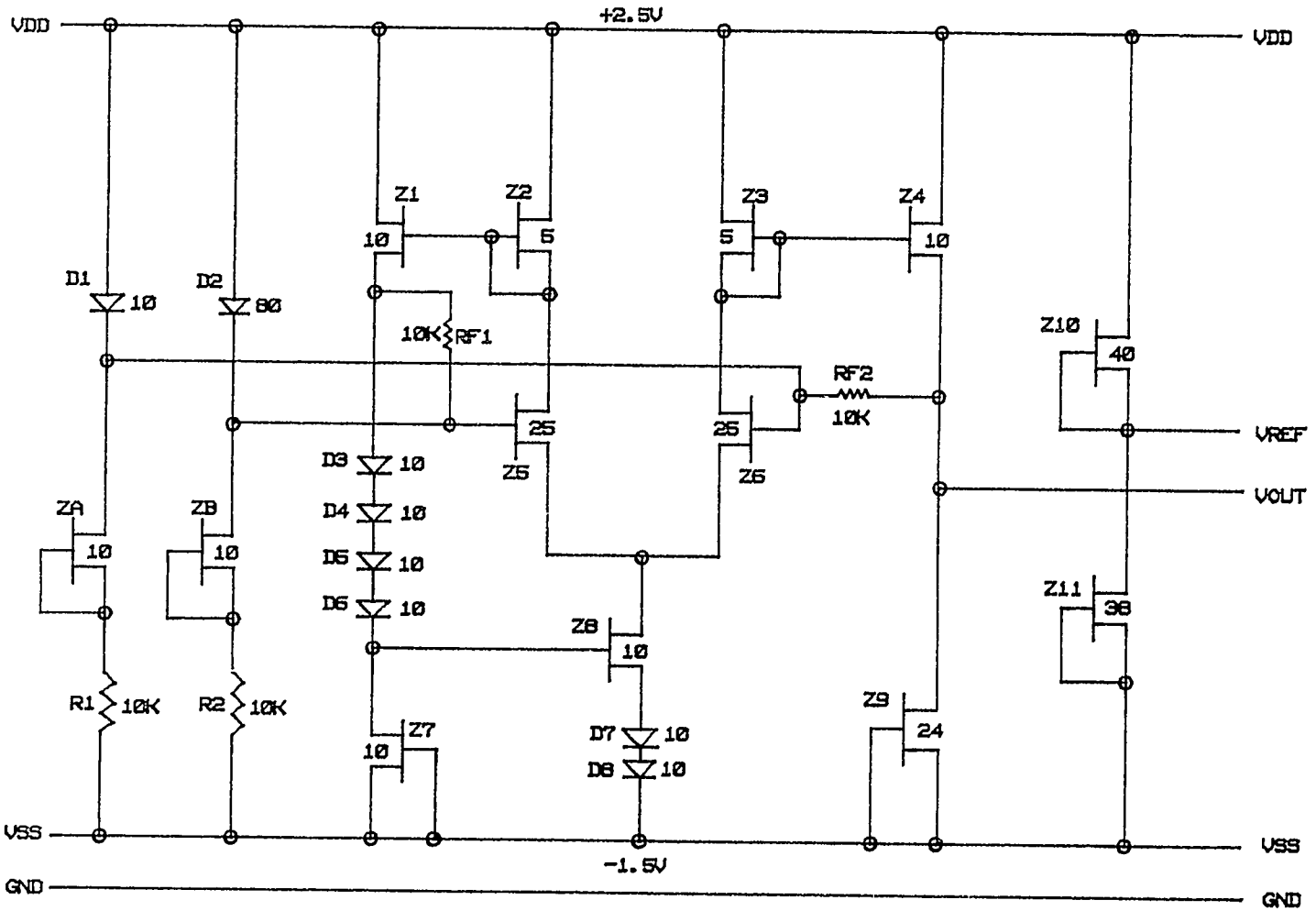


FIG 5.5

TEMPERATURE SENSING DIODES WITH DIFFERENTIAL AMPLIFIER & VOLTAGE REFERENCE

The amplifier demonstrated a mean offset of 2.6mV. When 8 mV was fed to the differential amplifier, it demonstrated an open loop gain of 44 db (the output of the amplifier being 1.273 V) and a closed loop gain of 32 db (with the resistive feedback). The SPICE results are shown in fig 5.6. At 125 °C, the diode pair generated 50 mV which was amplified to 1.847 V, with a gain of 31.35 db. The simulation results can be seen in fig 5.7.

Finally, the aim of the sensor circuit is to give out a message, when it senses a temperature of 125 °C. In order to achieve this, a NAND latch has been designed whose schematic is shown in the fig 5.8. This latch has two inputs which are connected to the output of the differential amplifier and a voltage reference whose value is fixed at 1.838 V. The output of the NAND latch is low, at 0.648 V, until the differential amplifier output reaches 1.847 V. At this instance, the differential amplifier is sensing a temperature of 125 °C and the NAND latch output goes high, to 1.933 V. This is evident from the SPICE results shown in the figs. 5.9 and 5.10. Thus, the temperature sensor output switches from a low value of 0.648 V to a high value of 1.933 V when the sensing temperature reaches 125 °C. Fig 5.11 shows the schematic of the complete sensor circuit.

The output of the differential amplifier changes from 1.273 V at 25 °C to 1.847 V at 125 °C. That is, there is a 5.74 mV increase per degree centigrade rise in the temperature. When the diode junction potential changes by ±5% there is a corresponding change of ±6.6 mV at the output of the differential amplifier which is equivalent to a change of ±1.15 °C. When V_T of the MESFET changes by +5%, there is an increase of 2.85 mV in the output of the amplifier i.e., a temperature rise of 0.5 °C.

```
temp sensing diodes with diff amp & reference
voltage (25 C)

vdd 1 0 2.5v
vss 14 0 -1.5v

d1 1 2 gaad area=10
d2 1 3 gaad1 area=80

za 2 4 4 dfet1 area=10
zb 3 5 5 dfet1 area=10

r1 4 14 10k
r2 5 14 10k

.model gaad d(is=0.803e-21 vj=0.9 m=0.5 rs=10)
.model gaad1 d(is=0.137e-21 vj=0.9 m=0.5 rs=10)
.model dfet1 nmf(vto=-1.0 beta=1e-6 b=0.5
+pb=0.75 alpha=1.5 rd=10 rs=10 lambda=0.3)

z1 1 6 9 dfet area=10
z2 1 6 6 dfet area=5
z3 1 7 7 dfet area=5
z4 1 7 20 dfet area=10
z5 6 3 8 dfet area=25
z6 7 2 8 dfet area=25
z7 13 14 14 dfet area=10
z8 8 13 16 dfet area=10
z9 20 14 14 dfet area=24

z10 1 21 21 dfet area=40
z11 21 14 14 fet1 area=38

.model dfet nmf(vto=-1.0 beta=0.00037 pb=0.75
+alpha=1.5 b=0.3 rd=10 rs=10)
.model fet1 nmf(vto=-1.0 beta=0.00037043 pb=0.75
+alpha=1.5 b=0.3 rd=10 rs=10)

d3 9 10 gad area=10
d4 10 11 gad area=10
d5 11 12 gad area=10
d6 12 13 gad  area=10
d7 16 15 gad area=10
d8 15 14 gad area=10

.model gad d(vj=0.9 is=4e-15 m=0.5)
.model gad1 d(vj=0.88 is=5.25e-15 m=0.5)

.width out=80
.option node
.op
.end
```

SPICE INPUT FILE FOR THE SIMULATION
OF TEMP SENSING DIODES WITH DIFF AMPLIFIER
AND REFERENCE VOLTAGE CIRCUIT AT 25 C

FIG 5.6(a)

```
Title: temp sensing diodes with diff amp & voltage ref (25 C)
Date: Thu Jan  5 16:28:49 EST 1989
Plotname: DC Operating point analysis.
Flags: real
No. Variables: 49
No. Points: 1
Variables: 0 ground voltage
 1 v(1) voltage
 2 v(2) voltage
 3 v(3) voltage
 4 v(4) voltage
 5 v(5) voltage
 6 v(6) voltage
 7 v(7) voltage
 8 v(8) voltage                    1.224877739379456e+00
 9 v(9) voltage                    5.849641508509211e-01
 10 v(10) voltage                  -5.494943767761341e-02
 11 v(11) voltage                  -6.948630262061479e-01
 12 v(12) voltage                  -1.500000000000000e+00
 13 v(13) voltage                  -8.804908032619473e-01
 14 v(14) voltage                  -2.609816065238947e-01
 15 v(15) voltage                  1.273874493403476e+00    VOUT
 16 v(16) voltage                  1.227146735639461e+00
 17 v(20) voltage                  2.499958432071663e+00
 18 v(21) voltage                  2.499999991010576e+00
 19 d1#internal voltage            -2.082966790534079e-02
 20 d2#internal voltage            2.082966790534072e-02
 21 vdd#branch current             2.497763522217051e+00
 22 vss#branch current             1.867027805693099e+00
 23 z1#internal#drain voltage      2.498259302170559e+00
 24 z1#internal#source voltage     1.955122801855822e+00
 25 z2#internal#drain voltage      2.498084830212548e+00
 26 z2#internal#source voltage     1.872894424957810e+00
 27 z3#internal#drain voltage      2.494050074911241e+00
 28 z3#internal#source voltage     1.280642046673851e+00
 29 z4#internal#drain voltage      1.953033964462557e+00
 30 z4#internal#source voltage     1.847102873274646e+00
 31 z5#internal#drain voltage      1.870923272486879e+00
 32 z5#internal#source voltage     1.846810716394360e+00
 33 z6#internal#drain voltage      -6.970866938310878e-01
 34 z6#internal#source voltage     -1.497776332375973e+00
 35 z7#internal#drain voltage      1.845744428087193e+00
 36 z7#internal#source voltage     -2.599713009043120e-01
 37 z8#internal#drain voltage      1.271042586118648e+00
 38 z8#internal#source voltage     -1.497168092716438e+00
 39 z9#internal#drain voltage      2.497306577154635e+00
 40 z9#internal#source voltage     1.229840158484397e+00
 41 z10#internal#drain voltage     1.224311553696972e+00
 42 z10#internal#source voltage    -1.497164818058339e+00
 43 z11#internal#drain voltage     1.564104081833557e+00
 44 z11#internal#source voltage    -1.374550294171247e+00
 45 za#internal#drain voltage      1.736676812380509e+00
 46 za#internal#source voltage     -1.371166322331588e+00
 47 zb#internal#drain voltage
 48 zb#internal#source voltage
Values:
 0      0.000000000000000e+00
        2.500000000000000e+00
        1.564116625549769e+00
        1.736689694460068e+00
        -1.374562837884420e+00
        -1.371179204407939e+00
        1.953382104027581e+00
        1.870979255171724e+00
        1.846754733709951e+00
        1.864791327907990e+00
```

SPICE OUTPUT DATA FOR THE SIMULATION OF TEMP SENSING DIODES WITH DIFF AMPLIFIER AND REFERENCE VOLTAGE CIRCUIT AT 25 C

FIG 5.6(b)

```
temp sensing diodes with diff amp & reference
voltage (125 C)

vdd 1 0 2.5v
vss 14 0 -1.5v

d1 1 2 gaad area=10
d2 1 3 gaad1 area=80

za 2 4 4 dfet1 area=10
zb 3 5 5 dfet1 area=10

r1 4 14 11.3k
r2 5 14 11.3k

rf1 9 3 11.3k
rf2 20 2 11.3k

.model gaad d(is=1.62e-17 vj=0.94 m=0.5 rs=11.3)
.model gaad1 d(is=1.4e-17 vj=0.94 m=0.5 rs=11.3)
.model dfet1 nmf(vto=-1.0 beta=1.76e-6 b=0.4
+pb=0.8 alpha=3.0 rd=11.3 rs=11.3)

z1 1 6 9 dfet area=10
z2 1 6 6 dfet area=5
z3 1 7 7 dfet area=5
z4 1 7 20 dfet area=10
z5 6 3 8 dfet area=25
z6 7 2 8 dfet area=25
z7 13 14 14 dfet area=10
z8 8 13 16 dfet area=10
z9 20 14 14 dfet3 area=24

z10 1 21 21 dfet area=40
z11 21 14 14 dfet2 area=38

.model dfet nmf(vto=-1.0 beta=0.0096 pb=0.75
+alpha=3.0 b=0.4 rd=11.3 rs=11.3)
.model dfet2 nmf(vto=-1.0 beta=0.009158 pb=0.75
+alpha=3.0 b=0.4 rd=11.3 rs=11.3)
.model dfet3 nmf(vto=-1.0 beta=0.006686 pb=0.75
+alpha=3.0 b=0.4 rd=11.3 rs=11.3)

d3 9 10 gad area=10
d4 10 11 gad area=10
d5 11 12 gad area=10
d6 12 13 gad  area=10
d7 16 15 gad area=10
d8 15 14 gad area=10

.model gad d(vj=0.94 is=2.8e-15 m=0.5)

.width out=80
.option node
.op
.end
```

SPICE INPUT FILE FOR THE SIMULATION
OF TEMP SENSING DIODES WITH DIFF AMPLIFIER
AND REFERENCE VOLTAGE CIRCUIT AT 125 C
FIG 5.7(a)

```
Title: temp sensing diodes with diff amp and voltage ref (175 C)
Date: Thu Jan  5 16:33:26 EST 1989
Plotname: DC Operating point analysis.
Flags: real
No. Variables: 49
No. Points: 1
Variables: 0 ground voltage
 1 v(1) voltage
 2 v(2) voltage
 3 v(3) voltage
 4 v(4) voltage
 5 v(5) voltage
 6 v(6) voltage
 7 v(7) voltage
 8 v(8) voltage                      1.394317939683932e+00
 9 v(9) voltage                      6.615864664167457e-01
 10 v(10) voltage                    -7.114500685044072e-02
 11 v(11) voltage                    -8.038764801176271e-01
 12 v(12) voltage                    -1.500000000000000e+00
 13 v(13) voltage                    -8.158319687334862e-01
 14 v(14) voltage                    -1.316639374669724e-01
 15 v(15) voltage                    1.847447050175203e+00→ VOUT
 16 v(16) voltage                    1.838023818128021e+00→ VREF
 17 v(20) voltage                    2.499985455763694e+00
 18 v(21) voltage                    2.499999941376526e+00
 19 d1#internal voltage              -3.911242469993840e-01
 20 d2#internal voltage              3.911242469993836e-01
 21 vdd#branch current               2.436338467247331e+00
 22 vss#branch current               2.190710946931074e+00
 23 z1#internal#drain voltage        2.489550767862689e+00
 24 z1#internal#source voltage       2.441511432253442e+00
 25 z2#internal#drain voltage        2.490958097223768e+00
 26 z2#internal#source voltage       2.449777744785781e+00
 27 z3#internal#drain voltage        2.381310762620323e+00
 28 z3#internal#source voltage       1.966146808791560e+00
 29 z4#internal#drain voltage        2.428972354179878e+00
 30 z4#internal#source voltage       2.405219215360962e+00
 31 z5#internal#drain voltage        2.438931669949238e+00
 32 z5#internal#source voltage       2.404933541484859e+00
 33 z6#internal#drain voltage        -8.675242777192708e-01
 34 z6#internal#source voltage       -1.436352202399359e+00
 35 z7#internal#drain voltage        2.393394324435608e+00
 36 z7#internal#source voltage       -1.219288924821633e-01
 37 z8#internal#drain voltage        1.797988676224190e+00
 38 z8#internal#source voltage       -1.450541626050772e+00
 39 z9#internal#drain voltage        2.437535237925978e+00
 40 z9#internal#source voltage       1.900488580201639e+00
 41 z10#internal#drain voltage       1.772271436997471e+00
 42 z10#internal#source voltage      -1.434247618870660e+00
 43 z11#internal#drain voltage       1.850821505541225e+00
 44 z11#internal#source voltage      -1.357932073754545e+00
 45 za#internal#drain voltage        1.989671378369099e+00
 46 za#internal#source voltage       -1.357932072185660e+00
 47 zb#internal#drain voltage
 48 zb#internal#source voltage
Values:
 0      0.000000000000000e+00
        2.500000000000000e+00
        1.850835710913313e+00
        1.989685583741344e+00
        -1.357946279122893e+00
        -1.357946277554008e+00
        2.431062200116426e+00
        2.440735842009812e+00
        2.403129369425027e+00
        2.127049412951119e+00
```

SPICE OUTPUT DATA FOR THE SIMULATION OF TEMP SENSING DIODES WITH DIFF AMPLIFIER AND REFERENCE VOLTAGE CIRCUIT AT 125 C

FIG 5.7(b)

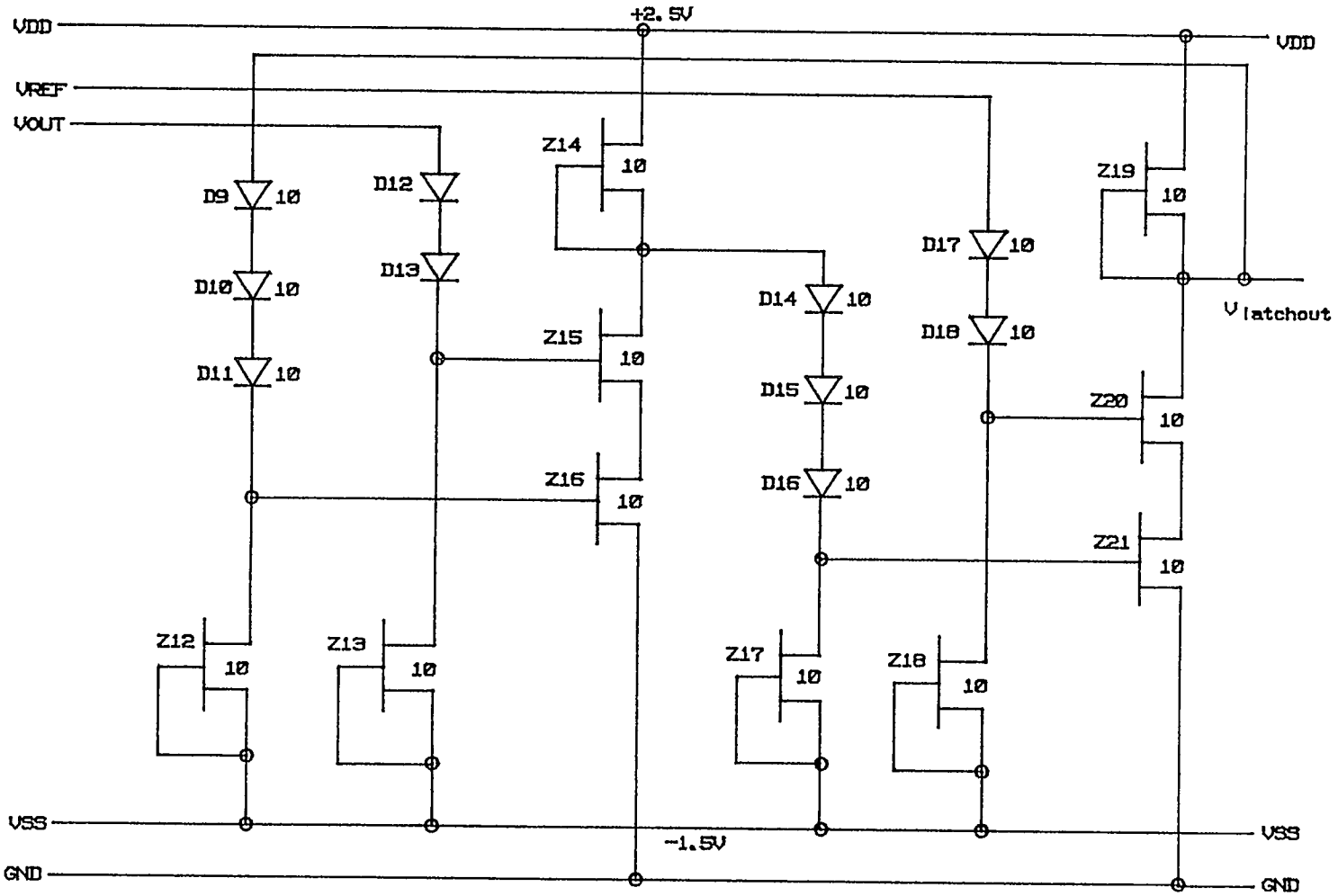


FIG 5.8

NAND LATCH CIRCUIT

```
nand latch analysis

vdd 7 0 2.5
vss 6 0 -1.5
vin1 21 0 1.838v
vin2 1 0 1.84v

c1 8 0 60ff
c2 30 0 60ff

d2 30 3 mod1 10
d3 3 4 mod1 10
d4 4 5 mod1 10
d5 1 22 mod1 10
d6 22 23 mod1 10

d7 21 28 mod1 10
d8 28 29 mod1 10
d9 8 25 mod1 10
d10 25 26 mod1 10
d11 26 27 mod1 10

.model mod1 d(is=2e-10 vj=0.94 m=0.5 rs=22.6)

z1 5 6 6 dmesfet1 area=10
z5 23 6 6 dmesfet1 area=10
z2 7 8 8 dmesfet2 area=10
z4 8 23 24 dmesfet3 area=10
z3 24 5 0 dmesfet3 area=10

z6 27 6 6 dmesfet1 area=10
z7 29 6 6 dmesfet1 area=10
z8 7 30 30 dmesfet2 area=10
z9 30 29 31 dmesfet3 area=10
z10 31 27 0 dmesfet3 area=10

.model dmesfet1 nmf(vto=-1.0v beta=.002
+pb=0.75 alpha=3.0 b=0.5 rd=11.3 rs=11.3)
.model dmesfet2 nmf(vto=-1.0v beta=.0024
+pb=0.75 alpha=3.0 b=0.5 rd=11.3 rs=11.3)
.model dmesfet3 nmf(vto=-1.0v beta=.0028
+pb=0.75 alpha=3.0 b=0.5 rd=11.3 rs=11.3)

.options node
.width out=80
.op
.end
```

SPICE INPUT FILE FOR THE SIMULATION OF
NAND LATCH CIRCUIT WHEN THE OUTPUT IS LOW

FIG 5.9(a)

```
Title: nand latch analysis
Date: Tue Dec  6 10:16:46 EST 1988
Plotname: DC Operating point analysis.
Flags: real
No. Variables: 53
No. Points: 1
Variables: 0 ground voltage
 1 v(1) voltage
 2 v(3) voltage
 3 v(4) voltage
 4 v(5) voltage
 5 v(6) voltage
 6 v(7) voltage                          2.500000000000000e+00
 7 v(8) voltage                          6.480053002545303e-01
 8 v(21) voltage                         1.838000000000000e+00
 9 v(22) voltage                         1.404846037223225e+00
 10 v(23) voltage                        9.696920744464508e-01
 11 v(24) voltage                        6.128681601494933e-01
 12 v(25) voltage                        2.131973(00705324e-01
 13 v(26) voltage                        -2.216107001134656e-01
 14 v(27) voltage                        -6.564187002974635e-01
 15 v(28) voltage                        1.402846072780929e+00
 16 v(29) voltage                        9.676921455618583e-01
 17 v(30) voltage                        6.479982832161129e-01 → V(latchout)
 18 v(31) voltage                        6.127925412929428e-01     - low
 19 d2#internal voltage                  6.187837919342790e-01
 20 d3#internal voltage                  1.839758302330186e-01
 21 d4#internal voltage                  -2.508321314682418e-01
 22 d5#internal voltage                  1.810601714218189e+00
 23 d6#internal voltage                  1.375447751441415e+00
 24 d7#internal voltage                  1.808601733133999e+00
 25 d8#internal voltage                  1.373447805914928e+00
 26 d9#internal voltage                  6.187907885610461e-01
 27 d10#internal voltage                 1.839827883770481e-01
 28 d11#internal voltage                 -2.508252118069498e-01
 29 vdd#branch current                   -3.106821904490856e-02
 30 vin1#branch current                  -1.300808268407131e-02
 31 vin2#branch current                  -1.300809105389846e-02
 32 vss#branch current                   5.186949172098750e-02
 33 z1#internal#drain voltage            -6.710328475309873e-01
 34 z1#internal#source voltage           -1.485392754357796e+00
 35 z2#internal#drain voltage            2.482446456239627e+00
 36 z2#internal#source voltage           6.655588440126422e-01
 37 z3#internal#drain voltage            6.099217414210844e-01
 38 z3#internal#source voltage           2.946418726006831e-03
 39 z4#internal#drain voltage            6.450590123408991e-01
 40 z4#internal#source voltage           6.158145788779021e-01
 41 z5#internal#drain voltage            9.549930623703233e-01
 42 z5#internal#source voltage           -1.485300987926825e+00
 43 z6#internal#drain voltage            -6.710259561466076e-01
 44 z6#internal#source voltage           -1.485392744151971e+00
 45 z7#internal#drain voltage            9.529931334857330e-01
 46 z7#internal#source voltage           -1.485300987926825e+00
 47 z8#internal#drain voltage            2.482446456239627e+00
 48 z8#internal#source voltage           6.655518269742248e-01
 49 z9#internal#drain voltage            6.450519850966566e-01
 50 z9#internal#source voltage           6.157389607692744e-01
 51 z10#internal#drain voltage           6.098461218166112e-01
 52 z10#internal#source voltage          2.946419473929603e-03
Values:
 0      0.000000000000000e+00
        1.840000000000000e+00
        2.131903215148525e-01
        -2.216176401864079e-01
        -6.564256018876683e-01
        -1.500000000000000e+00
```

SPICE OUTPUT DATA FOR THE SIMULATION OF NAND LATCH CIRCUIT WHEN THE OUTPUT IS LOW

FIG 5.9(b)

```
nand latch analysis

vdd 7 0 2.5
vss 6 0 -1.5
vin1 21 0 1.838v
vin2 1 0 1.847v

c1 8 0 60ff
c2 30 0 60ff

d2 30 3 mod1 10
d3 3 4 mod1 10
d4 4 5 mod1 10
d5 1 22 mod1 10
d6 22 23 mod1 10

d7 21 28 mod1 10
d8 28 29 mod1 10
d9 8 25 mod1 10
d10 25 26 mod1 10
d11 26 27 mod1 10

.model mod1 d(is=2e-10 vj=0.94 m=0.5 rs=22.6)

z1 5 6 6 dmesfet1 area=10
z5 23 6 6 dmesfet1 area=10
z2 7 8 8 dmesfet2 area=10
z4 8 23 24 dmesfet3 area=10
z3 24 5 0 dmesfet3 area=10

z6 27 6 6 dmesfet1 area=10
z7 29 6 6 dmesfet1 area=10
z8 7 30 30 dmesfet2 area=10
z9 30 29 31 dmesfet3 area=10
z10 31 27 0 dmesfet3 area=10

.model dmesfet1 nmf(vto=-1.0v beta=.002
+pb=0.75 alpha=3.0 b=0.5 rd=11.3 rs=11.3)
.model dmesfet2 nmf(vto=-1.0v beta=.0024
+pb=0.75 alpha=3.0 b=0.5 rd=11.3 rs=11.3)
.model dmesfet3 nmf(vto=-1.0v beta=.0028
+pb=0.75 alpha=3.0 b=0.5 rd=11.3 rs=11.3)

.options node
.width out=80
.op
.end
```

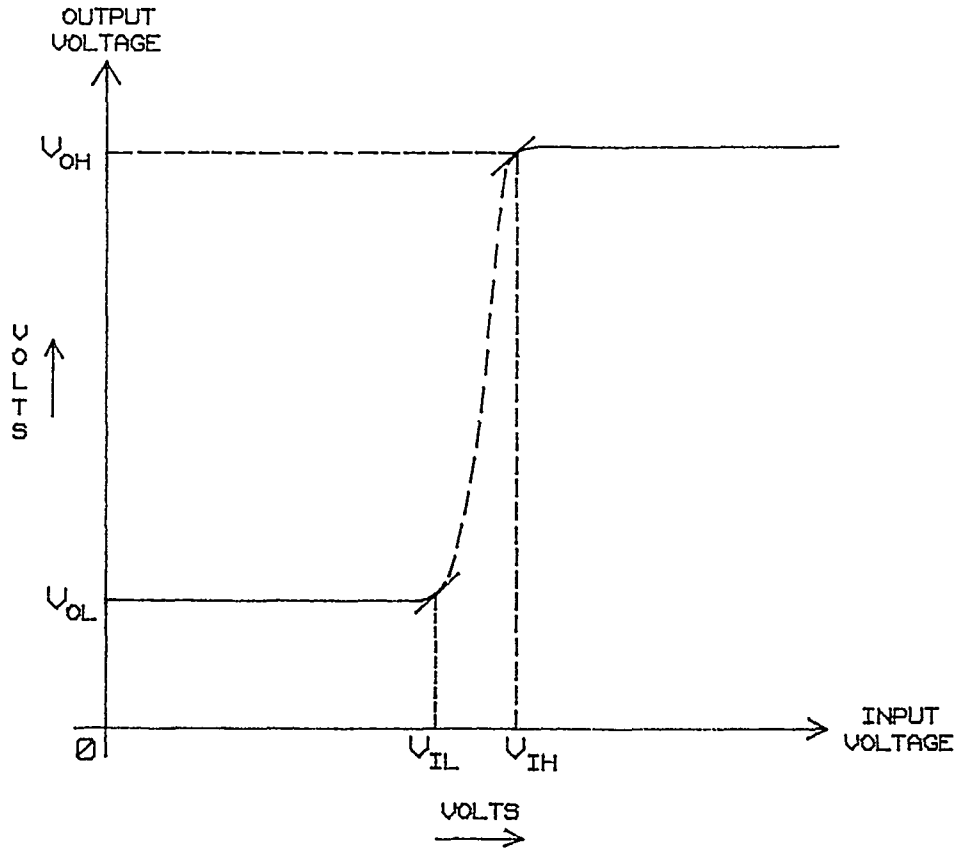
SPICE INPUT FILE FOR THE SIMULATION OF
NAND LATCH CIRCUIT WHEN THE OUTPUT GOES HIGH

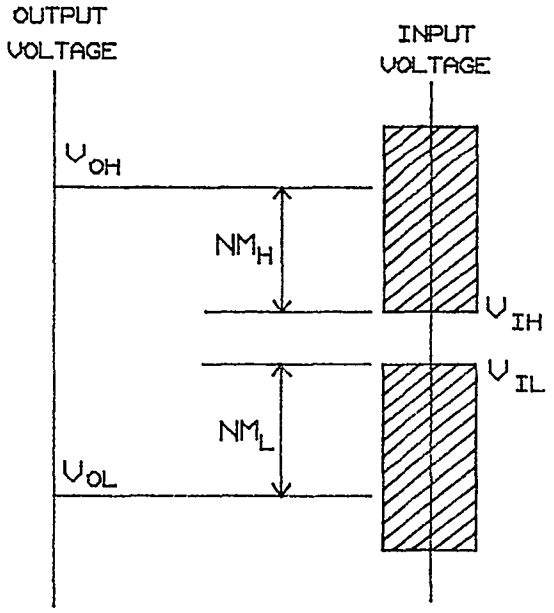
FIG 5.10(a)

```
Title: nand latch analysis
Date: Tue Dec  6 10:33:39 EST 1988
Plotname: DC Operating point analysis.
Flags: real
No. Variables: 53
No. Points: 1
Variables: 0 ground voltage
 1 v(1) voltage                          2.500000000000000e+00
 2 v(3) voltage                          2.816266850378385e-01
 3 v(4) voltage                          1.838000000000000e+00
 4 v(5) voltage                          1.365171061672513e+00
 5 v(6) voltage                          8.843421233450255e-01
 6 v(7) voltage                          2.079387192186948e-01
 7 v(8) voltage                          -1.454217749553299e-01
 8 v(21) voltage                         -5.724702349484984e-01
 9 v(22) voltage                         -9.995186949416668e-01
 10 v(23) voltage                        1.402846529040867e+00
 11 v(24) voltage                        9.676930580817351e-01
 12 v(25) voltage                        1.933734065518869e+00→ V(latchout)
 13 v(26) voltage                        1.933666194764097e+00    - high
 14 v(27) voltage                        1.902073279286372e+00
 15 v(28) voltage                        1.462739180290788e+00
 16 v(29) voltage                        1.023405081295205e+00
 17 v(30) voltage                        1.788346605999296e+00
 18 v(31) voltage                        1.307517667671809e+00
 19 d2#internal voltage                  1.808601975852568e+00
 20 d3#internal voltage                  1.373448504893435e+00
 21 d4#internal voltage                  2.563880509901165e-01
 22 d5#internal voltage                  -1.706604090030519e-01
 23 d6#internal voltage                  -5.977088689962204e-01
 24 d7#internal voltage                  -2.954331346056291e-02
 25 d8#internal voltage                  -1.300797528647449e-02
 26 d9#internal voltage                  -2.551035132774499e-02
 27 d10#internal voltage                 5.019146305877431e-02
 28 d11#internal voltage                 6.010327564563902e-01
 29 vdd#branch current                   -1.485300987926825e+00
 30 vin1#branch current                  2.482446456239213e+00
 31 vin2#branch current                  2.991802287959504e-01
 32 vss#branch current                   1.888768075574479e-01
 33 z1#internal#drain voltage            2.019329270176775e-02
 34 z1#internal#source voltage           2.766924583009122e-01
 35 z2#internal#drain voltage            2.270006308799418e-01
 36 z2#internal#source voltage           8.696431112689943e-01
 37 z3#internal#drain voltage            -1.485300987926825e+00
 38 z3#internal#source voltage           -1.012138011970198e+00
 39 z4#internal#drain voltage            -1.487380682972191e+00
 40 z4#internal#source voltage           9.529940460056098e-01
 41 z5#internal#drain voltage            -1.485300987926825e+00
 42 z5#internal#source voltage           2.484169599550351e+00
 43 z6#internal#drain voltage            1.949564465967713e+00
 44 z6#internal#source voltage           1.933734058185468e+00
 45 z7#internal#drain voltage            1.933666202095088e+00
 46 z7#internal#source voltage           1.933666187433106e+00
 47 z8#internal#drain voltage            7.326321290371436e-09
 48 z8#internal#source voltage
 49 z9#internal#drain voltage
 50 z9#internal#source voltage
 51 z10#internal#drain voltage
 52 z10#internal#source voltage
Values:
 0      0.000000000000000e+00
        1.847000000000000e+00
        1.494399966523285e+00
        1.055065867527701e+00
        6.157317685321178e-01
        -1.500000000000000e+00
```

SPICE OUTPUT DATA FOR THE SIMULATION OF NAND LATCH CIRCUIT WHEN THE OUTPUT GOES HIGH

FIG 5.10(b)





$$NM_H = V_{OH} - V_{IH}$$
$$= 1.93\ V - 1.847\ V$$
$$= 0.083\ V$$

$$NM_L = V_{IL} - V_{OL}$$
$$= 1.84\ V - 0.648\ V$$
$$= 1.19\ V$$

FIG 5.10c
NAND LATCH NOISE MARGINS

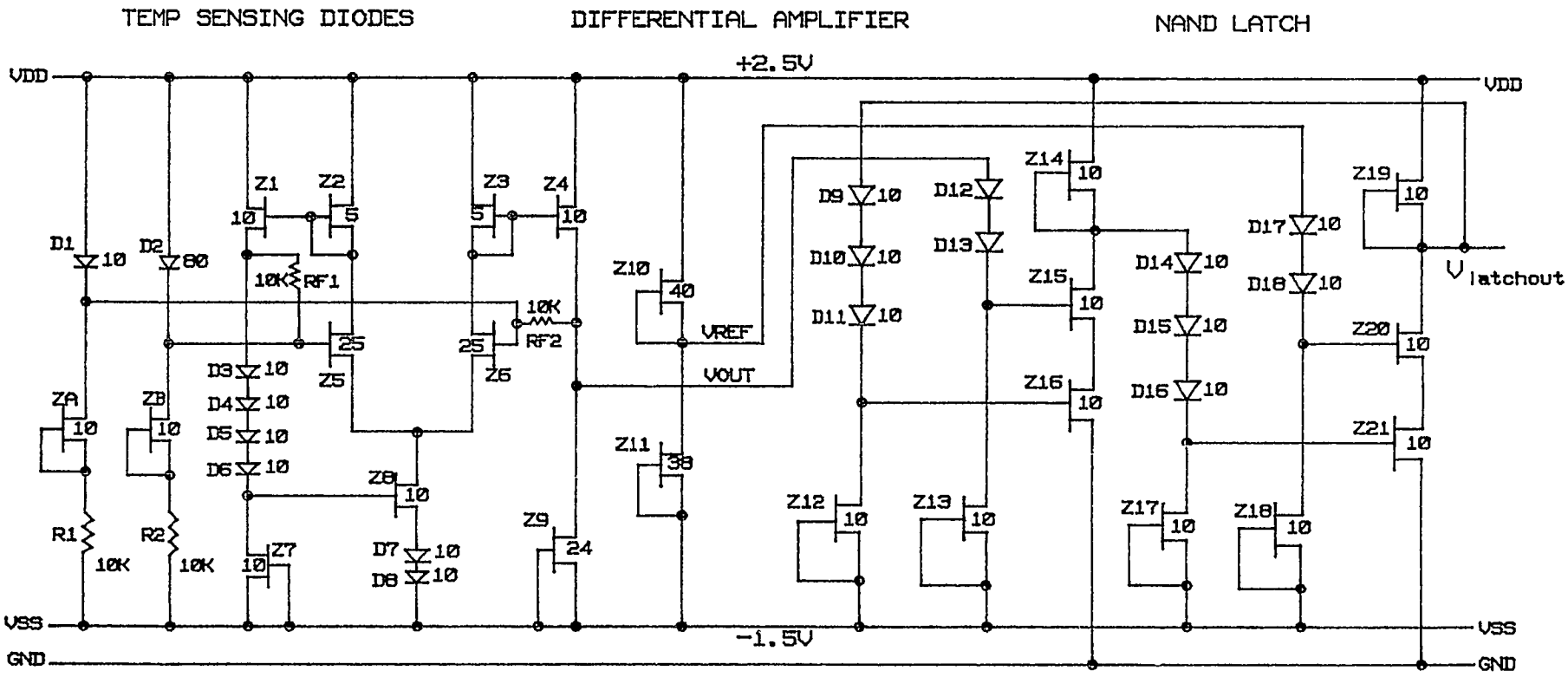


FIG 5.11

TEMPERATURE SENSOR CIRCUIT

PARAMETER	VARIATION	ERROR IN TEMP
MESFET THRESHOLD VOLTAGE [V_T]	±5%	1.0 °C
DIODE JUNCTION POTENTIAL [ϕ_{Bn}]	±5%	2.3 °C
POWER SUPPLY VOLTAGE [V_{DD}]	±5%	0.5 °C
MESFET TRANS-CONDUCTANCE [BETA]	±10%	1.9 °C
RESISTOR LAYOUT MISMATCH [R_m]	±5%	2.0 °C
	WORST CASE ERROR =	7.7 °C

EFFECTS OF PARAMETER VARIATIONS
ON THE SENSING TEMPERATURE
TABLE 5.1

A 5% decrease in the MESFET threshold voltage resulted in a 2.85 mV decrease in the output of the amplifier which corresponds to a 0.5 °C decrease in the temperature. For a ±10% variation in the MESFET transconductance value, the temperature error was ±0.95 °C. A 5% error in the resistor layout mismatch resulted in a temperature error of 2.0 °C. When the power supply voltage V_{dd} was varied by ±5%, the output of the differential amplifier changed by ±1.435 mV, which corresponds to a ±0.25 °C error in the sensing temperature. Hence, the worst case error in the output of the differential amplifier due to cumulative effect of the above mentioned tolerances is 7.7 °C. Also, the NAND latch output doesn't flip for a ±10% change in the diode junction potential and ±15% change in the MESFET threshold voltage. Table 5.1 gives the summary of all the sensitivities discussed above.

B. Calculation of Component Widths for MESFET & Diode

MESFET gate width determination : The gate width of the MESFET is based on the transconductance (β) parameter value used by the SPICE input description data. The following equations are used to determine the relationship between the MESFET gate width and β. These equations apply to devices configured in Schottky Diode FET Logic [Shur, 1987].

$$\beta = \frac{2\ \epsilon\ \mu\ v_s\ W_g}{A\ (\mu\ V_{po} + 3\ v_s\ L)} \tag{1}$$

$$V_{po} = \frac{q\ N_d\ A^2}{2\ \epsilon} \tag{2}$$

$$V_{po} = V_{bi} - V_T \tag{3}$$

$$V_{bi} = \phi_{Bn} - 0.026\ ln\frac{N_c}{N_d} \tag{4}$$

Where,

ϵ = dielectric permittivity = 1.16 x 10^{-10} $Farads/meter$

μ = electron mobility = 5100 $cm^2/volt - sec$

v_s = electron saturation velocity = 10^7 cm/sec

V_{po} = pinch-off voltage, volts

V_{bi} = built-in voltage, volts

V_T = threshold voltage = -1.0 volt

N_d = channel doping density = 7.24 x 10^{16} cm^{-3}

A = channel thickness = 0.187 um

W_g = gate width, um

L = gate length = 1 um

ϕ_{Bn} = Schottky barrier height = 0.8 volts

N_c = density of states in the conduction band = 4.7 x 10^{17} cm^{-3}.

From equation (4), we get

$$V_{bi} = [0.8 - 0.026\ ln\frac{4.7X10^{17}}{7.24X10^{16}}]volts = 0.75volts \tag{5}$$

From equations (3) & (5), we get

$$V_{po} = 0.75 - (-1) = 1.75volts \tag{6}$$

From equations (2) & (6), we get

$$1.75 = \frac{1.6X10^{-19}\ coul(7.24X10^{16}\ cm^{-3})A^2}{2(1.16X10^{-12}\ Farads/cm}$$

Which implies that A, the channel thickness = 0.187 um

Substituting the value of A and the other constants in equation (1), we get

$$\beta = \frac{2(1.16X10^{-12}\ Farads/cm)(5100\ cm^2/volt{-}sec)(10^7\ cm/sec)W_g}{0.187X10^{-4}\ cm[(5100\ cm^2/volt{-}sec)1.75volts\ +\ (3X10^7\ cm/s)10^{-4}\ cm]}$$

Therefore, the value of MESFET gate width (W_g) in terms of the MESFET transconductance (β) is,

$$W_g = [(1.8846X10^4)\ \beta]\ \ um$$

Calculation of Diode Width : The diode width is determined by the SPICE parameter I_s i.e.,the saturation current of the diode (Amps). The equation that is used to find the relationship between I_s and the diode width is given below. This equation applies to the devices configured in Schottky Diode FET Logic [Sze, 1981].

$$I_s = W_d\ A\ A^*\ T^2\ e^{-\phi_{Bn}/0.026}$$

Where,

W_d = diode width, um

A = channel thickness = 0.187 um

A^* = 1.2 x Richardson constant = 144 $\frac{Amps}{cm^2\ K^2}$

T = absolute temperature in degree Kelvin

ϕ_{Bn} = diode junction potential = 0.8 volts.

From the equation above, we get

$$I_s = W_d(0.187X10^{-4}\ cm)\ 144\ \frac{A}{cm^2\ K^2}\ (300^2\ K^2)\ e^{-0.8/0.026}$$

Therefore, the diode width (W_d) is related to the diode saturation current (I_s) by the following equation:

$$W_d = [(1.95)X10^{14}\ I_s]\ \text{ um.}$$

C. Design of N+ and N- Resistors

Resistors can be constructed by using either N+ or N- implants. N+ and N- resistors are used for general precision requirements, with N+ resistors preferred over N- resistors because the N+ variety are less likely to be affected by nearby backgating effects.

N+ and N- implanted layers have a nominal sheet resistance of 125 and 1000 ohms/square respectively. The maximum current density rating of N- resistor is 0.15 mA/um resistor width and that of N+ resistor is 0.5 mA/um resistor width. Fig 5.12 shows a typical N- resistor structure. The values of W, W', and L are calculated from the following equations.

$W > Wmin = 7XImax(mA)$ in um.

$W' = W + 2$

$L = \frac{R(W+2.4)(W+0.1)-408.11(W+0.1)}{1000(W+2.4)} + 0.4$

where, L is in microns.

Fig 5.13 shows a typical N+ resistor structure where the dimensions are determined by the following equations.

$W > Wmin = 2XImax(mA)$, $Wmin$ in microns.

$W' = W + 2$

$L = \frac{R(W+2.4)(W+0.1)-408.11(W+0.1)}{1000(W+2.4)} + 0.4$

where, L is in microns.

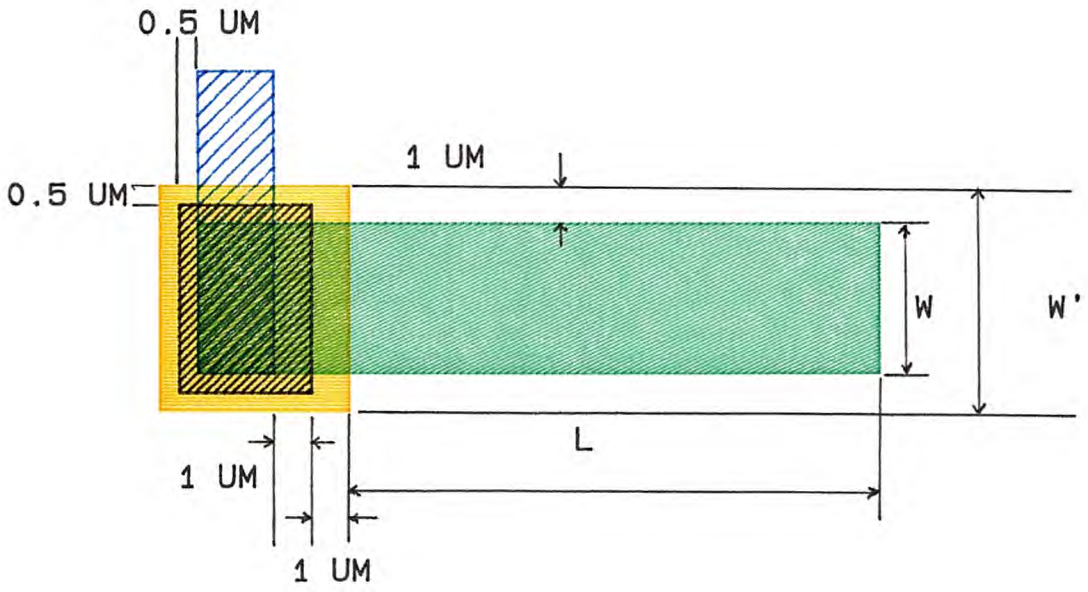


FIG 5.12 N- IMPLANTED RESISTOR

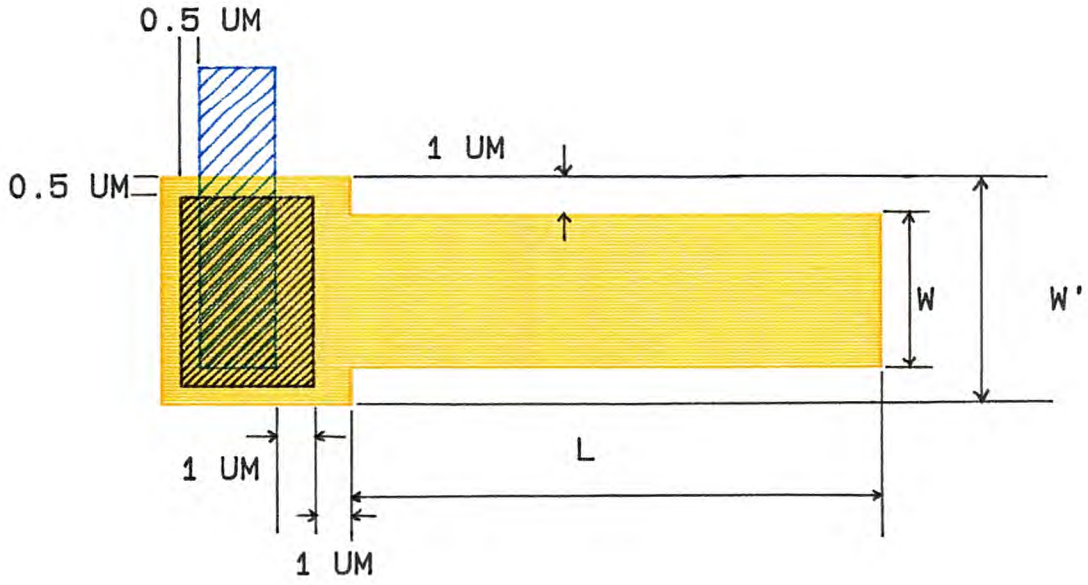


FIG 5.13 N+ IMPLANTED RESISTOR

D. Physical Layout

The layout of the temperture sensor circuit was done based on 1 um gate length depletion mode MESFET technology. The total sensor circuit occupies an area of 195x195 square microns. The mask key of the layers and the symbols used in the physical layout are shown in appendix A. The layout has been done using Layout Editor (LED) provided by the VALID CAE software. Fig 5.14 shows the layout of the temperature sensing diodes, with the differential amplifier and the voltage reference circuit. Fig 5.15 shows the layout of the nand latch circuit. Finally, the layout of the complete sensor circuit is shown in the fig 5.16. In laying out the circuit, the design rules enumerated in the appendix A, have been strictly followed.

In the layout, N- ion-implantation layer is used to form the MESFET channel and N+ layer for the diffused diodes. N- layer is also used to form ion-implanted resistors. N+ ion-implantation is used to form the source and drain contact regions. Similar to the N+ layer, N- layer can also be used to form diodes and implanted resistors. Ohmic metal is defined on top of N+ implants and alloyed to GaAs to form low contact resistance ohmic contact. Ohmic metal is never used for interconnections. The gate metal makes a Schottky barrier contact with GaAs and is defined using a lift-off process. The smallest feature on the gate metal mask is 1 um and is the most critical mask for gate alignment. Gate metal is never used for interconnections. Metal 1 (1ME) is used for the first level interconnections. It is also used to form the bottom electrode of the MIM capacitors. 1ME connects to ohmic metal and gate metal by physically overlapping it. There is no need for a via to define the contact areas in these cases.

That is, the gate metal, the ohmic metal and 1ME are at the same mask level in the lithography process. Intermetal via is used to make contact between the 1ME and metal 2 layers. Metal 2 is used to interconnect various parts of the circuit. It is also used to form the top electrode of the capacitor, inductor coils. The first level metal is the only metal that can be connected to the metal 2 through the intermetal via.

TEMPERATURE SENSING DIODES WITH DIFFERENTIAL AMPLIFIER AND REFERENCE VOLTAGE

CELL LENGTH = 121 UM
CELL HEIGHT = 195 UM

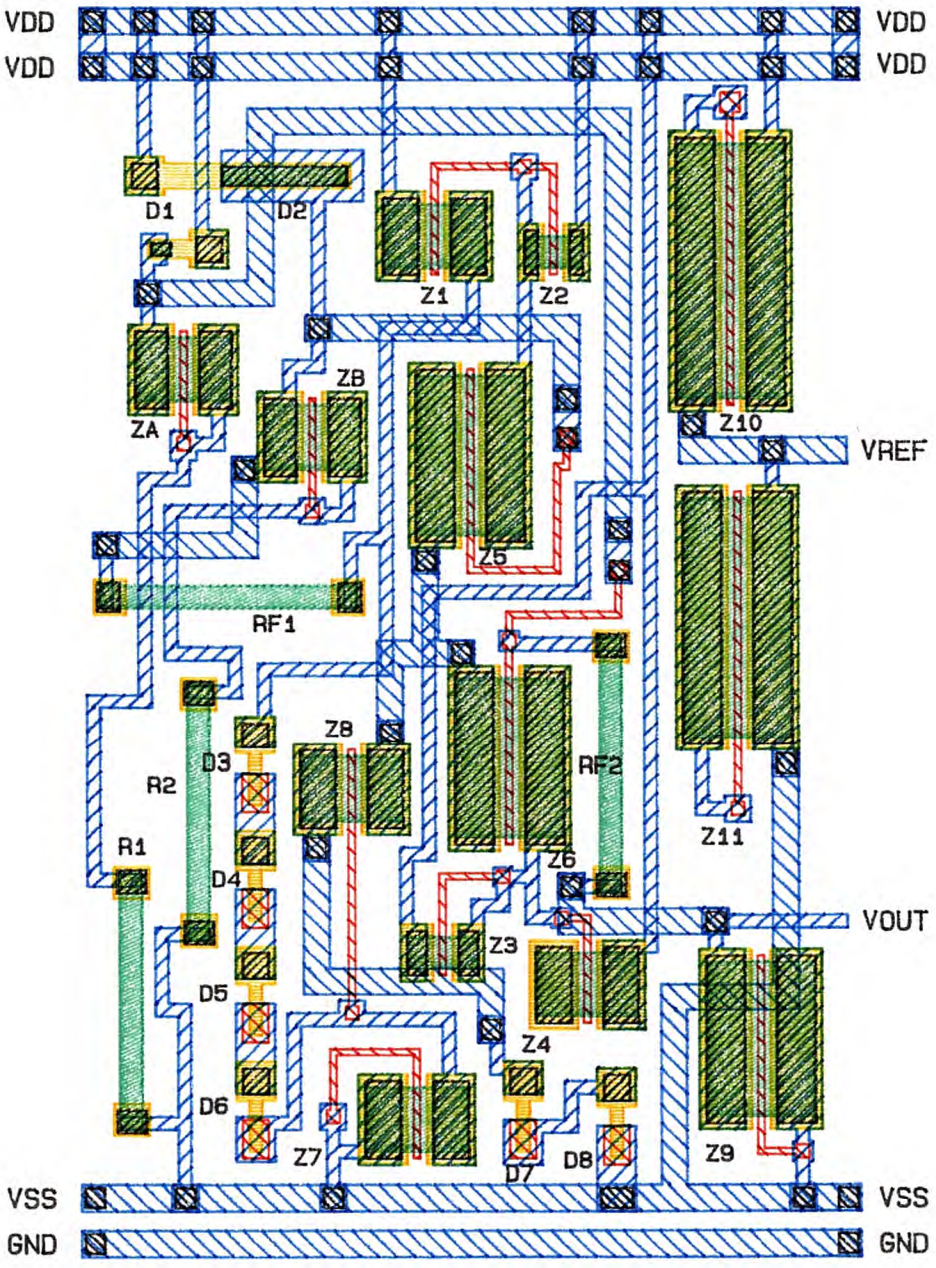


FIG 5.14

NAND LATCH CIRCUIT

CELL LENGTH = 74 UM
CELL HEIGHT = 195 UM

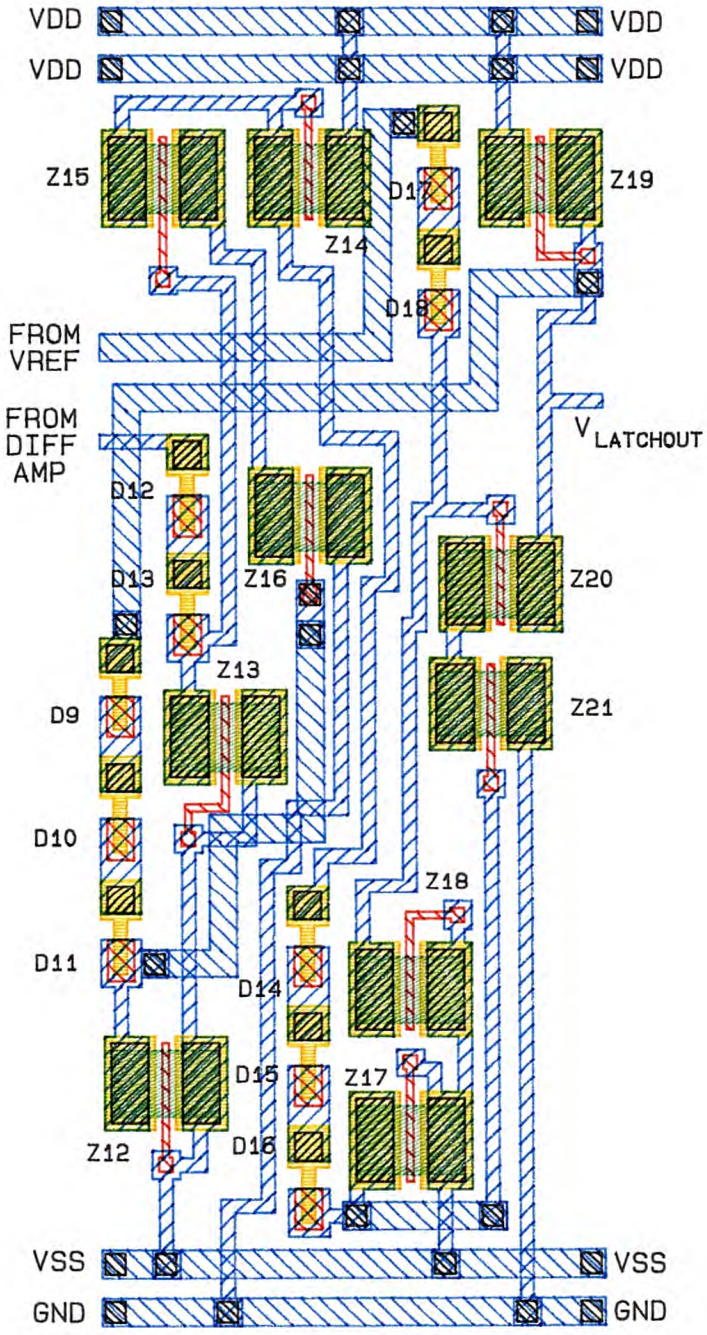


FIG 5.15

TEMPERATURE SENSOR CELL
1 UM DEPLETION MODE GAAS MESFET TECHNOLOGY

CELL LENGTH = 195 UM
CELL HEIGHT = 195 UM

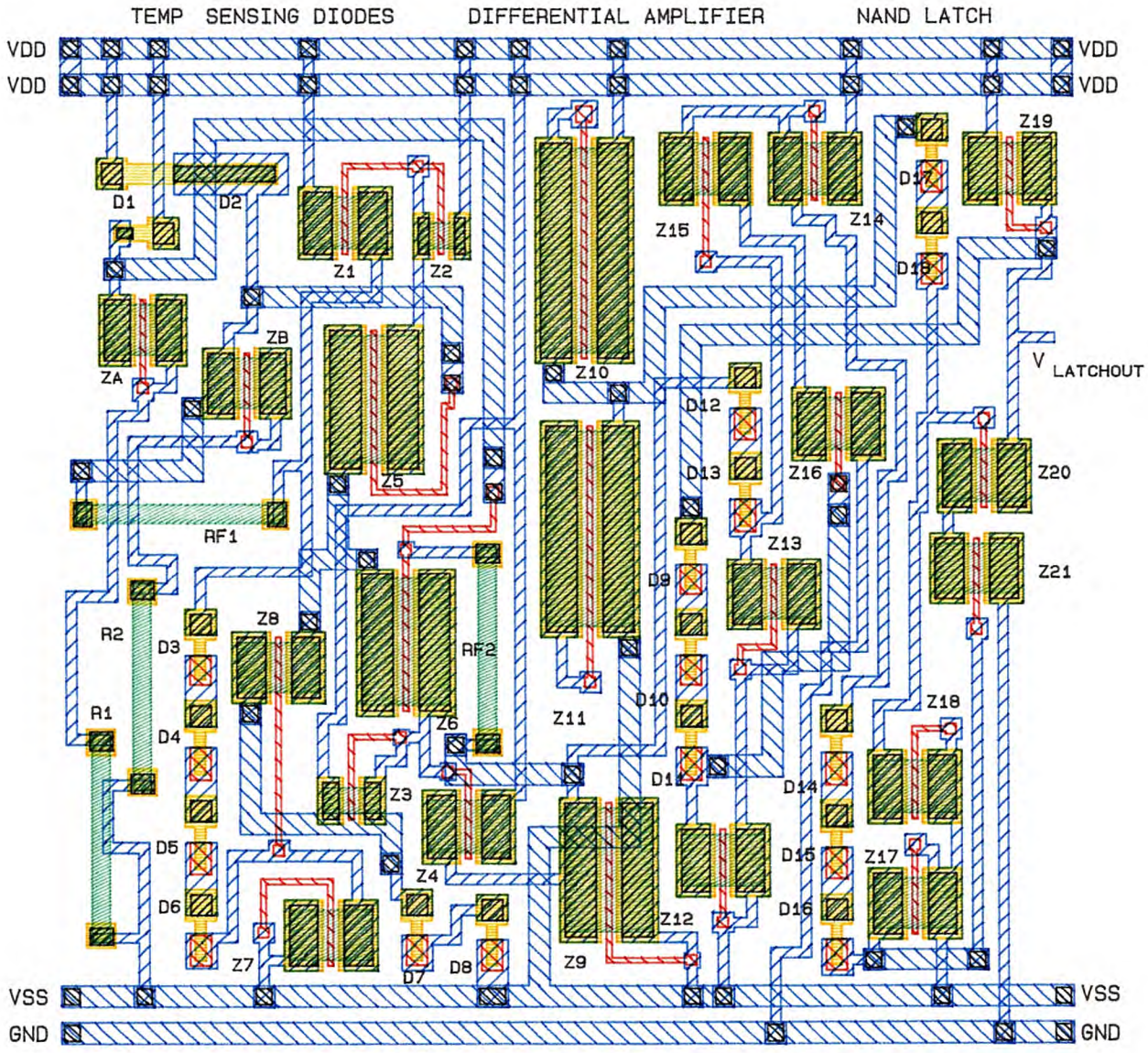


FIG 5.16

E. References

1. W.R. Curtice, A MESFET Model for Use in the Design of GaAs Integrated Circuits, IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-28, No. 5, pp. 448-456, May (1980).

2. Joseph Mun, *GaAs Integrated Circuits Design and Technology*, Macmillan Publishing Company, N.Y., pp. 100-105 (1988).

3. L.E. Larson, J.F. Jensen, H.M. Levy, P.T. Greiling G.C. Temes, GaAs Differential Amplifiers, IEEE GaAs IC Symposium, pp. 19-22 (1985).

4. Michael Shur, *GaAs Devices and Circuits*, Plenum Press, N.Y., pp. 450-476 (1987).

5. H. Statz, P. Newman, I.W. Smith, R.A. Pucel and H.A. Haus, GaAs FET Device and Circuit Simulation in SPICE, IEEE Transactions on Electron Devices, Vol. ED-34, No.2, pp. 160-169, Feb (1987).

6. S.M. Sze, *Physics of Semiconductor Devices*, Wiley, N.Y., pp. 279-293 (1981).

CHAPTER VI

SUMMARY AND CONCLUSIONS

The temperature sensor circuit designed, can be used as a standard cell in GaAs ICs for providing an alarm mechanism that initiates systems-level cooling or shut down in order to safeguard the chip when it gets too hot. The sensor circuit sets a NAND latch when the chip cell temperature reaches 125 °C. The output of the latch can be sensed by additional circuits(on or off the GaAs chip) which initiate the cooling.

The circuit simulation was done using SPICE3B.1 software installed on VAX station II/GPX hardware in Ultrix V2.0 Operating System environment. The Valid CAE software has been used for the schematic capture and the physical layout of the sensor circuit. The photolithography mask key utilizes 8 layers viz., active area (N-), source & drain (N+), ohmic contact, Schottky gate metal, first level interconnect or metal1, metal2, intermetal via and passivation. In the layout, N- implantation is used to form the MESFET channel and N+ layer for the diffused diodes. N+ ion-implantation is used to form the source and drain contact regions. Similar to the N+ layer, N- layer can also be used to form diodes and implanted resistors. Ohmic metal is defined on top of N+ implants and alloyed to GaAs to form low contact resistance ohmic contact. Ohmic metal is never used for interconnections. The gate metal makes a Schottky barrier contact with GaAs and is defined using a lift-off process. The smallest feature on the gate metal mask is 1 um and is the most critical mask for gate alignment. Gate metal is never used for interconnections. Metal1 connects to ohmic metal and gate metal by physically overlapping it. There is no need for a via to define the contact areas in these cases. Metal 2 is used to interconnect

various parts of the circuit. The total area of the GaAs sensor circuit is 195x195 square microns.

The worst case error demonstrated by the sensor circuit due to the cumulative effect of ±5% variations in the MESFET threshold voltage, diode junction potential, power supply voltage, resistor layout mismatch and ±10% variation in the MESFET transconductance was found to be 7.7 °C.

Finally, the suggestions for future works include, fabrication of the sensor cell and testing its functionality by incorporating it into a GaAs IC chip.

APPENDIX A

LAYOUT DESIGN RULES AND PROCESS PARAMETERS

The mask key used for the layout of the GaAs temperature sensor cell is shown in the fig A.1. The Layout Design Rules are enumerated below:

1. N+ to N- spacing in level shifting diodes (Forward biased) = 2 um.

2. When gate metal is positively biased with respect to implant region (either N- or N+) the following rules should apply:

Implant to gate metal spacing = 3 um (for V < 3v)

Implant to gate metal spacing = 5 um (for 3v > V > 5v)

Implant to gate metal spacing = 7 um (for V >= 5v).

3. N+ to gate spacing = 1um inside the FET channel.

4. Gate on N- overlap, when gate exits N- in a FET channel = 1um.

5. N+ overlap (on the gate side) beyond the ohmic source and drain contacts = 1um.

6. 1ME on ohmic, (on the gate side) beyond the ohmic source and drain contacts = 1um.

7. Conservative rule for backgating dictates that the spacing between two adjacent devices (or spacing between a device and a backgating electrode) be such that there be 1um spacing per volt of the potential difference between the two nodes.

8. Minimum contact area, 1ME on gate = 2 x 2 um^2.

9. Maximum metal2 width = 20 um, any wider than 20um should be split into smaller width segments.

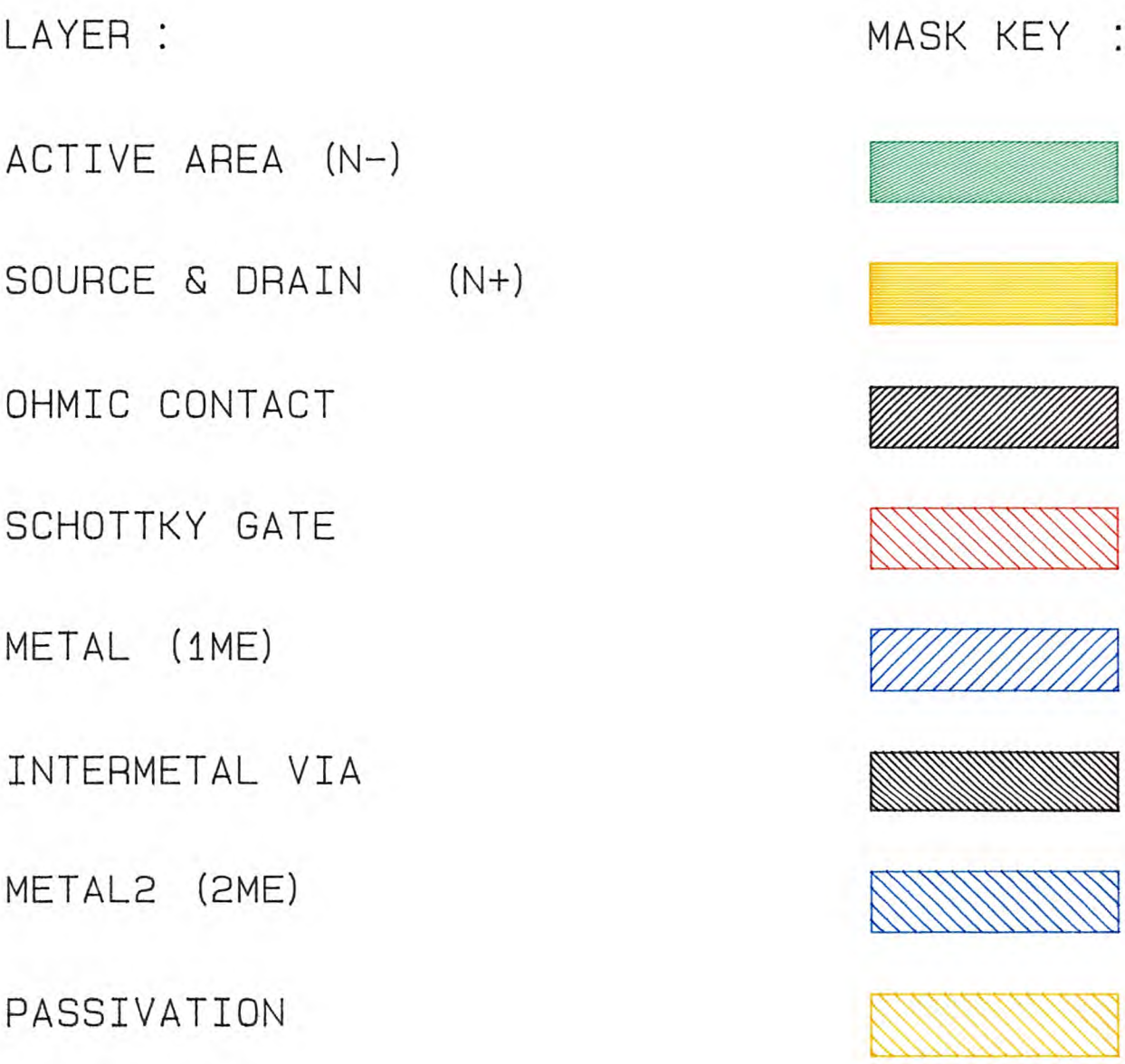


FIG A.1

MASK KEY FOR GALLIUM ARSENIDE 1 PROCESSES

10. Minimum bond pad size = 100 x 100 um^2.

11. Interdie scribe moat size (on layers 8 and 10) = 150 um.

12. Minimum bond pad to scribe moat edge = 25 um.

13. Minimum bond pad to the nearest implant or metal = 20 um.

14. Bond pad center to bond pad center = 150 um.

15. All gates should be oriented in the same direction. When digitizing, all all the gates should be in the perpendicular direction to avoid confusion.

16. There must be a 1ME layer underneath the intermetal via layer.

17. All corners of metal2 should be gusseted.

18. There should be no 'donut' or almost closed structures on ohmic contact layer, Schottky gate layer and 1ME layer.

19. On dual gate FETs, both the gates should be digitized at 0.75 um and the spacing between them should be digitized at 1.25 um. When the masks are fabricated, the gated will end up being 1 um and the spacing between them will be 1 um.

20. There is a need for passivation via to open the bond pads and the test pads for probing and wire bonding. Passivation via should be inside the intermetal via by 2 um on bond pads and test pads.

21. Long parallel lines of 1ME should be avoided. A rule of thumb is to avoid lines where (L/W) > 80. This rule should be used in conjunction with the area/gap rule for 1ME. See fig A.2.

22. Metal exiting from the bond pad must be 1ME or combination of 1ME/2ME. It should never be 2ME alone in the air as it gives rise to problems during testing and bonding.

23. When there are multiple parallel metal2 lines, with intermetal via or

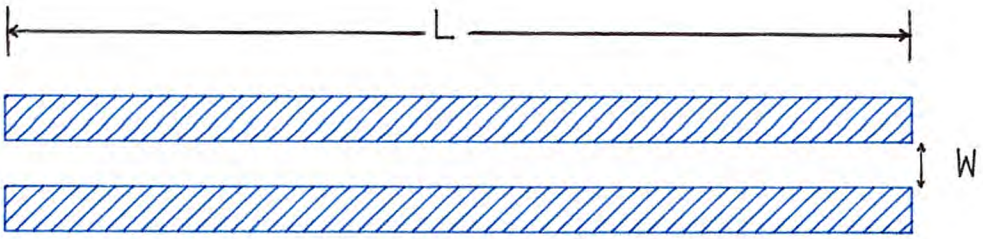


FIG A.2 LONG PARALLEL LINES OF 1ME

FIG A.3 STAGGERING VIAS/SUPPORT POSTS

support posts all in one line as shown in the fig A.3, the intermetal vias should be staggered. The recommended stagger is 7 um, the next grid point.

Minimum Digitized Feature sizes of the different layers are shown in table A.1. The electrical parameters of the different layers are listed in tables A.2 and 3. The process specifications are given in table A.2. Table A.3 describes the typical, minimum and maximum parameter values for a 1x300 um device which is arranged in an interdigitated manner with 50 um wide fingers. The gate to source and gate to drain spacings are both 1 um.

LAYER	LENGTH	WIDTH
N- IMPLANT (ACTIVE AREA)	2 UM	2 UM
N+ IMPLANT (SOURCE & DRAIN)	2 UM	2 UM
OHMIC CONTACT	2 UM	2 UM
SCHOTTKY GATE METAL	1 UM	2 UM
INTERMETAL VIA	3 UM	3 UM
METAL 1 (1ME)	2 UM	2 UM
VIA/SUPPORT POST	3 UM	3 UM
METAL 2 (2ME)	4 UM	4 UM
PASSIVATION	25 UM	25 UM

TABLE A.1 MINIMUM DIGITIZED FEATURE SIZES

SYMBOL	PARAMETER NAME	NOMINAL	MINIMUM	MAXIMUM	UNITS
RSNM	SHEET R OF N-	1000	800	1200	OHM/SQ
RSNP	SHEET R OF N+	125	100	150	OHM/SQ
RS1ME	SHEET R OF 1ME	85	70	110	MOHM/SQ
RS2ME	SHEET R OF 2ME	20	10	30	MOHM/SQ
CMIM	CAPACITANCE OF MIM	0.275	0.23	0.32	fF/UM^2
TCRNP	TEMP COEFF OF N+ R (0 TO 150 C)	0.07	—	—	% /DEG C
TCRNM	TEMP COEFF OF N- R (0 TO 150 C)	0.13	—	—	% /DEG C

TABLE A.2 PROCESS SPECIFICATIONS (25 C)

SYMBOL	DC PARAMETER NAME	NOMINAL	MINIMUM	MAXIMUM	UNITS
-Vp [Vds = 2.5 V] [Ids = 300 UA]	PINCHOFF VOLTAGE	1.5	1.2	1.8	VOLTS
Idss [Vds = 2.5V] [Vgs = 0 V]	S-D SATURATION CURRENT	45	32	58	mA
$g_m dc$ [Vds = 2.5V] [Vgs = 0 V]	TRANSCONDUCTANCE	40	34	46	mS
BVGSO	G TO S BREAKDOWN VOLTAGE	10	7	—	VOLTS
BVGDO	G TO D BREAKDOWN VOLTAGE	10	7	—	VOLTS

TABLE A.3 DEVICE SPECIFICATIONS (25 C)

APPENDIX B

VALID DESIGN METHODOLOGY

Valid software design tools enable the user to create, modify, and manage logic designs. The block diagram, showing various design packages available in Valid software, can be seen in the fig B.1. Valid, basically has two editors GED (Graphics Editor) and LED (Layout Editor). In GED, using a convenient menu of commands, bodies (the graphical representation of library parts) can be called from a full spectrum of Valid-created libraries. Then, the bodies can be wired together by drawing lines with the mouse. All or part of a design may be moved or copied very quickly. LED is used to create and modify mask layouts for integrated circuits.

The GED window includes four items - the cursor, the command area, the command menu and the status line. the cursor moves around the screen as the mouse is moved. An item can be chosen from the menu by pointing to it with the cursor and clicking one of the buttons on the mouse. The cursor and the mouse are used to draw lines, position library parts, and move parts of the drawing. The command menu is the boxed list on the right side of the screen. It contains many of the GED commands. When one of these commands is selected, the corresponding box is highlighted. Most of the commands listed in the menu are self-explanatory. The command area is at the bottom of the screen. The commands can be typed here instead of choosing from the command menu. There are more GED commands than those appear on the menu. These have to be typed in the command area. The status line has three items - name of the

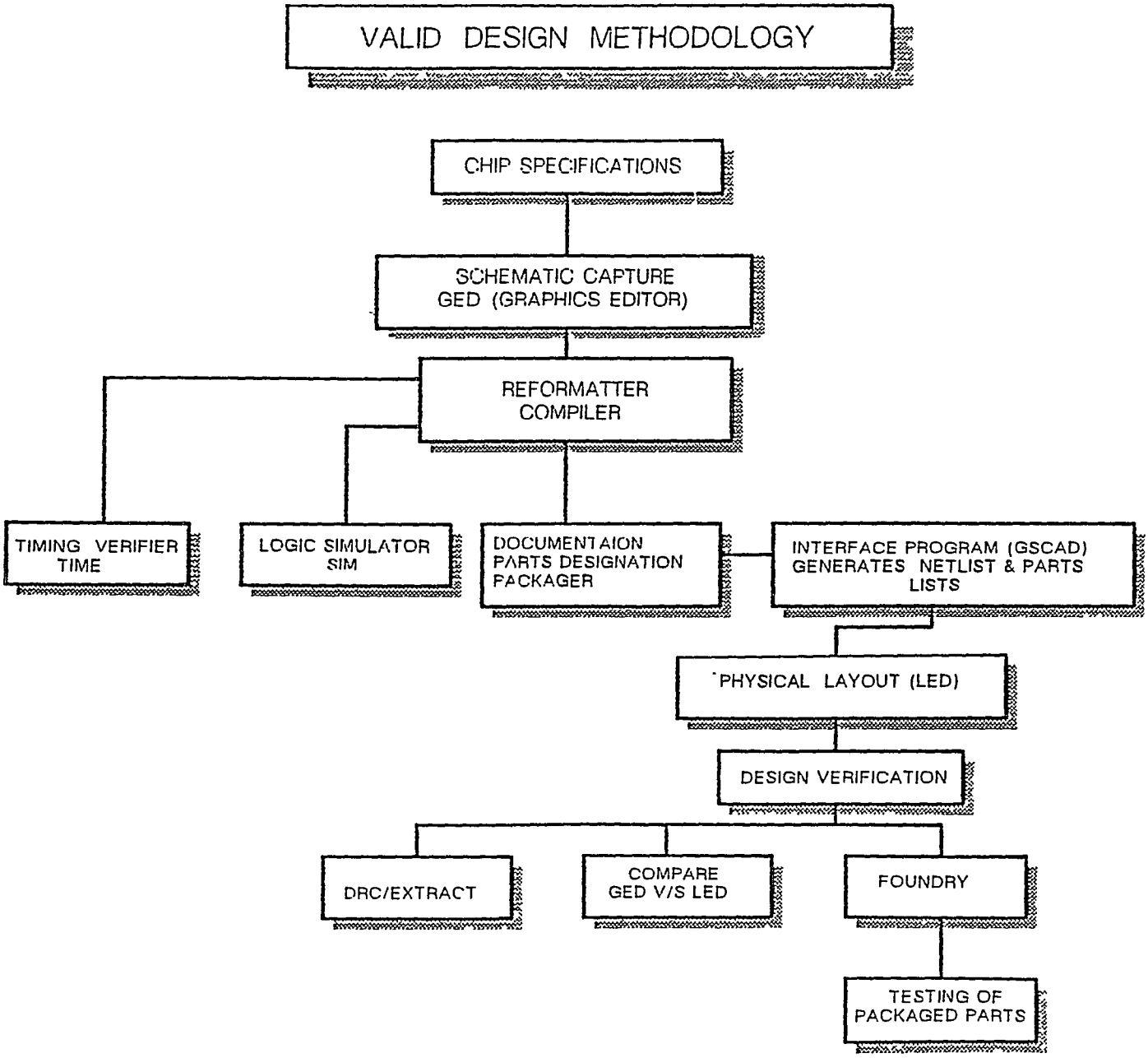

VALID DESIGN METHODOLOGY
CHIP SPECIFICATIONS
SCHEMATIC CAPTURE
GED (GRAPHICS EDITOR)
REFORMATTER
COMPILER
TIMING VERIFIER
TIME
LOGIC SIMULATOR
SIM
DOCUMENTAION
PARTS DESIGNATION
PACKAGER
INTERFACE PROGRAM (GSCAD)
GENERATES NETLIST & PARTS
LISTS
PHYSICAL LAYOUT (LED)
DESIGN VERIFICATION
DRC/EXTRACT
COMPARE
GED V/S LED
FOUNDRY
TESTING OF
PACKAGED PARTS

Fig B.1

drawing currently edited, the grid setting and the current working directory.

The LED screen contains several display areas which are briefly described below. The command menu is the vertical column of boxes at the right hand edge of the screen. These boxes contain the most commonly used commands. The command menu can be customized to suit the requirements of the user. Active Palette is the column to the left of the command menu. This is a menu that shows the currently active and visible layers. These layers are determined by the process or technlogy being used to create the design. The Graphics box is a rectangular or trapezoidal graphics cursor. The shape and size of the box is set, to define areas for painting and editing. The Grid is used to guarantee that the distances between the chip coordinates are accurate. The grid spacing, the displayed interval and the origin coordinates can be set by the user to suit the design. LED can be tailored to meet specific design requirements. There is a default.tech file in the layout directory which is the system-wide default technology file. This file sets the default technology for cells created on the system. The default.cmap file in the layout directory is the system-wide default colormap file, which sets the default colors used to display on the system. The system allows the users to create their own technology and colormap files to suit the requirements of the process. The technology of a cell corresponds to the fabrication process used to create the chip.