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Design and development of CCD camera for document scanner using optical fiber bundle

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ABSTRACT

Design And Development of CCD Camera For Document Scanner Using Optical Fiber Bundle

by

Aniruddha P. Joshi

A CCD camera for the gray scale document line scanner has been designed and developed at Photon Imaging Corp. The scanner consists of a revolutionary optical fiber bundle, CCD camera, and control electronics. The key concept resides in the fiber-optic bundle. At one end it has a linear array of equally spaced light guides. These terminate at the opposite end in a square array with a polished surface for viewing by a camera. The fan-out from linear to square end is not done with attention to ordering, so the bundle may be relatively inexpensive. Reordering is done electronically using an address map unique to each bundle. The CCD used is a virtual phase imager from Texas Instruments with a resolution of 165 x 204 pixels. The CCD clocking sequence is generated using EPROM and different voltage levels are switched using fast switching transistors. The CCD chip output is compensated for dark voltage with run time dark voltage reference. The output of the camera is digitized by a flash analog to digital converter and stored in the scanner memory. The Scanner/camera has a serial interface to transfer the data from memory to a host computer, PC. For serial communication HDLC protocol is used. The scanned document can be viewed on the PC monitor or can be printed for hard copies with half tone techniques to preserve gray scale information. The scanner has a resolution of 300 dpi, compatible with todays laser printers.

2) DESIGN AND DEVELOPMENT OF CCD CAMERA FOR DOCUMENT SCANNER USING OPTICAL FIBER BUNDLE

by

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To my Mother and Father

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CHAPTER 1

INTRODUCTION

New Jersey Institute of Technology in co-operation with Photon Imaging Corp. of Edison, NJ is currently supporting optoelectronics projects in the field of document imaging with a charge coupled device (CCD) imager. The scanner/camera described in this thesis was designed and developed at Photon Imaging Corp. under the direction of Professor Walter F. Kosonocky, Chair Professor of Electrical Engineering at New Jersey Institute of Technology, Prof. Eugene Gordon at New Jersey Institute of Technology, and Mr. Peretz Feder, Vice President Engineering at Photon Imaging Corp. This project was developed for possible future products of Photon Imaging Corp. Products are held by Photon Imaging Corp. where the basic concepts were developed.

1.1 General Description of Document Scanner

Since the invention and development of CCD's in the early 70's the remarkable versatility of this devices has led to their applications in a diverse number of fields. These applications include visible and IR light imagers i.e. videos and still cameras, optical character recognition for desktop publishing and document storage, digital memories, signal processing, etc. The goals of this thesis project were to design and develop a document scanner using a CCD camera with the help of an

optical fiber bundle. The CCD camera can also be used as stand alone equipment.

Most document scanners are used to scan a document in a raster mode and store it in the memory of a host computer, e.g. personal computer (PC). The number of picture elements in a typical line exceeds 2550 so that extremely high resolution CCD linear arrays are used typically. These are expensive. Patented approach, based on less expensive rectangular CCD array is described in this thesis. To capture the image line by line, an optical fiber bundle in a linear array is coupled with the CCD camera. Because of this combination and the sensitivity of the CCD cells, the document can be scanned with gray scale. The fiber bundle has horizontal resolution of 300 dpi, hence the document scanned has the resolution of 300 dpi which is compatible with the todays laser printer.

Part of the scanner is a CCD camera that has a resolution of 192 x 165 pixels. The data collected by the CCD chip, a line of the document, is transferred to the PC's memory via a communication link. The picture taken can be seen on the VGA monitor of the computer. The scanner works in a simple way. The paper to be scanned is held on a plate and a fiber bundle, in a linear array, held virtually against the paper, scans the paper in the vertical direction relative to the document. The other end of the bundle is brought to an incoherent square array. Incoherent means no attention is paid to position or spacing of the fibers in the square face. For every position of the linear bundle, the CCD camera takes the picture and the data from the CCD

camera is digitized and sent to a PC for storage. The stored data can be used to display the document on the monitor or can be used to make hard copies. The gray scale information of the picture can be printed by half tone techniques.

The key element in the process is a look-up table unique to the particular bundle. It provides the correspondence between pixel address positions at the linear end of the fiber bundle and CCD elements. Although the bundle has 2550 fibers the CCD has more than 31000 elements. There are thus about 12 CCD elements for each fiber and only one CCD cell is used per fiber. This makes alignment unnecessary. The look up table is created in an initialization procedure to be described later.

In this thesis, block diagram description of the scanner is described in second chapter. Image sensor description is in third chapter which can be read afterwards to keep flow of scanner description. Design of the circuits is explained in chapter four. The demonstration of the operation of the CCD camera is described in chapter five and conclusion is in chapter six.

CHAPTER 2

BLOCK DIAGRAM AND DESCRIPTION OF SCANNER

Basic building blocks of the scanner are the fiber bundle and illumination source, the stepping table to move the paper, CCD camera, the initialization procedure and look up table and signal processing to create the image in bit map to either display on the monitor or to make hard copy.

The fiber bundle used for the scanner is obtained commercially and described in some detail later. Illumination is done in a relatively unique way and part of the work is reported in thesis. Most of the detail in the thesis will relate to design of the camera for the CCD chip which is different in significant aspects from typical CCD chips used in video cameras. The initialization procedure described here is an experimental one and the actual process used for the production is not described here as it is proprietary. Image processing and details of the output end of the scanner are not described for the same reason. The stepping table used to advance the paper was obtained from a commercial scanner. In the scanner project author was responsible for the CCD camera design and development. The focus of this thesis on the camera is consistent with the objectives of Prof. Kosonocky's group.

The block diagram of the document scanner is shown in Fig. 1. The scanner consists of the fiber bundle, light source, CCD camera, control circuitry, look up table and communication interface. A detail

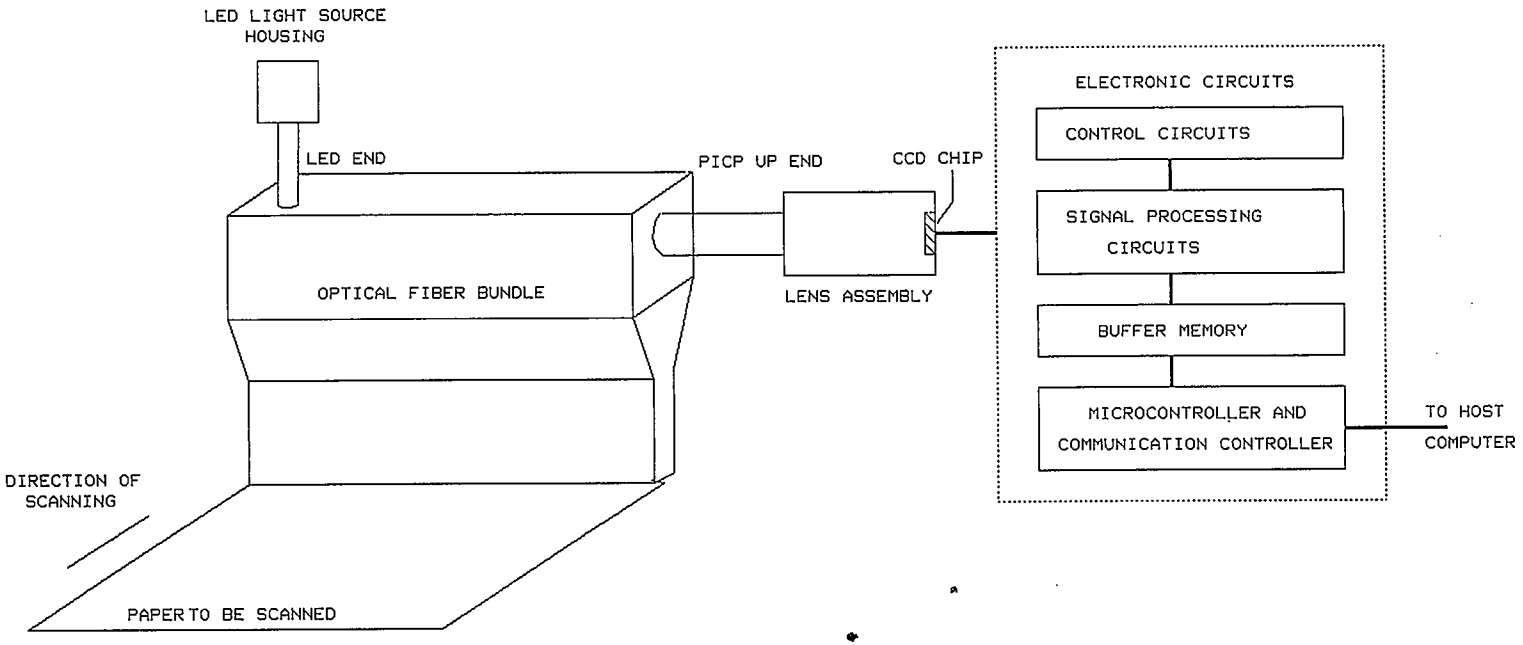

FIG.1 BLOCK DIAGRAM OF DOCUMENT SCANNER

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description for every part is given below. The initialization is also described.

2.1 Fiber Bundle

The optical fiber bundle used in the document scanner is shown in Fig. 2, with it's details. The fiber bundle consists of two rows of fibers, one for illumination of the line to be scanned and the other for information pick up of the reflected/scattered light from the scanned paper. The two rows of fibers are laid one over the other. Each row is brought out to a separate bundle; one circular and one square respectively.

The first row of illumination fibers are used to provide uniform illumination of the line to be scanned. The light source used is a single ultra bright LED. Ground glass is used to diffuse the light incident on the circular end. This diffused light is passed on to the paper via the illumination fibers. The diameter of the illumination fibers is 250 micron, which is good enough to provide uniform light on the line of the paper. The illumination fibers are squeezed into a circular shaped bundle for good coupling to the LED light source. As mentioned before the light source is an LED that provides light in circular area.

The second row in the fiber bundle is for the pick up. This is the row which actually transfers graphic information on the paper to the CCD camera. It provides the optical coupling between the paper and the CCD camera. The scanner is designed for a resolution of 300 dots

per inch (dpi). The pick up fibers are laid in a row and have a diameter of about 70 micron. The spacing between two fibers is 10 to 15 microns. The width of the bundle is 8.5 inches which is compatible with letter size paper. Hence there are 2550 (300 x 8.5) fibers in every bundle for information pick up. The other end of the bundle is the randomly squeezed fibers in a square shape for coupling into the CCD.

Fig. 2 shows a fiber bundle in horizontal view and vertical view looking from the paper side. To scan the paper, line by line, the fiber row moves in the vertical direction relative to the paper. In this way the whole paper can be scanned with horizontal resolution of 300 dpi. The vertical resolution depends upon the distance traversed by the fiber bundle during the scan cycle. The resolution is arbitrary; the tradeoff is the time to scan a full page versus vertical resolution.

2.2 Light Source for Illumination

As mentioned before a single LED is used as a light source. A ground glass is used to get uniform light for illumination on the paper by diffusing the light falling on the circular bundle. The LED is placed in a housing with the ground glass (Fig. 1). This housing fits on the illumination end of the fiber bundle. The CCD chip can not be exposed to light while it is being read as described later, so that the LED is turned ON when the CCD is integrating the reflected light from the paper and is turned OFF while the CCD is being read. The paper is moved during the read cycle. The light source, an ultra bright LED has

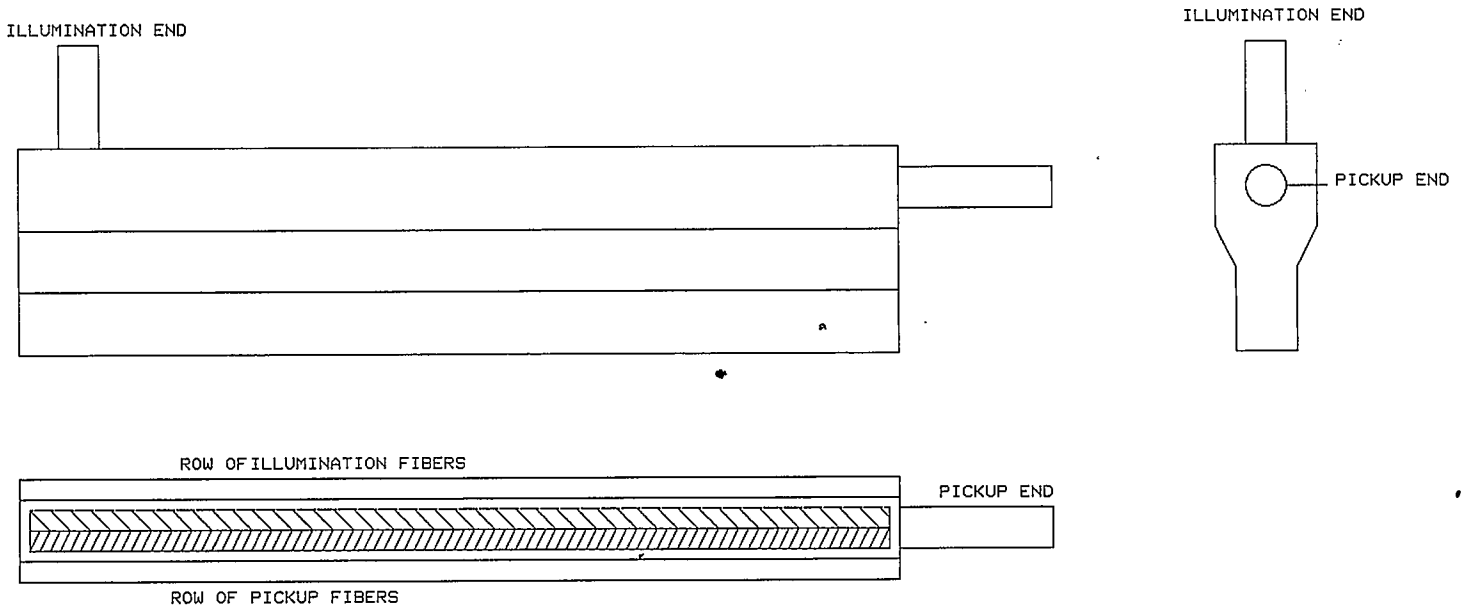

FIG.2 FIBER BUNDLE USED IN DOCUMENT SCANNER

FIGURE NOT TO SCALE

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brightness of 1000 mCds. The brightness of the LED, even with all the coupling loss, is sufficient to saturate the CCD cells.

2.3 Lens Assembly

The size of the square fiber bundle at the pick up end is 3.75 mm x 3.75 mm and the size of the CCD chip is 2.64 mm x 2.64 mm. Hence 1.5:1 demagnification is used to map the pick up end of the fiber bundle onto the CCD chip. The lens does the job of imaging the picture at the fiber bundle to the CCD chip. The lens assembly has a small adjustment for accurate focussing and can be locked into this position by a ring nut which slides over the assembly.

2.4 CCD Chip and It's Mounting Assembly

The CCD chip is arranged in a two dimensional array. It has 210 cells called pixels in a row and contains 165 rows. Each row includes 12 unilluminated/dark pixels at the end. Hence there are 34650 usable pixels in total on the CCD chip. The size of each pixel is 13.75 micron x 16 micron. The active CCD area is almost a square. As the fiber bundle pick up end is also a square, it is easy to map the pick up end of the fibers to the CCD chip. Each fiber on the pick up end corresponds to at least 12 CCD cells approximately on the CCD chip.

The CCD has only active image area. It has no frame memory consequently it must have a distinct integration cycle. Followed by a

read cycle during which time there can be no light, otherwise blurring of the image will result.

A process called initialization maps one fiber at the linear end to only one CCD element. In the initialization process, light is projected through one fiber at a time. All the CCD cells are read and the cell that reads the maximum output is mapped to that fiber. This step is repeated for all 2550 fibers to find a corresponding mapped pixel on the CCD. Each fiber bundle and CCD chip has their own unique initialization map or look up table. This map is the key to the scanner. This map is essential because only the output of the mapped CCD cells of appropriate fibers are selectively stored in the scanner's memory and these are related properly to the fibers. All other CCD pixels are not relevant.

Initialization is a time consuming process but it has to be done only once for each fiber bundle and CCD chip combination. There are proprietary schemes for doing initialization rapidly in production.

The CCD must be read completely during each cycle . This takes time. A more efficient imaging device would allow random access reading of the appropriate pixels. Such devices do exist but are either extremely expensive or do not provide gray scale. Even when not used in the output, the gray scale is essential for initialization and signal processing.

2.5 Control Circuitry and Signal Processing

The control circuitry used the document scanner is used for clocking the CCD chip and storing the digitized data from the CCD cells in the buffer memory. The block diagram of scanner electronics is shown in Fig. 4.

The CCD chip requires three different signals for it's operation. These signals are derived from the EPROM and related circuitry. In the signal processing block the output from the CCD cell is compensated for dark voltage from the dark cells and amplified so that it can be fed directly to the analog to digital (A to D) converter. The scanner has a fast A to D converter. This A to D converter quantizes the CCD cell output gray scale output information. The digitized output is stored into the buffer memory of the scanner. There is an address counter, read/write signal generator and tristate buffers for the buffer memory. The Buffer memory is also accessed by a microcontroller when the information stored in memory is transferred to a host PC. This block includes the microcontroller and related hardware, serial communication controller and interface for communication.

The electronics of the document scanner has been divided into two boards called analog and digital boards. The analog board contains analog circuitry with some relevant digital hardware; the other board contains all other digital circuitry.

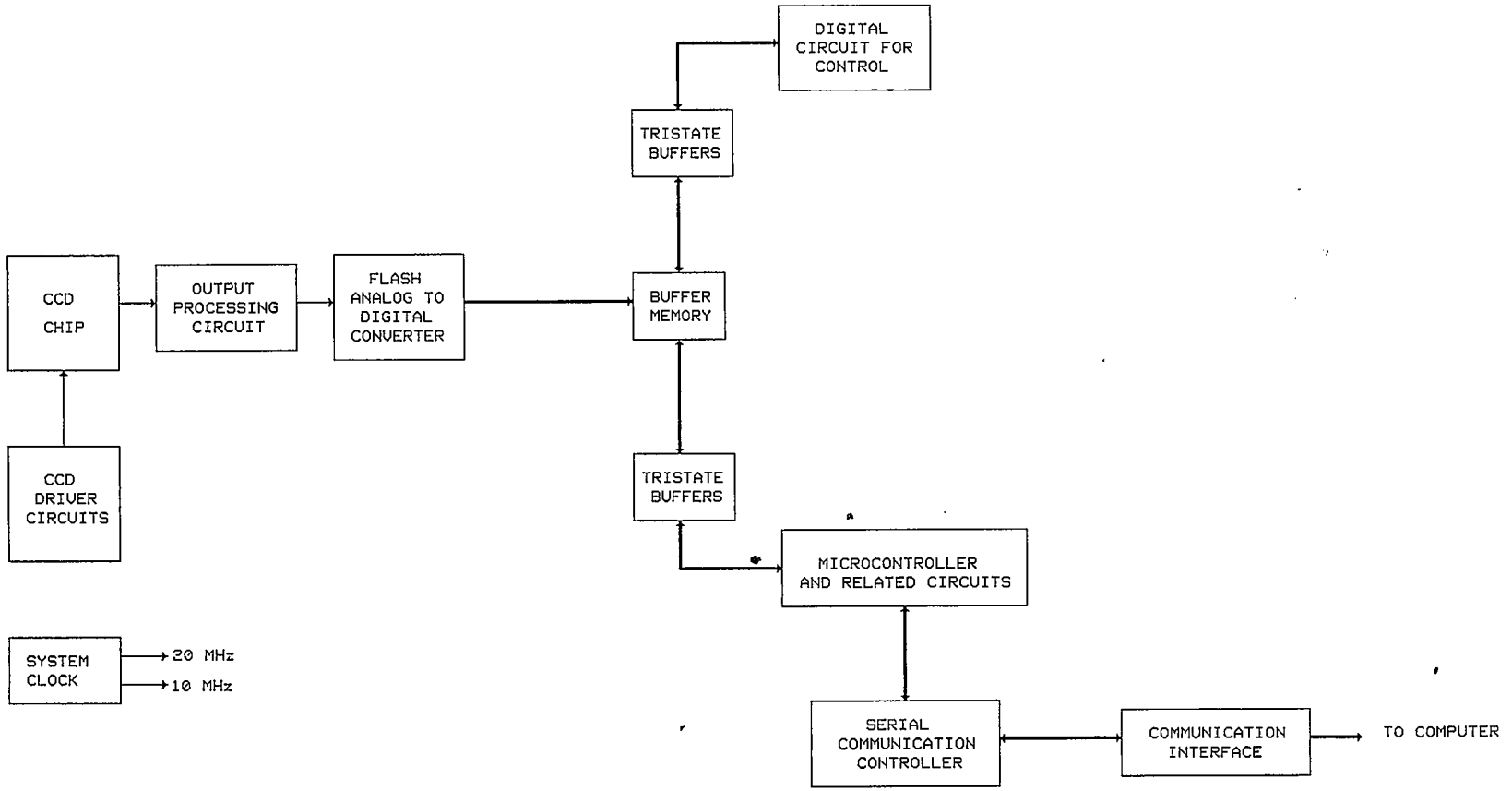

FIG. 4 FIBER OPTIC SCANNER ELECTRONICS

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A detailed block schematic is shown in Fig. 5. The analog board includes the CCD chip and it's clock drivers, clock generator, micro coded EPROM, address counter, read signal generator, initialization EPROM and related circuitry, CCD output signal processing circuit and flash A to D converter with it's output latch. The digital board consists of buffer memory, address counter, read/write generator, microcontroller, serial communication controller and interface for data transfer.

The CCD chip requires three different clock signals serial gate clock, antiblooming clock and image area gate clock. All of these clocks are generated using a micro-coded EPROM and transistors drivers. CCD requires nonstandard voltage levels clocks for operation. The transistors are switched ON and OFF in a certain sequence so as to generate the proper clocks for the CCD chip. The address counters are used to generate these sequences from an EPROM. The sequence is repeated for every line as the CCD is read line by line. This process stops when the line counter counts to zero which indicates that 165 lines have been read. The line counter is used as the end of frame signal.

The signal coming out of the CCD cell has to be compensated for dark voltage. Hence the CCD cell output is fed to a subtracter which subtracts the dark voltage every time. The dark voltage reference is formed by holding the dark current value of the previous line from the CCD chip in the sample and hold circuit. The last 12 pixels in every

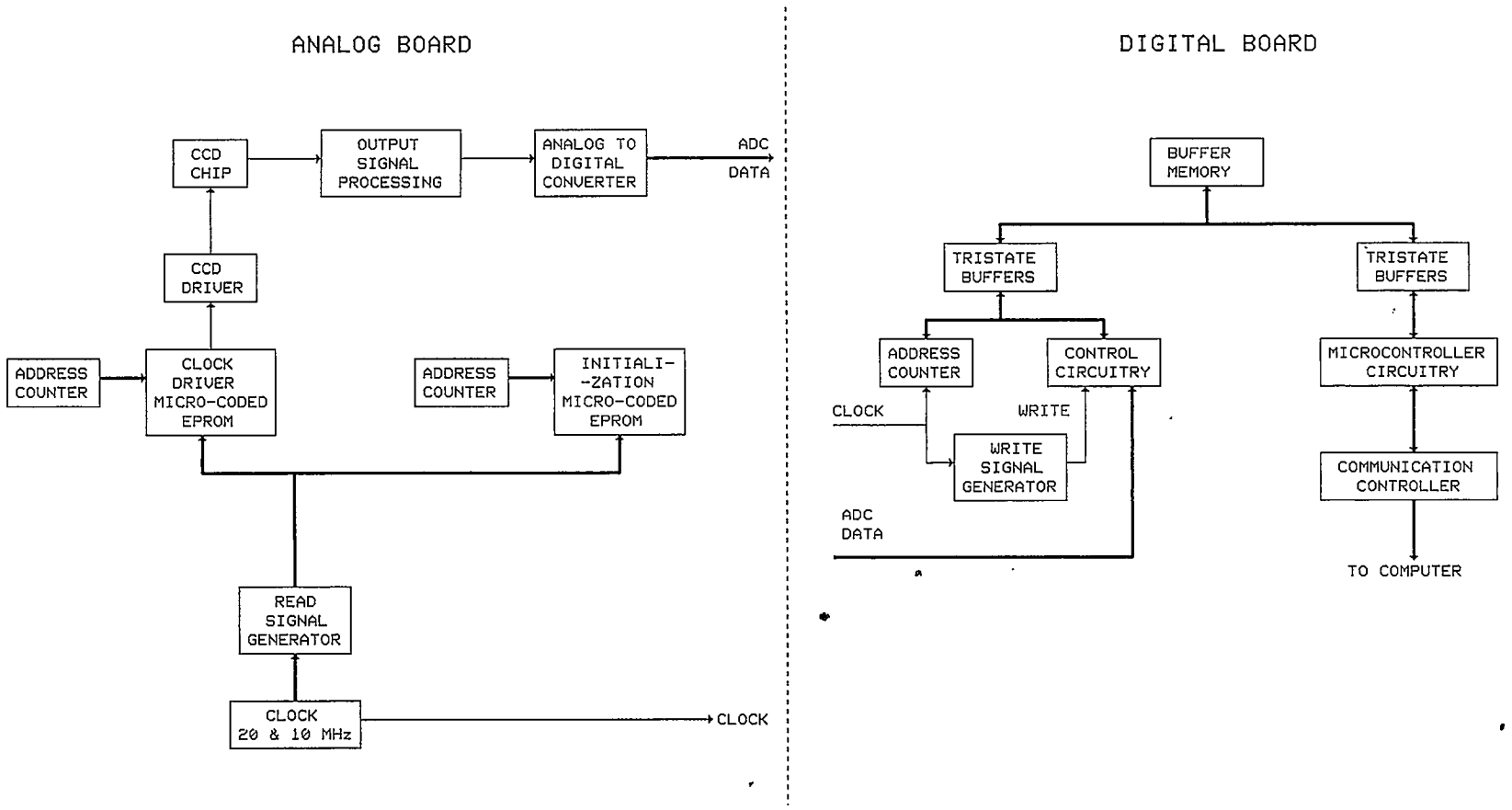

FIG. 5 BLOCK SCHEMATIC OF FIBER OPTIC SCANNER CIRCUITS

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line are dark voltage reference pixels which provides run time dark voltage reference value.

The compensated output is fed to a flash A to D converter that converts these signal continuously. The appropriate digitized output of the CCD cells that need to be latched are determined by the initialization EPROM. This EPROM determines which pixels are mapped to the fiber and need to be stored as part of the data. The latched data from the A to D converter is fed to a buffer memory for storage. The buffer memory's address and data lines are interfaced using tristate buffers. So at any time, only one source can access the memory; either scanner electronics or the microcontroller. The address counter generates the required address and a logic circuit generates the write pulses to write the data from the A to D converter to the buffer memory.

The digitized data from the CCD chip, written into the buffer memory is read by the microcontroller. Here the microcontroller is used to initialize the serial communication controller and feed the data from memory to it. The serial communication controller is used to transfer the data to a host computer e.g. PC. For communication the HDLC protocol is used. The HDLC protocol is selected because of the unlimited information field length. For the serial communication interface differential drivers are used on the scanner side and differential receivers are used on the PC side.

The system clock is running at 10 MHz. It is generated on the analog board and is provided to the digital board through buffers. The microcontroller has separate clock running at 16 MHz.

CHAPTER 3

IMAGE SENSOR CHIP

Traditionally CCD chips are being used in imaging systems. The charge coupled device, popularly known as CCD, is a charge transfer device made up of metal oxide semiconductor photodiodes.

It is made up of silicon with silicon dioxide as the dielectric and metal over the oxide. Each reverse biased photodiode, comprising one element of a linear shift register, works as a capacitor or storage well to store locally generated minority carriers. The incident light creates electron-hole pairs. The minority carriers are gathered in the storage well of a CCD element by virtue of the potential well created by depleting the semiconductor under reverse bias. With different clock voltages and proper sequence it can be read out as the information. The charge is proportional to the amount of locally incident light flux, when the CCD is used for imaging with light being the external excitation source.

The main feature of a CCD shift register is the different potential wells created due to overlapping gates of adjacent MOS devices. A CCD is capable of storing the charge and transferring it out afterwards, i.e. the CCD has the built in feature of analog delay [1]. A CCD is a simple device that can be viewed as an analog shift register made up of MOS photodiode. In each photodiode charge can be stored and transferred to an adjacent element. The charge can be introduced or transferred

electrically or optically [2]. An array of serial shift registers comprises vertical lines coupled in parallel into a horizontal shift register which reads out a line at a time in a raster mode.

3.1 Physical Device Structure of CCD

The MOS devices used to form a CCD operates in deep depletion mode. The element of a CCD, a MOS capacitor is shown in Fig. 6 [3] and is discussed in the next section. The CCD element stores the charge in potential wells. The potential wells, to store and transfer charge, are created by a multiphase clock coupled to the CCD gates.

There are two basic types of CCDs, surface channel CCDs and buried channel CCDs. In the first device, minority carriers are stored near the depleted interface of the semiconductor and the oxide i.e. charges are stored near the surface. Hence these CCDs are called surface channel charge coupled devices. A charge trapped at the silicon dioxide-silicon interface represents the main limitation of surface channel CCDs and this results in significant charge losses that can be minimised by burried channel CCDs. In burried channel CCDs the charge is stored away from the interface, in the bulk semiconductor itself, hence, these devices are called buried channel devices.

The surface channel CCDs have more charge transfer losses than burried channel device. Typically 10^{-3} losses for surface channel CCDs

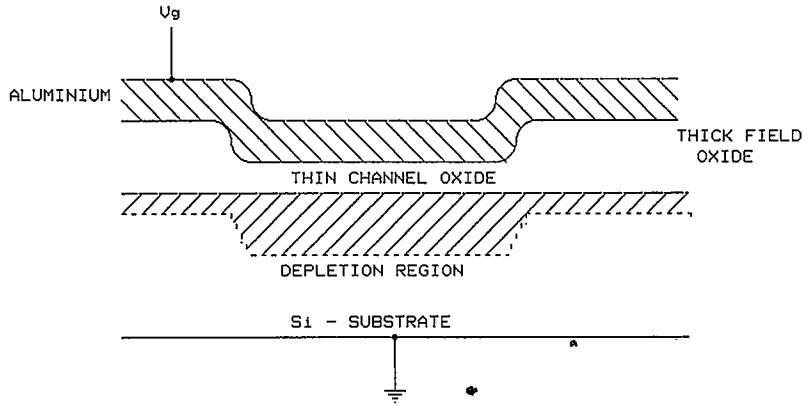

FIG.6 CROSS SECTION VIEW OF MOS CAPACITOR

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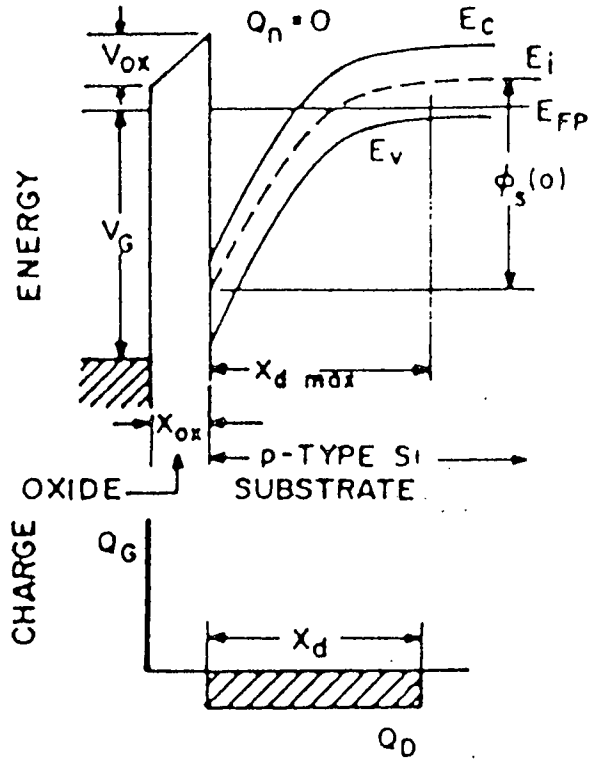
and 10^{-5} for burried channel CCDs. [1],[3]. Surface channel CCDs have higher charge handling capability per unit area.[3].

3.1.1 Cross Section view of MOS Capacitor

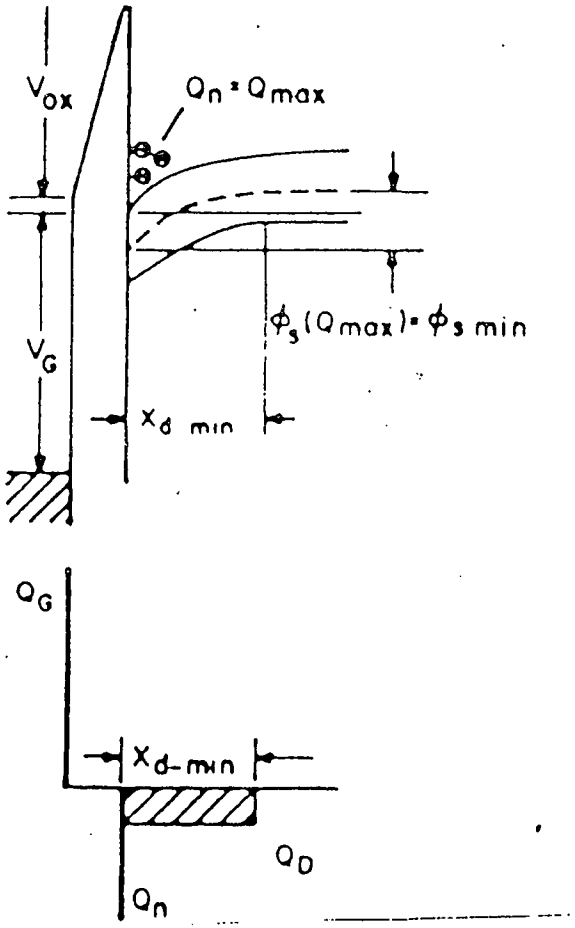
The MOS capacitor, the basic element of a surface channel CCD, shown in Fig. 6 has p-substrate. and contains thick silicon dioxide. The actual channel oxide is thin and under an aluminium metalization layer. Such a configuration is a surface channel CCD. Figure 7 shows operation of the CCD cell. The MOS capacitor in deep depletion mode indicating the curvature of the energy bands due to applied voltage. Fig. 7 shows the thermal equilibrium case of the MOS capacitor of a surface channel device in depletion mode. The potential distribution through the depleted semiconductor, indicated by the curvature of the energy bands, varies with the square of the distance from the edge of the depletion layer adjacent to the neutral semiconductor.

3.2 Device Technology of CCD Chip Used for Scanner

The CCD chip used for the scanner has different technology of fabrication. It is called virtual phase CCD technology.[5]. The virtual phase CCD technology has only one layer of metalization compared to multilayer metal layers in 2 phi technology. The use of a single gate level eliminates the possibilities of gate to gate shorts encountered in previous CCD technologies and also has the added advantage of



ENERGY DIAGRAM AND CHARGE DISTRIBUTION
FOR MOS CAPACITOR PULSED INTO DEEP DEPLETION



ENERGY DIAGRAM AND CHARGE DISTRIBUTION
FOR MOS CAPACITOR IN THERMAL EQUILIBRIUM

FIGURE 7

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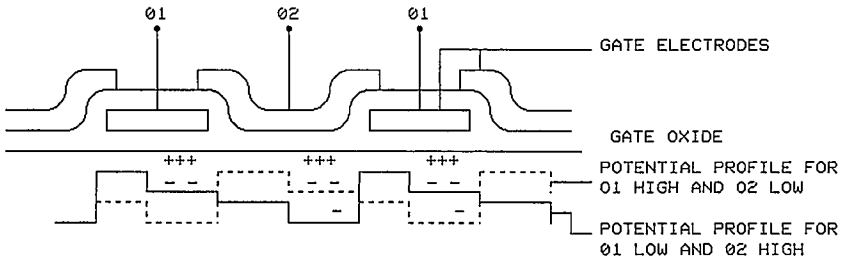
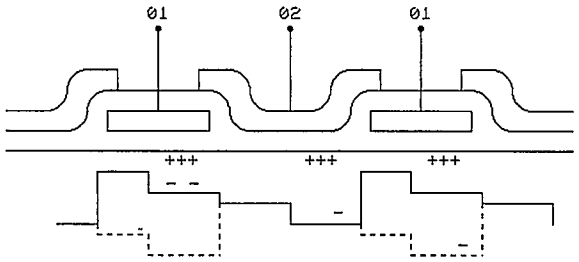
producing devices with high quantum efficiency, excellent uniformity, low dark current and blemish free imaging [5].

The 2 phase buried channel CCD cell is discussed below to explain the virtual phase technology and it has been illustrated in Fig. 8. A cross section a of two phase CCD along the charge transfer channel is shown in Fig. 8(a), together with corresponding channel potential profiles. In this design the charge transfer directionality is achieved by placing suitable implants under the portions of phase electrodes as indicated by "+" signs. These implants produce permanent potential barriers and wells which are raised and lowered by application of the appropriate voltages on the overlapping gates to provide complete unidirectional charge transfer. [5].

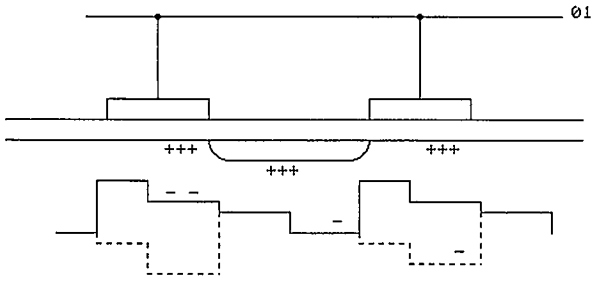
This two phase structure can be clocked by "1+1/2" phase mode. In this mode of operation one electrode is maintained at some intermediate DC potential and the other phase is clocked above and below this potential in order to accomplish charge transfer as shown in Fig 8(b). Virtual phase technology is an extension of this mode of operation of two phase device. In the virtual phase technology, however, the electrode which is maintained at the DC potential is not built above the gate dielectric as a separate structure but rather is built directly into the silicon surface and is biased at the substrate potential. The virtual phase CCD technology is shown in Fig. 8(c) [5]. The virtual phase is obtained by appropriate implant.



(a). CROSS SECTION OF A TWO PHASE CCD
USING TWO LEVEL OVERLAPPING TECHNOLOGY



(b). CROSS SECTION OF A TWO PHASE CCD
CLOCKED IN 1+1/2 PHASE MODE



(c). CROSS SECTION OF A VIRTUAL PHASE CCD
BUILT WITH A SINGLE LEVEL GATE STRUCTURE

FIGURE 8 [5]

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3.2.1 Description Of the CCD Chip Used In Scanner

The device used for the document scanner is the Texas Instruments, TC211, a virtual phase imager. Fig. 9 shows the layout of the TC211 device. It is a full frame imager with 204 horizontal elements and 165 rows. In each horizontal row there are 192 imaging pixels and 12 dark voltage reference pixels. Each CCD cell consists of clocking electrode, clocked by serial gate clock, antiblooming electrode, clocked by antiblooming clock, and virtual phase region. Antiblooming is used to get rid of the excess charge by electron-hole recombination at the silicon-silicon dioxide interface.

The output serial register is composed of 210 CCD cells. There are first six dummy cells, 192 imaging cells and last 12 dark voltage reference cells. All of the charges are moved out of the serial register to the charge detection node. This node is reset through a MOSFET that interfaces to a diode connected to an on chip reference generator. The gate of the reset MOSFET is internally connected to the serial register electrode. The charge detection node is connected to the input gate of a high performance amplifier as shown in the figure to provide output signal from the CCD cells [6].

3.2.2 Operational and Functional Description

The quantity of charge collected in each well is a linear function of the product of the locally incident light intensity and the exposure or

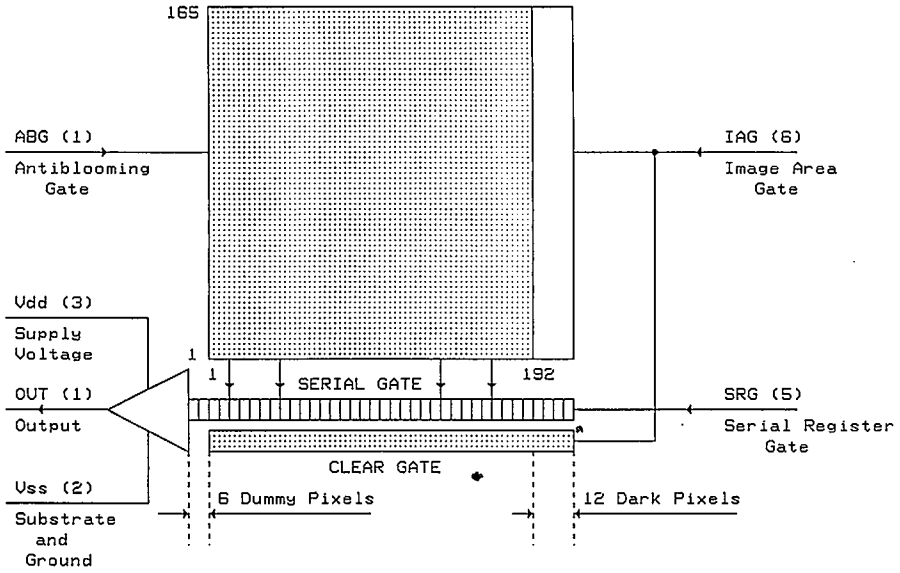

Fig.9 Functional Diagram of TC211

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integration time, that is, the light flux. After exposure and under dark condition, the charge packets are transferred from the image area to serial register one row at a time with each clock pulse applied to the image area gate.

Every pulse at the image area gate causes an automatic fast clear of the serial register before the next row of charges is transferred in. After a row of charge packets is transferred to the serial register, the serial register gate may be clocked until all the charges are moved out of the serial register to the charge detection node at the input of the built in amplifier. The automatic fast clear feature can be used to initialize the image area by transferring all 165 rows to the serial register gate under dark conditions without clocking the serial register gate.

The CCD chip requires serial register gate clock, image area gate clock and antiblooming clock for it's operation. The timing diagrams of these clocks are shown in Fig. 10. This figure also gives the recommended timing conditions and the actual timing diagrams for all the clocks used in the scanner.

Fig. 11 explains the timing conditions for reading the CCD cells. This diagram shows the typical serial gate clock and the CCD output waveform. The actual output waveform with the serial gate clock is shown in Fig. 11. Data sheets for the Texas Instruments CCD chip TC 211 is included in appendix 1.

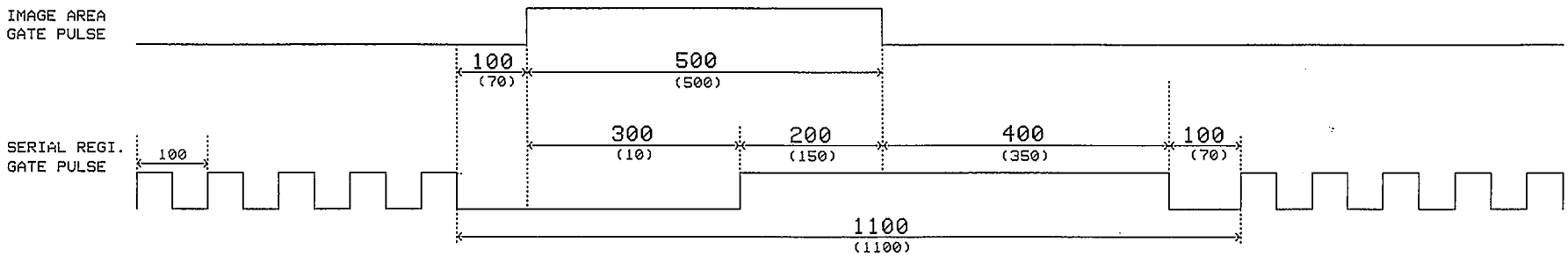

FIG. 10 TIMING DIAGRAMS OF CCD CLOCKS

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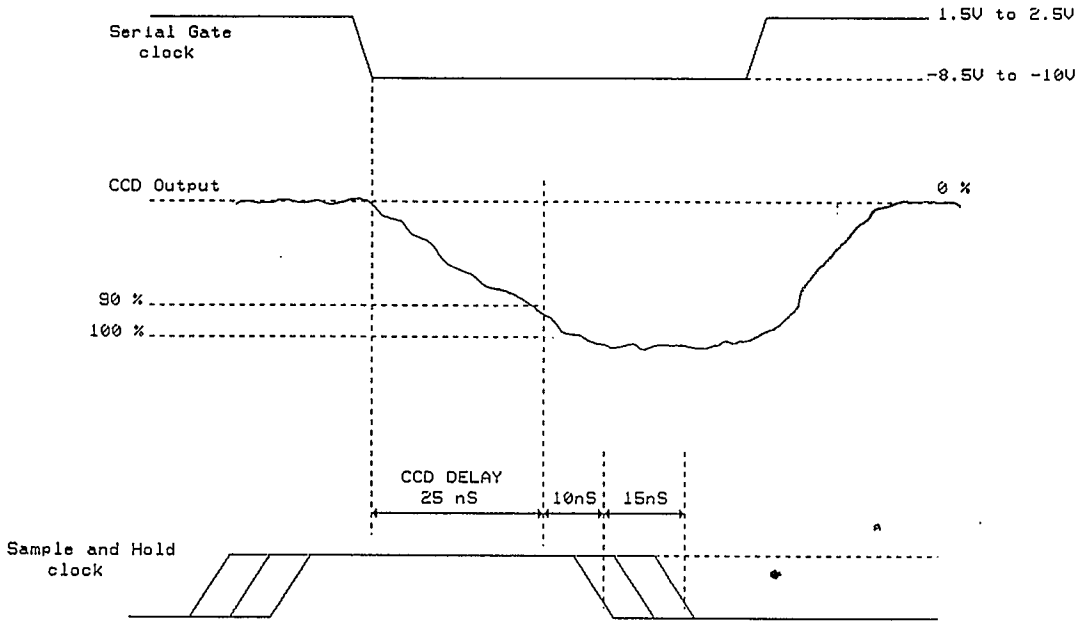

FIG.11 Typical SRG and CCD output Waveform

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This chip has one feature that distinguishes it from other CCD imagers, with frame memory, used in conventional video cameras. The later integrates the photo-excited charge in cells that are not part of the read out shift register. This charge can be shifted rapidly into the readout shift register which is not exposed to light. Thus the light flux may be continuously integrated. That is not the case with this TI device. The photosensitive cells and the shift register cells are the same. The resultant simplicity makes the device less expensive and faster. However, the device can not be read out while light is falling on it because smearing results. In this application the line being read is stationary when the CCD chip is integrated with light. The line on the paper is illuminated by a light pulse. The CCD chip is read when the paper is not illuminated. Hence this device is ideal for this application.

CHAPTER 4

DESIGN CONSIDERATION FOR CCD CAMERA FOR THE SCANNER

In this chapter the design of the analog and digital circuits for a CCD based scanner are explained. The scanner circuitry could also be employed as a camera where the information from every pixel is stored in a buffer memory. The output from the CCD is digitized with the help of flash analog to digital converter and stored in the device's memory. This digital data is transmitted serially to a PC for storage and display. As a 300 dpi (gray scale) scanner is desired, 300 x 11 = 33000 lines per page are scanned and stored.

4.1 Introduction To Circuits Used In the Scanner

The basic block diagram of the scanner is shown in Fig. 4. The system consists of a CCD camera, made up of a TI CCD chip and it's driver, flash analog to digital converter, buffer memory, microcontroller, microcoded ROM and address counters. In the scanner configuration the CCD output is clocked at a speed of 10MHz. The CCD also requires an image area gate clock i.e. line clock and antiblooming clock which is generated by the CCD driver block. It contains micro coded ROM, address counter and clock generation circuitry. The serial gate and image area gate clocks are generated using discrete devices and the antiblooming clock is generated using analog switches.

The output of the CCD chip is provided to the output processing block for dark current compensation. Hence, the output of this block contains a CCD output level proportional to the amount of light exposure. This signal is then fed to a flash analog to digital converter which converts the signal at 10MHz rate. The output of the A/D converter goes to a buffer memory. The addresses for the memory are generated by either the address counter or the microcontroller, depending upon the phase of operation.

The operation of the system is divided into two phases. In phase 1 the CCD is exposed to light and integrated and then the charge is shifted out. In phase 1 the addresses for buffer memory are generated by the scanner's address counter. The write signal for the memory is derived from the system clock by a small circuit. In phase 2, the data stored in buffer memory is transmitted out via UART to the memory of the PC.

In phase 2 high speed serial communication between the scanner's buffer memory and the PC's memory takes place using the HDLC protocol. In phase 2 the microcontroller in the scanner initiates the communication and the output of address counters used in phase 1 are tristated. A PC plug in card from Quatech is used for communication. When all the data in buffer memory is transmitted, the microcontroller gives the signal to start phase 1, to read the next line sequentially and to fill up the data in buffer memory. This process repeats itself every time to capture one frame of image.

In the following paragraphs the operation of the scanner circuits and the circuit diagrams are explained in detail.

4.2 CCD Chip And It's Driving Circuits

The CCD chip and it's driver circuit diagram are shown in Fig 13. It requires three clock signals for it's serial gate, image area gate and antiblooming gate. The serial gate is clocked at a rate of 10MHz. Consequently the output from the serial gate register are clocked out at 10MHz. The serial gate clock has a bias range of +2V to -9.5V. This clock is generated using a fast PNP switching transistor, 2N5771. The base of this transistor is driven by a TTL level signal from micro coded ROM (IC 50, Fig. 14), called driver ROM. The Serial gate clock is used to output the pixel data from the CCD. A total of 204 clock pulses are required per line to read all CCD elements in a line.

The image area gate which acts as a line clock, operates at a speed of 45KHz. It is generated using a fast switching PNP transistor, 2N5771 which is driven by the driver ROM. This clock loads the output of the serial register data of the next line. Hence, 165 pulses are provided in one frame. This clock operates at a voltage range of +1V to -9.5V.

When the CCD is exposed to intense light, the CCD charge wells may become overfilled and the charge may be spilled over onto

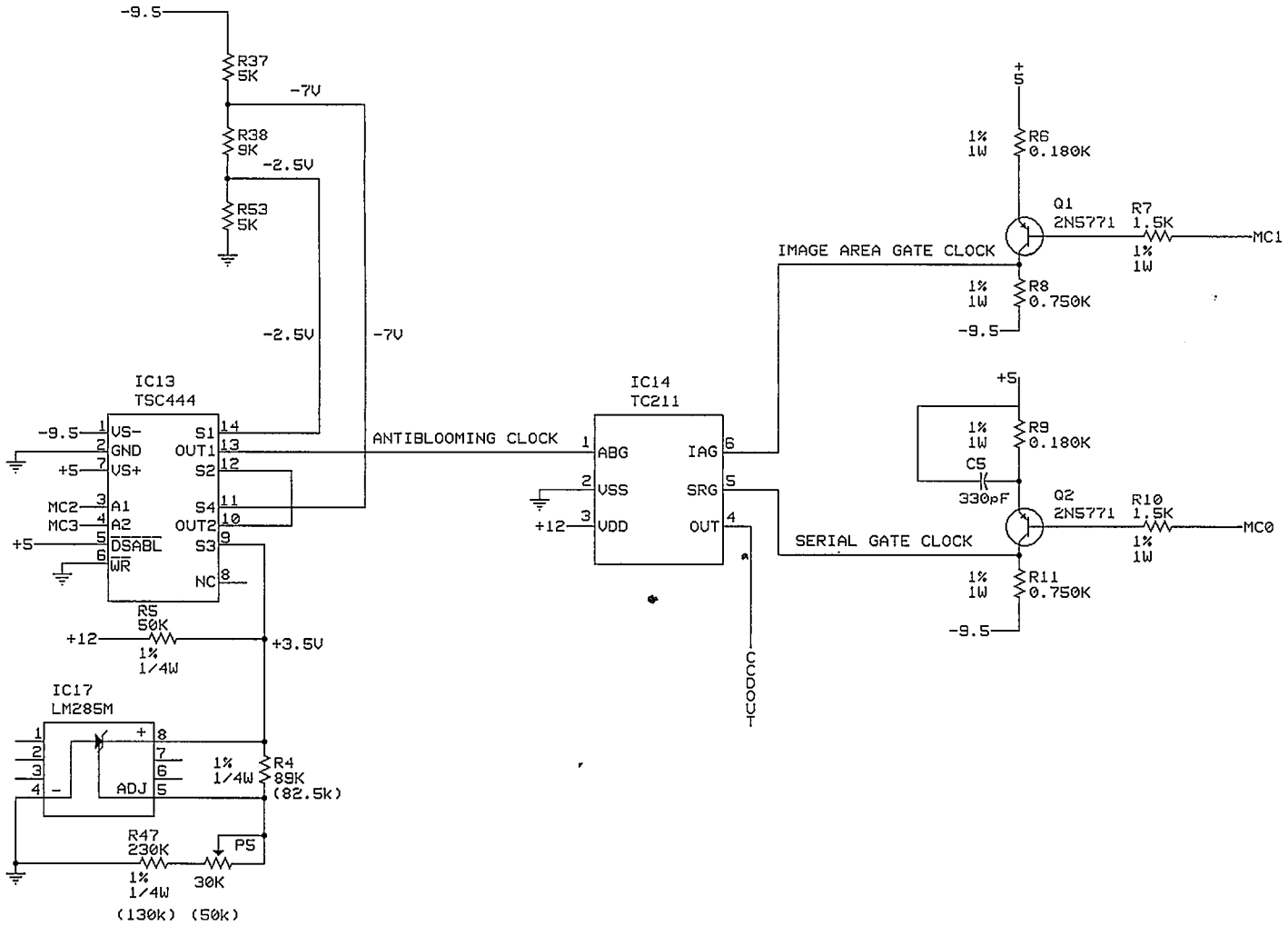

FIGURE 13

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adjacent pixels. To avoid this, antiblooming operation is used. In the scanner (and camera) 100KHz signal is used as antiblooming clock. When the CCD is read, the antiblooming clock is left at an intermediate level. The antiblooming clock is generated using analog switch and voltage divider. The required negative voltages are generated using negative voltage regulator, LM337, and a metal film resistor divider and analog switch TSC444 from Teledyne semiconductor is used to switch the different voltage levels for antiblooming. The selection of the switches is done by micro coded ROM bits. As antiblooming requires three different voltage levels, an analog switch is used.

The positive voltage required for the antiblooming clock is generated by using variable voltage zener LM285BXZ from National Semiconductor. The antiblooming signal requires +3.5V to -7V alternating voltage levels when the CCD is integrating light and -2.5V for intermediate voltage level when the CCD is read.

4.3 Digital Clock Drivers For CCD

The digital clock driver circuits are shown in Fig.14. Various clocks for the CCD chip are described above. The control signals for these clocks are derived from a micro coded driver ROM. The ROM used is HC27C64 EPROM from Hitachi Semiconductors (IC # 50, Fig. 14) with 80 nSec. access time. The micro coded ROM contains information of the serial bit pattern which represents the actual clocks required for the CCD for one row. The same clock pattern is repeated

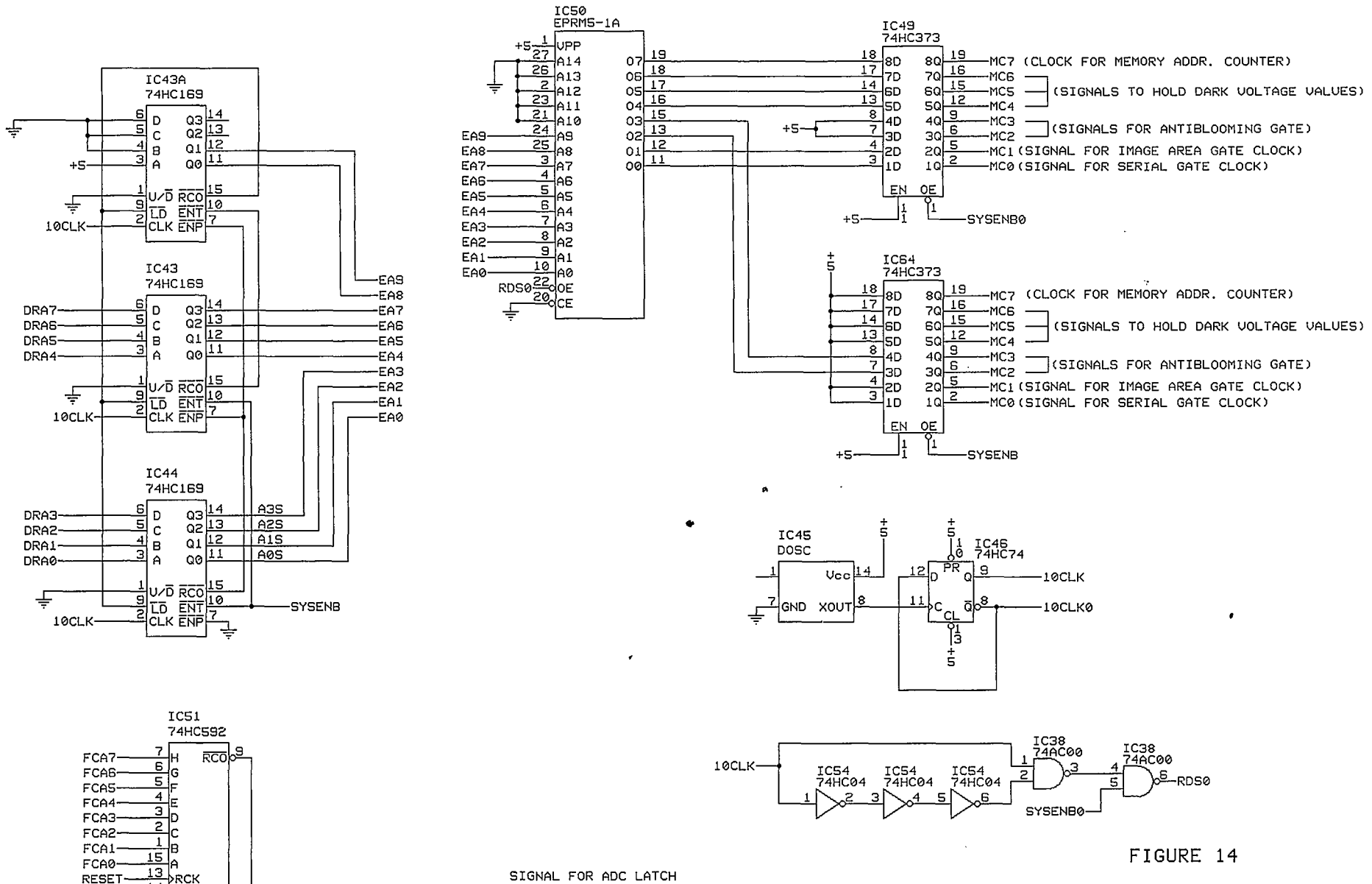

FIGURE 14

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every row. Consequently, this ROM is read 165 times as there are 165 lines in one frame. The ROM bits are used as follows :

MC0 is used for serial gate clock signal
MC1 is used for image area gate clock signal
MC2 and MC3 are used for antiblooming signal
MC4, MC5 and MC6 are used as control signal for the sample and hold circuit

The driver ROM also contains a signal to control the sample and hold circuits. At the end of every line three signals are generated to sample and hold the dark signal value as reference for the next line. The driver ROM has 8 bit presettable address counter (IC # 43 & 44, Fig. 14) that generates 204 clock patterns per row. The Read signal for driver ROM is generated using a small logic circuit shown in Fig. 14. A presettable down counter, called line counter is used for counting the number of rows (IC # 51, Fig. 14). It counts 165 rows per frame and generates frame end signal (FRMEND) at the end of a frame.

The circuit diagram is shown in Fig 14. In the scanner implementation an initialization ROM is used to select the appropriate mapped pixels. The mapped pixel are the 2550 pixels per CCD frame that contain useful information which corresponds to the resolution of 300 dpi. The mapped pixel means pixel mapped to a fiber at the square end of the fiber bundle. The initialization micro coded ROM is 32 KByte deep (IC # 87, Fig. 15). Select pixel signal (SELPIX) is used to choose the mapped pixel and is also used to store that pixel in to the buffer

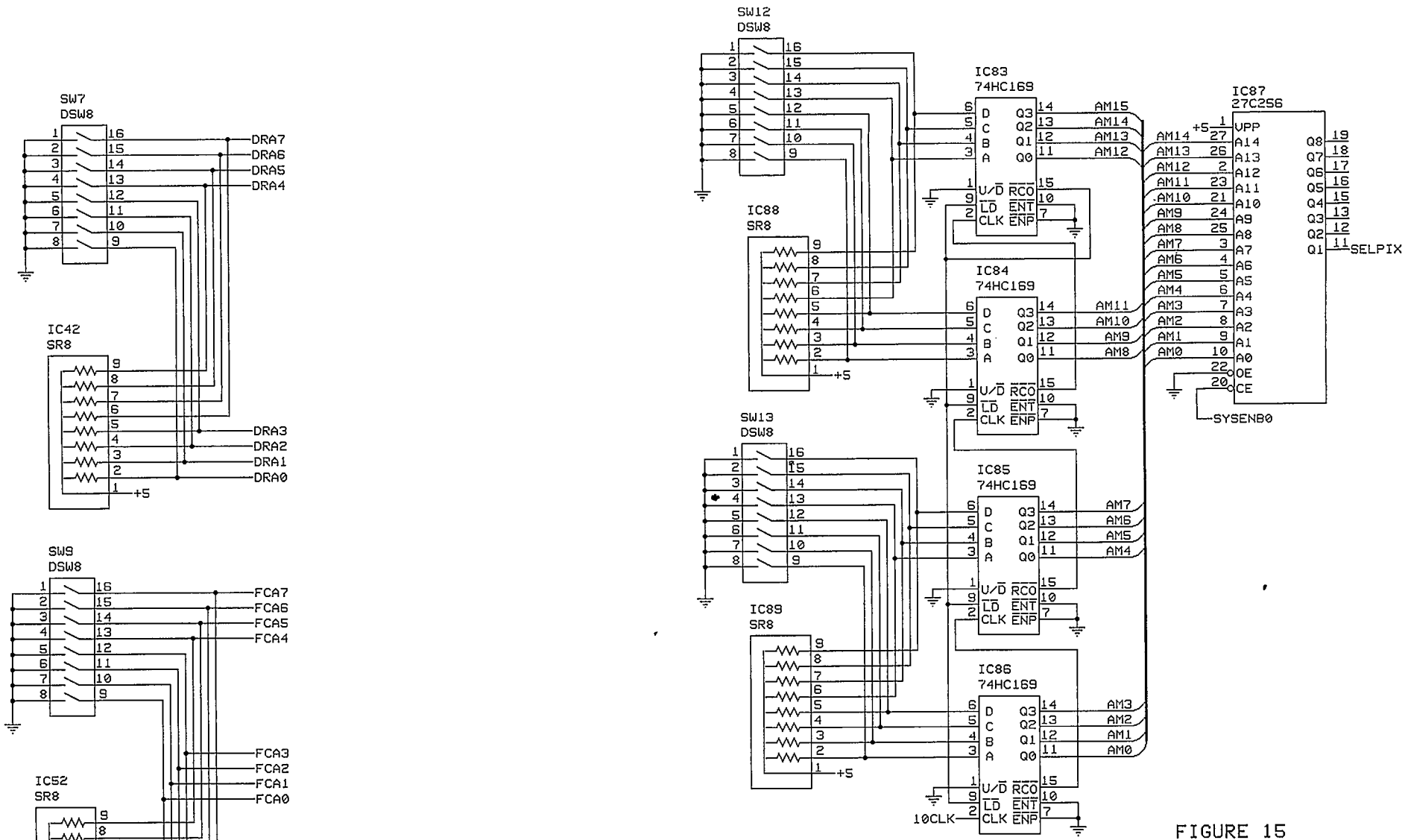

FIGURE 15

PHOTON IMAGING CORP.

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memory. The circuit diagram is shown in Fig. 15. The initialization ROM is clocked by 16 bit binary presettable down counter (IC # 83 thru 87, Fig. 15).

4.4 Processing Of CCD Output Signal

The circuit diagram for the output signal processing is shown in Fig. 16. The output of the CCD is fed to fast settling op amp that compensates for the dark voltage signal. To do this, a sample and hold circuit TL1593 from Texas Instruments (IC #21, FIG. 16), is being used. It has three sample and hold circuits. The last 12 pixels in each CCD row are the reference dark cells. In the scanner implementation three dark pixel's data are stored in the sample and hold circuit. The control signal that samples the dark pixel's data is generated in the driver ROM. Acquisition time of the sample and hold circuit is 50nS, hence, first, third, and fifth dark pixel values are sampled and held. Consequently, these values are added with the help of the AD5539 an operational amplifier (IC # 19, Fig. 16) which is configured as an unity gain amplifier to provide a real time dark signal for the CCD output compensation.

The circuit also contains an option for a fixed dark signal reference that compensates equally for all pixels. The output of the CCD and inverted dark signal voltage from the unity gain buffer are added with the help of a fast settling op amp. AD5539 from Analog Devices (IC # 20, Fig. 6). This op amp. configuration has a gain of 2

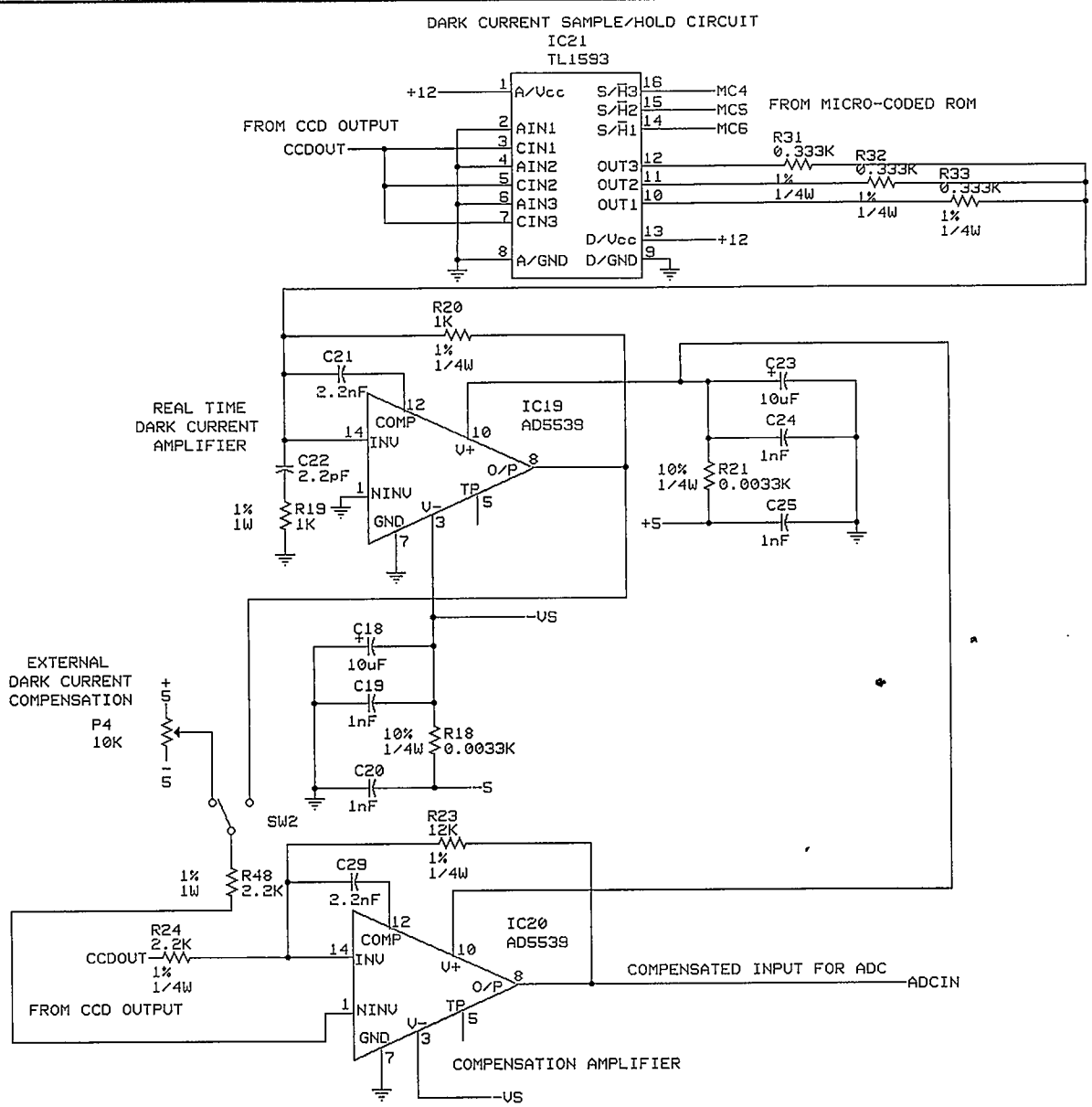

FIGURE 16

PHOTON IMAGING CORP.		
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and is compensated externally for stability with lead-lag network. Hence, the output of this stage varies between 0 - 2V according to intensity of the light and the exposure time light for the CCD chip. This signal is fed to the analog to digital converter.

4.5 Analog To Digital Converter Circuit

The analog to digital converter circuit diagram is shown in Fig 17. Dark current compensated output from the op amp. is fed to a 8 bit flash A to D converter from Motorola, MC10319 (IC. # 32, Fig. 17). The voltage reference for the ADC is generated using a variable voltage Zener LM285BXZ from National Semiconductor. It is configured in a fixed voltage reference mode with the help of metal film resistors to get a stable voltage reference. The compensated CCD output from the op amp. is in the range of 0 - 2V. Hence, the reference for the ADC is adjusted at 2V. The negative reference is grounded as the output of CCD varies in 0 - 2 V. The ADC is converting at a rate of 10MHz.

The output of the ADC is enabled only when the scanner system is in phase 1 and the output is tristated in phase 2. The Digitized data from the ADC is taken to a buffer memory through eight bit parallel bus which uses buffer (IC # 80, Fig 18). This is because the CCD, it's driver, output processing circuit, and the ADC are on the analog board, and all other digital circuits are located on a separate digital board. The communication between these two boards is handled via buffers which can handle the data rate at 10MBits per second. Figure 18 shows the

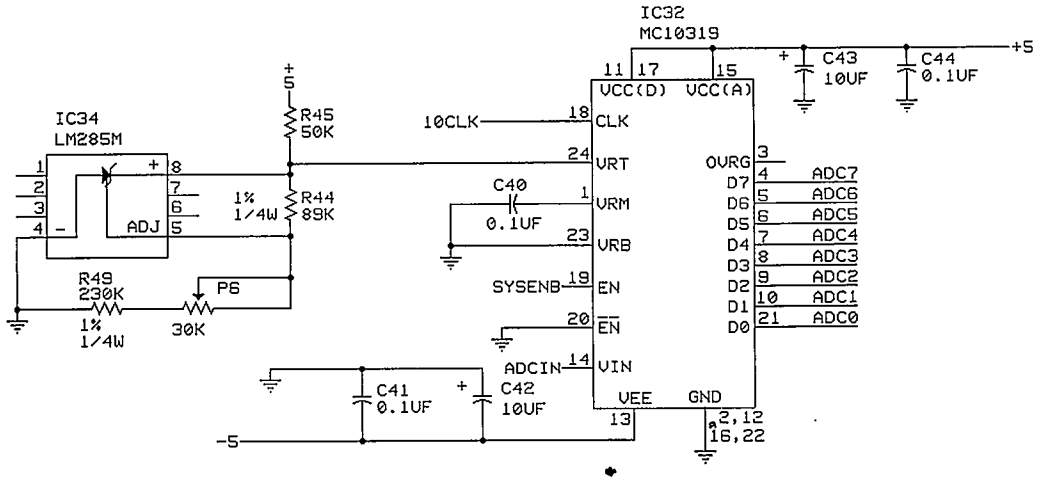

FIGURE 17

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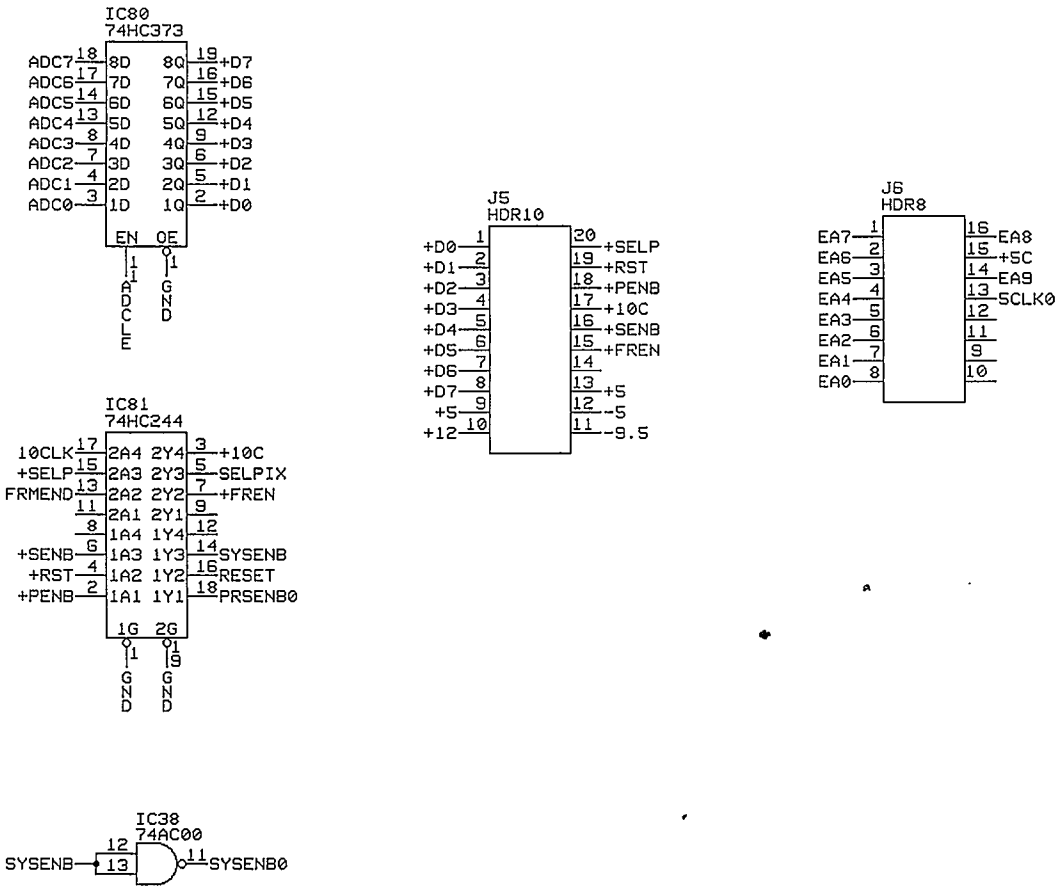

FIGURE 18

PHOTON IMAGING CORP.		
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connector pinout and the buffers used between the analog and digital boards.

4.6 Microcontroller And Its Related Circuits

The microcontroller circuit diagram is shown in Fig. 19. The scanner implementation uses a 87C51 Intel microcontroller (IC # 1, Fig. 19) which is basically used to initialize the UART and to load the data from the buffer memory to the UART for communication. The address and data bus of the microcontroller are passed through tristate buffers, so that when the scanner is in phase 1, the microcontroller buses are tristated.

During phase 2 the microcontroller is actively in control. The address and data buses are enabled by the scanner enable signal (SYSENB). The microcontroller is clocked at a speed of 8MHz. The microcontroller generates signal from port 0, bit 0, called processor enable (PRSENB0) which is used to generate signal SYSENB. Port 0 bit 1 and 3 are used to initialize the counters used in scanner for address generation for memory. Port 0, bit 2 is used to detect FRMEND signal. The SYSENB signal is used to choose between phase 1 or phase 2. The buffer memory used is 32k x 8 bit wide static CMOS RAM (IC # 35 Fig. 19). It has access time of 85nSec which is fast enough for this purpose. In phase 2 the read signal and addresses for the buffer memory are generated by the microcontroller.

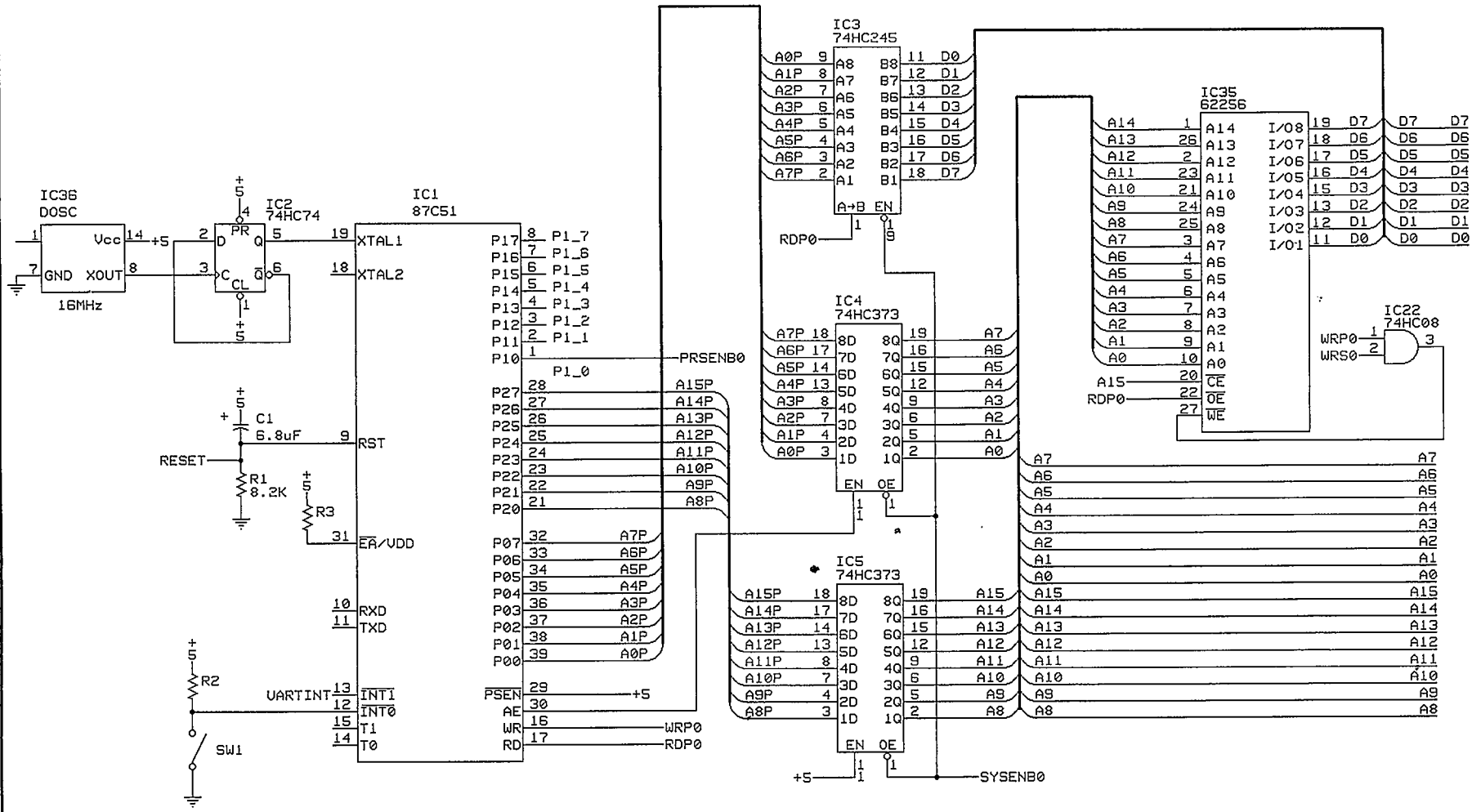

FIGURE 19

PHOTON IMAGING CORP.

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In phase 1, 16 bit address counter is used to generate address using four, 4 bit binary presettable down counters (IC # 6 thru 11, Fig. 20). The address bits go through tristatable buffers so that they can be tristated in phase 2. The write signal for the RAM is generated using small logic circuit which is shown in Fig29. To generate the write signal AHCT-series logic chips are used as they have less propagation delay. The counter from the microcontroller is used in serial communication. It counts the number of bytes transferred and after transferring all the data it interrupts the microcontroller to stop transferring data and switch to phase 1.

4.7 Serial Communication Controller

The diagram of the serial communication controller circuit is shown in Fig. 21. The scanner uses a UART for the serial communication. The UART being used is the uPD7201A from NEC Electronics, (IC # 12A, Fig. 21). It communicates up to 1Mbits per second with the PC plug in board from Quatech. The protocol used for communication is HDLC with a start flag, address field, information field and a stop flag. HDLC protocol is chosen because of the unlimited length of information field. The length of the information field depends on the receiver buffer size. For communication link RS422 differential drivers and receivers from Advanced Micro Devices are being used (IC # 55 & 56 Fig. 21). The buffers are used as receivers for receiving signals from the analog board (IC # 81 & 82, Fig. 22). Figure 22 also shows the

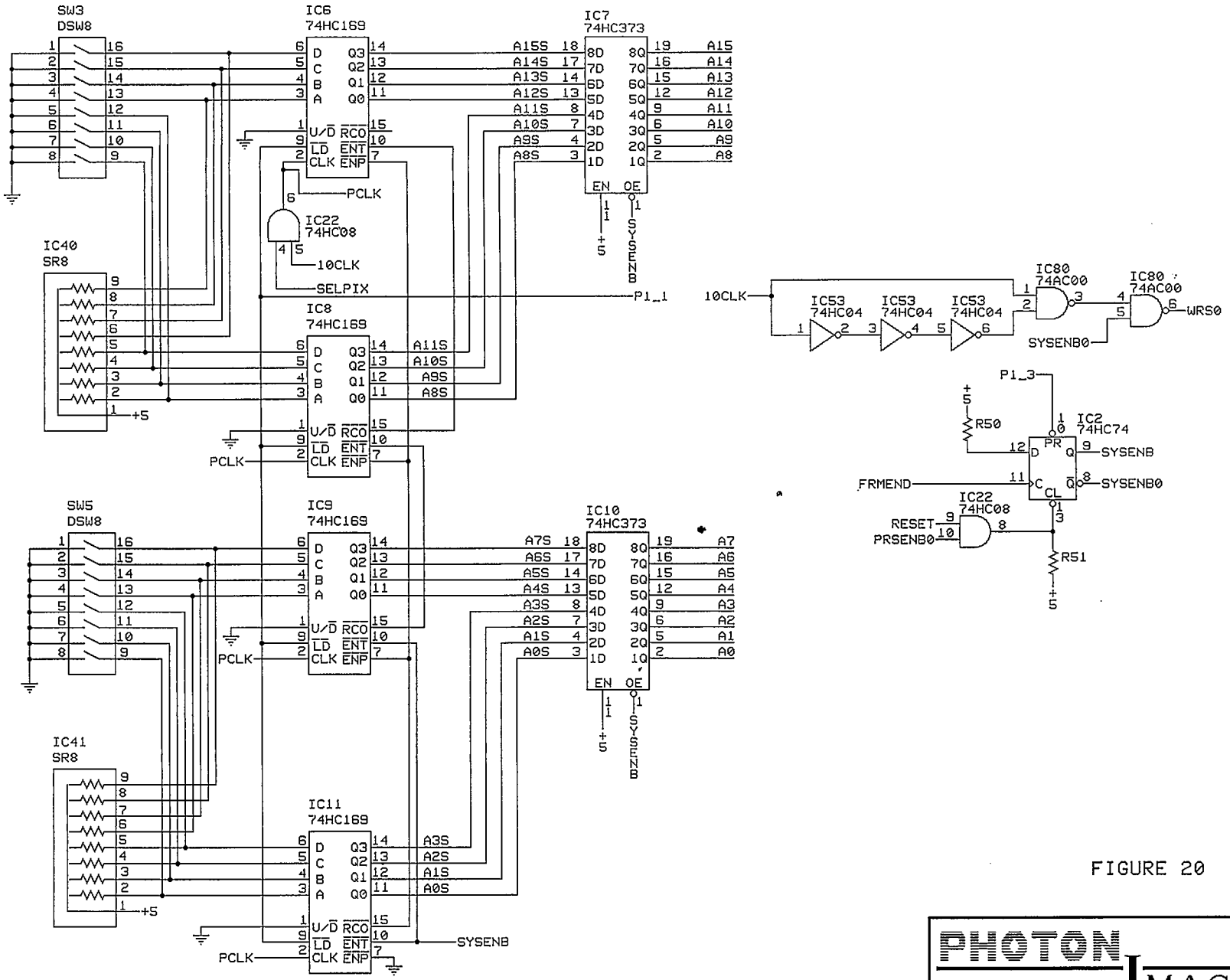

FIGURE 20

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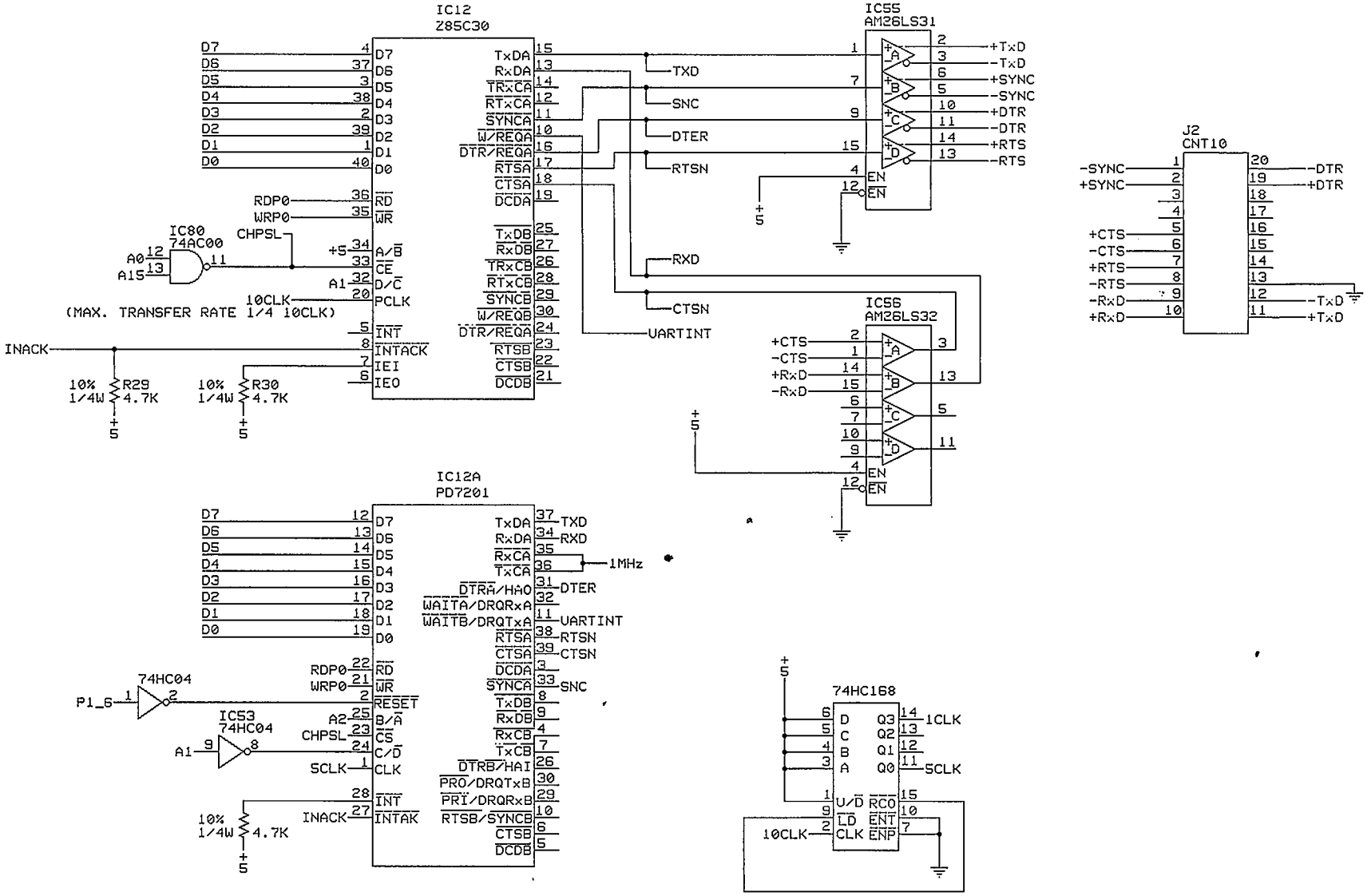

FIGURE 21

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header pinout for the connector. It also shows the different power supplies for the system (IC # 24, 15, 16 & 59 Fig. 22).

4.8 Light Source For Scanner

The light source for the scanner is a single bright LED HLMP4100 from Hewlett Packard. The LED is driven by SYSENB, system enable signal. It is turned ON when the scanner is in phase 1 and is turned OFF to prevent the CCD from integrating while reading.

4.9 Timing Diagrams

The timing diagram of memory read/write cycle is shown in Fig. 23. The Read/write signals are generated using AHCT series logic and propagation of HC devices. HC series devices are used as limited delay line.

4.10 Timing Consideration For Scanner

In the scanner configuration 198 pixels are read per row, including dark pixels , so the time required is 19.800 microSec. per row. The CCD chip requires 1100 nSec between two rows, so the total time required per line is 20.9 microSec. As there are 165 lines, the time to read a complete frame for reading is 3.449 mSec. The paper is

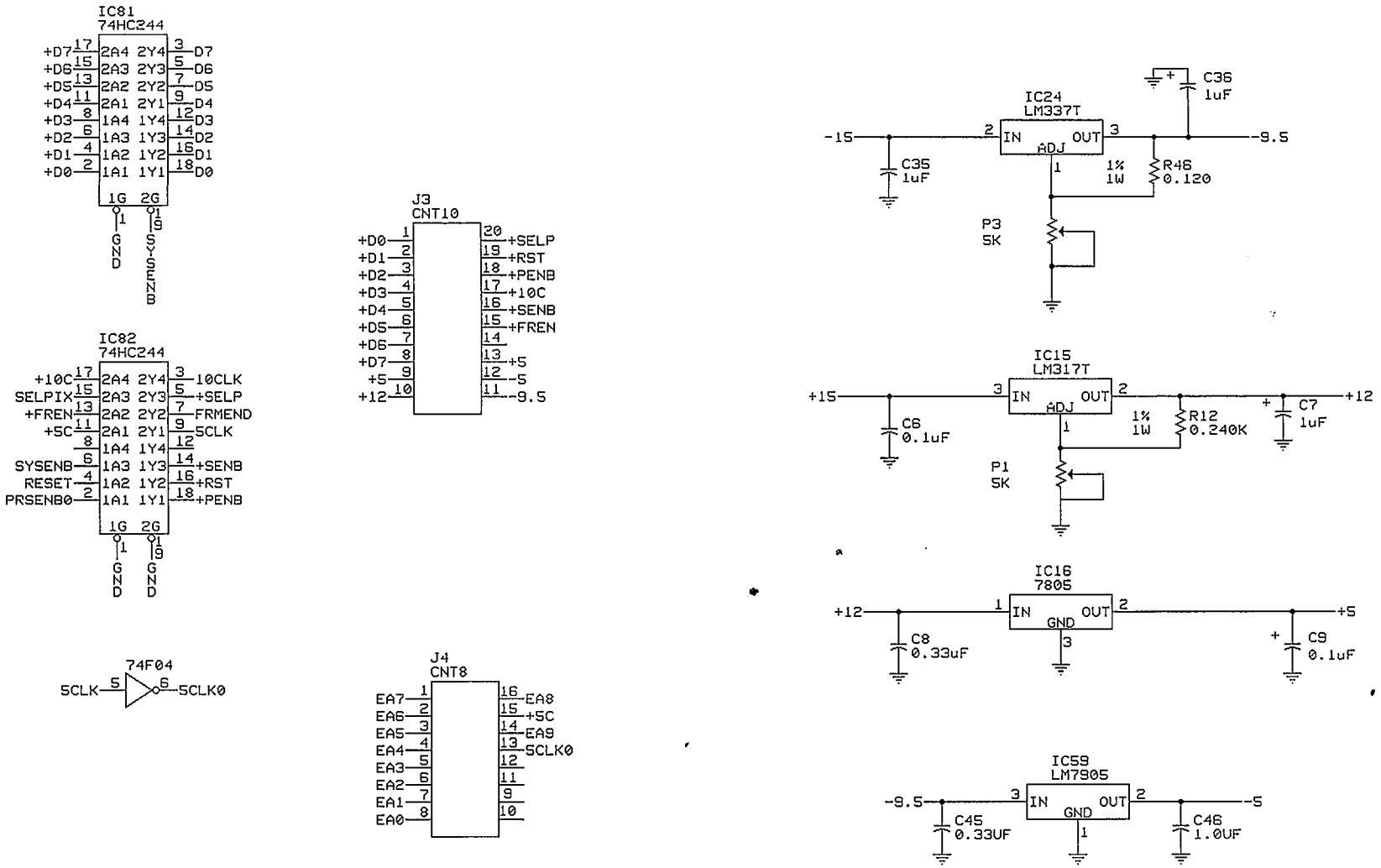

FIGURE 22

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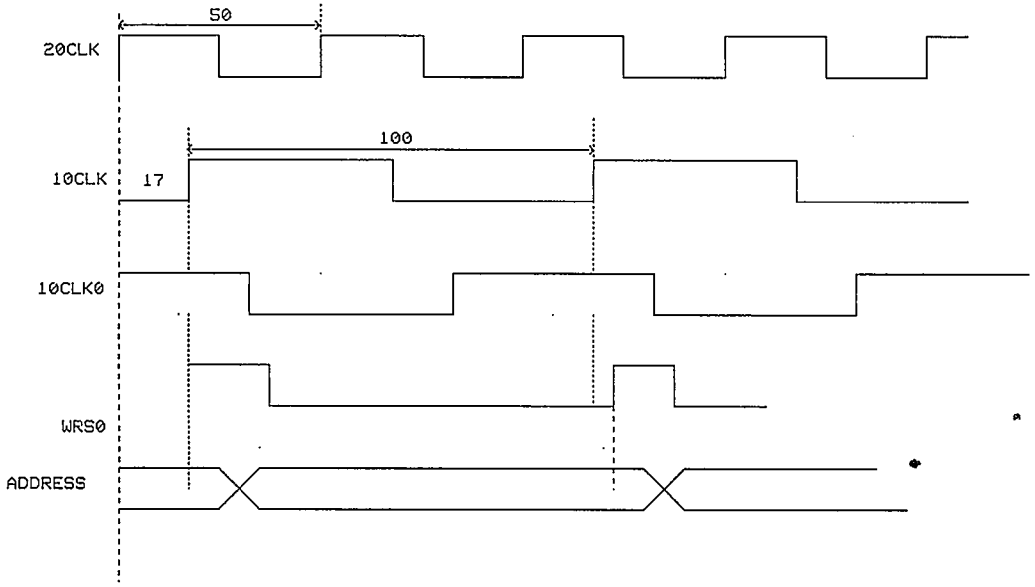
shifted during this time. With a nominal integration time for the CCD is 3 mSec, total time per frame is 6.449 mSec.



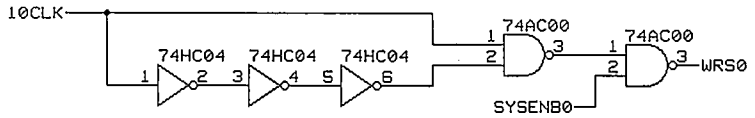


FIG.23 MEMORY WRITE CYCLE IN SCANNER

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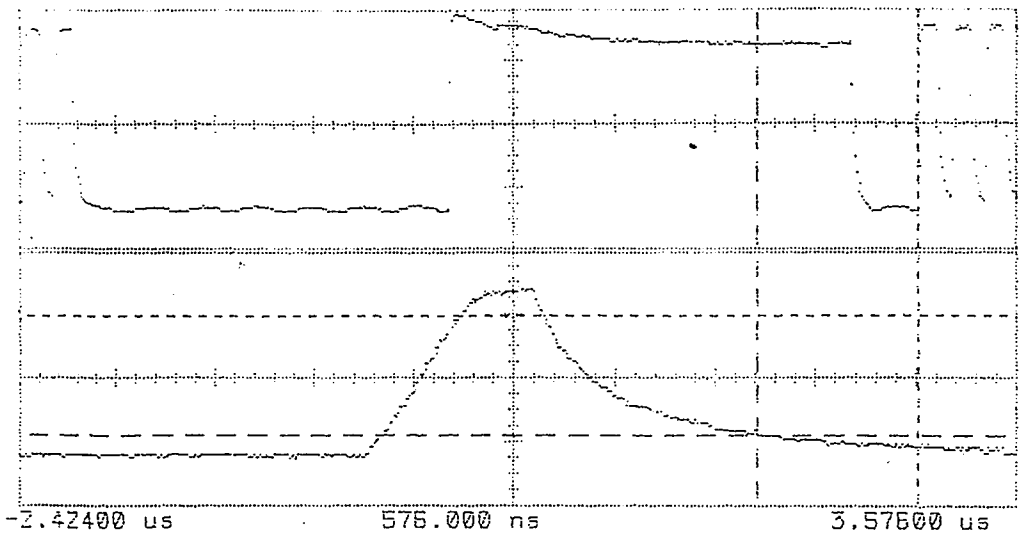
CHAPTER 5

DEMONSTRATION OF THE OPERATION OF THE CCD CAMERA

The demonstration of the operation of the CCD camera designed for document scanner is shown in Figs. 24, 25, 26 and 27. These figures are the actual waveforms from the camera circuits.

The serial gate clock and image area gate clock are shown in Fig. 24. It shows the image area gate clock which transfers the charges from the line of the image area to the serial shift register. The serial clock pulses shift it to the output amplifier. The output of the CCD cell with the serial gate clock is shown in Fig. 25. It shows typical CCD cell output.

The dark current compensated CCD output, which is fed to the A to D converter and clock for the A to D converter is shown in Fig. 26. Every falling edge of this clock samples the input and A to D converter digitizes the input. The output of the A to D converter of the previous sample is latched into latch with falling edge of the A to D latch pulse shown in Fig. 27. Write pulse for the buffer memory is also shown in Fig. 27. The latched data from the A to D converter is written into the buffer memory with this pulse.

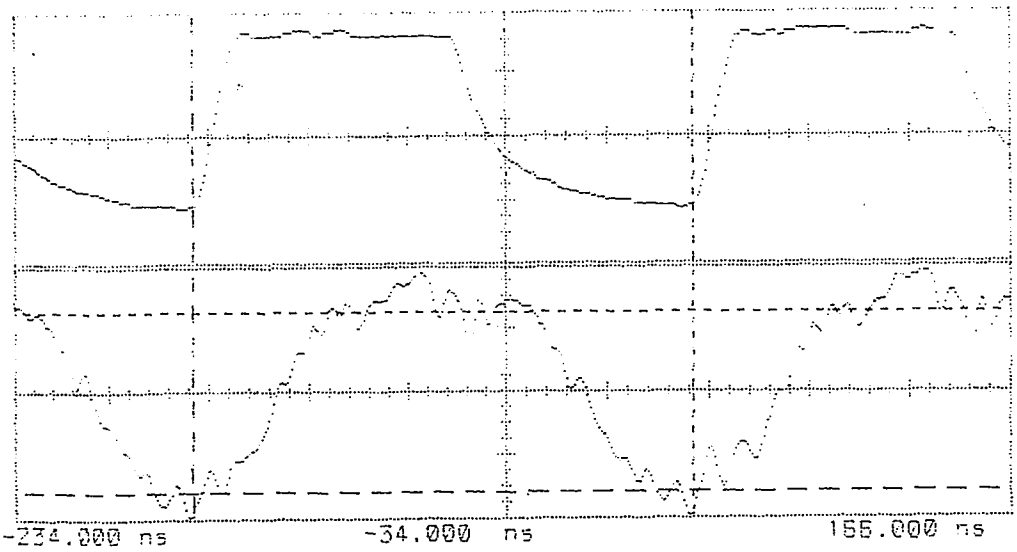


Channel 2 = 4.000 Volts/div
Channel 3 = 4.000 Volts/div
Timebase = 600 ns/div

Offset = -3.900 Volts
Offset = -3.400 Volts
Delay = 576.000 ns

Delta T = 960.000 ns
Start = 2.02800 us
Stop = 2.98800 us
Delta V = 7.500 Volts
Vmarker1 = -7.500 Volts
Vmarker2 = 0.000 Volts

Trigger mode : Edge
On Pos. Edge on Channel 2
Trigger Levels
Channel 2 = -3.900 Volts



SERIAL GATE CLOCK

CCD CELL OUTPUT

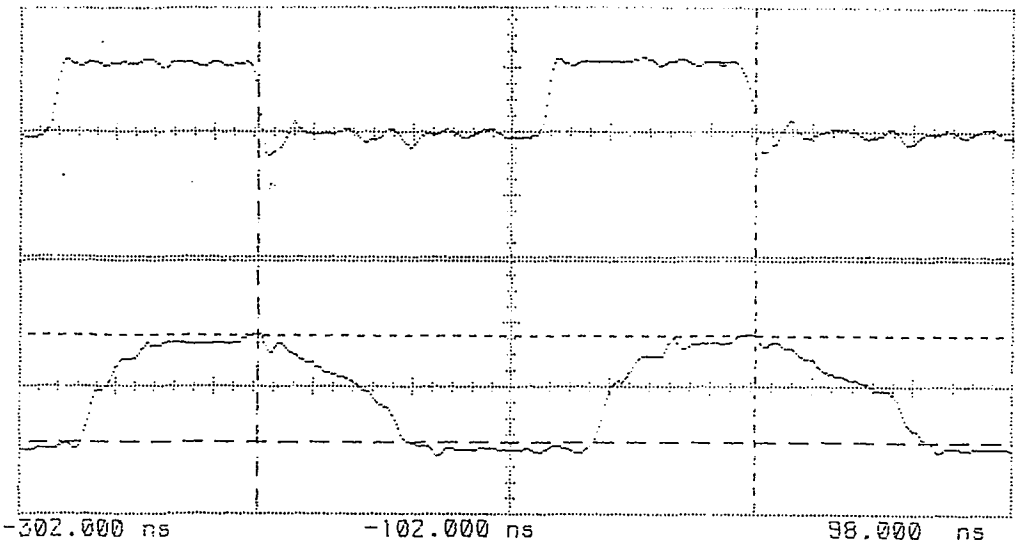
Channel 2 = 250.0 mVolts/div
Channel 3 = 4.000 Volts/div
Timebase = 40.0 ns/div

Offset = 1.720 Volts
Offset = -3.500 Volts
Delay = -34.000 ns

Delta T = 200.000 ns
Start = -160.000 ns
Delta V = 707.5 mVolts
Vmarker1 = 1.325 Volts

Stop = 40.000 ns
Vmarker2 = 2.032 Volts

Trigger mode : Edge
On Neg. Edge on Channel 2
Trigger Levels
Channel 2 = 1.720 Volts



A/D CONVERTER CLOCK

DARK CURRENT COMPENSATED CCD OUTPUT.

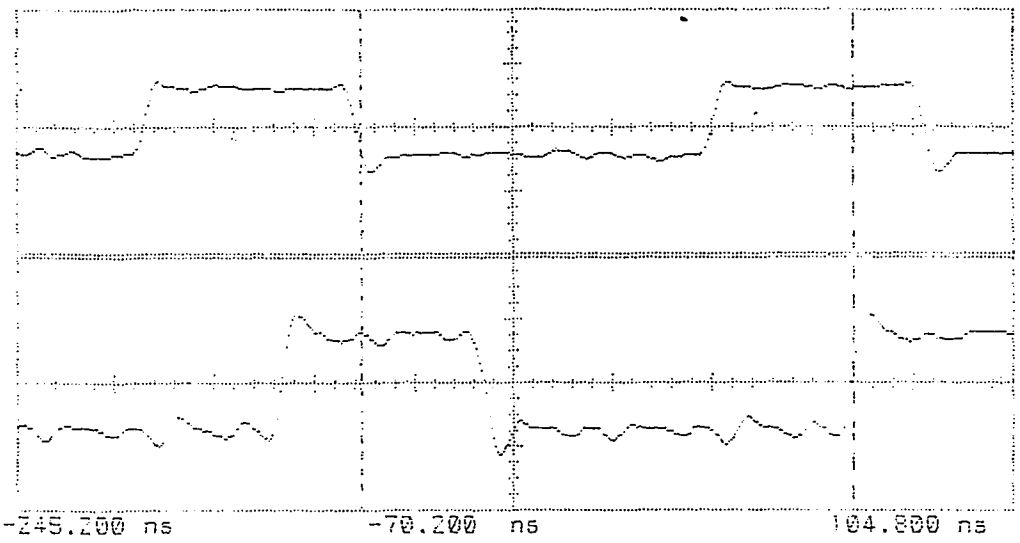
Channel 2 = 1.200 Volts/div
Channel 3 = 4.000 Volts/div
Timebase = 40.0 ns/div

Offset = 1.050 Volts
Offset = 0.000 Volts
Delay = -102.000 ns

Delta T = 300.000 ns
Start = -204.000 ns
Delta V = 2.004 Volts
Vmarker1 = 0.000 Volts

Stop = -4.000 ns
Vmarker2 = 2.004 Volts

Trigger mode : Edge
On Neg. Edge on Channel 2
Trigger Levels
Channel 2 = 1.720 Volts



A/D CONVERTER LATCH CLOCK

WRITE PULSE FOR BUFFER MEMORY

Channel 1 = 4.000 Volts/div
Channel 4 = 400.0 mVolts/div
Timebase = 35.0 ns/div

Offset = 1.500 Volts
Offset = 250.0 mVolts
Delay = -70.200 ns

Delta T = -173.000 ns
Start = 49.000 ns

Stop = -124.000 ns

Trigger mode : Edge
On Pos. Edge on Channel 1
Trigger Levels
Channel 1 = 1.500 Volts

CHAPTER 6

CONCLUSION

The CCD camera for the fiber optic scanner was developed at Photon Imaging Corp, as a part of the joint program with the New Jersey Institute of Technology. The CCD camera consists of clock drivers for the CCD chip, microcontroller and other digital circuitry, analog to digital converter, signal processing circuitry and communication interface to the host computer. The CCD camera is part of the document scanner using optical fiber bundle. The CCD camera system works as expected producing images compatible with the laser printers. It uses inexpensive optics because of the optical fiber bundle. The virtual phase CCD imager allows to use simple clock drivers.

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[6] Discussion with Prof. Walter F. Kosonocky.

[7] Discussion with Peretz Feder from Photon Imaging Corp.

[8]. "Optoelectronics and Image Sensor Data Book", Texas Instruments, 1987

[9] "High Speed CMOS logic IC Data Book", Samsung Semiconductors, 1988

[10] "Linear and Interface ICs", Motorola Semiconductors, 1988

[11] "Linear Products Data Book", Analog Devices, 1988

[12] "Precision Analog and Power Control Handbook", Teledyne Semiconductors, 1989

[13] "Microcomputer Products vol. 2", NEC Electronics Inc., 1988

[14] "IC Memory Data Book", Hitachi Semiconductors, 1988

[15] "Optoelectronics Designers Catlog", Hewlett-Packard Company, 1988-89

APPENDIX

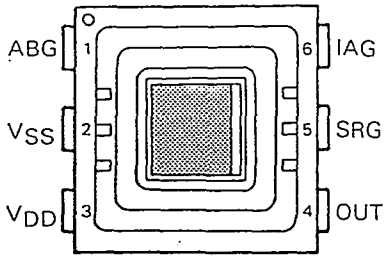
1. Data sheets for the CCD chip TC211 from Texas Instruments.

TC211
192 × 165-PIXEL CCD IMAGE SENSOR

D2991, AUGUST 1986—REVISED MAY 1987

- Full-Frame Operation
- Antiblooming Capability
- Single-Phase Clocking for Horizontal and Vertical Transfers
- Fast Clear Capability
- Dynamic Range . . . 60 dB Typ
- High Blue Response
- High Photoresponse Uniformity
- Solid-State Reliability with:
  - No Image Burn-In
  - No Residual Imaging
  - No Image Distortion
  - No Image Lag

DUAL-IN-LINE PACKAGE
(TOP VIEW)



- 6-Pin Dual-In-Line Ceramic Package
- Square Image Area
  - 2640 μm by 2640 μm
  - 192(H) Pixels by 165(V) Pixels
  - 13.75 μm (H) by 16 μm (V) Pixels

description

The TC211 is a full-frame charge-coupled image sensor designed specifically for industrial applications where ruggedness and small size are required. The image sensing area is configured into 165 horizontal lines containing 192 elements each. Twelve additional covered pixels are provided at the end of each line to establish a dark reference and line clamp. The antiblooming feature is activated by supplying clock pulses to the antiblooming gate, which is an integral part of each image-sensing element. The charge is converted to signal voltage at 4 μV per electron by a high-performance structure with built-in automatic reset and a voltage reference generator. The signal is further buffered by a low-noise two-stage source-follower amplifier to provide high output drive capability.

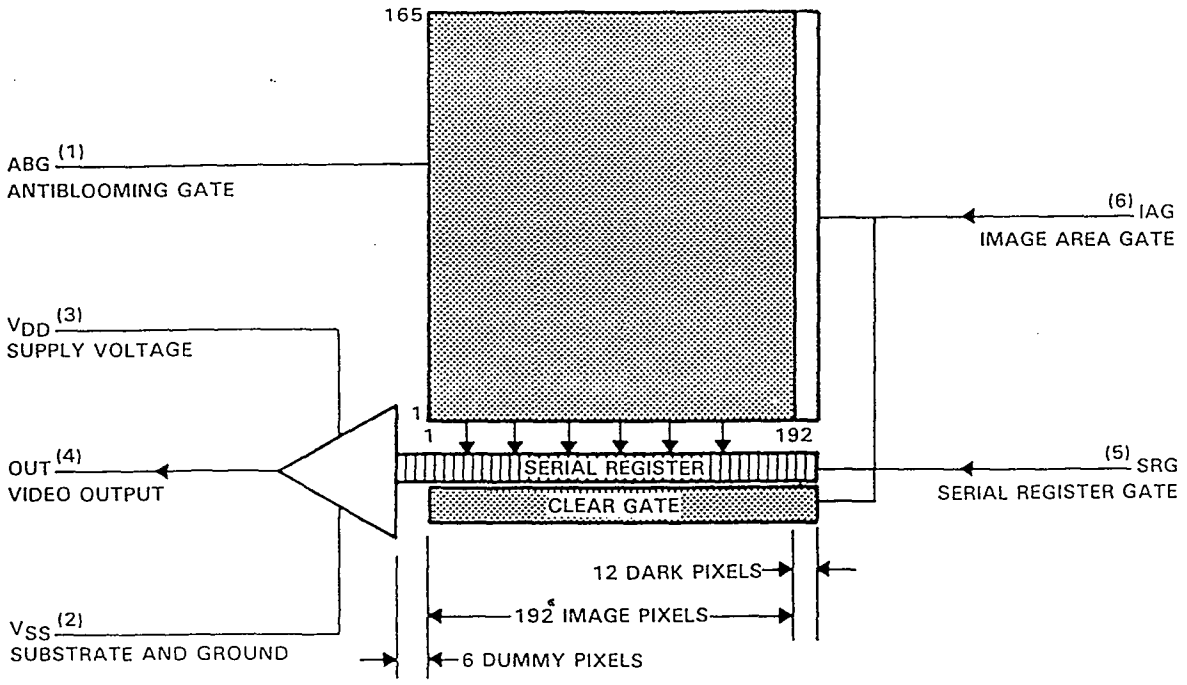
This device is supplied in a 6-pin dual-in-line ceramic package approximately 7,5 mm (0.3 in.) square.

operating and handling precautions

The TC211 is an N-channel MOS device and requires all the standard precautions used with MOS circuits. Limited gate protection circuitry is incorporated into the device, and the pin voltages must not under any circumstances exceed the absolute maximum ratings. The device can also be damaged if the drains or the output terminals are reversed biased and an excessive current is allowed to flow. When the device is not mounted in a circuit, all leads should be shorted together with wire or inserted into conductive foam. The glass window can be cleaned using any standard method for cleaning optical assemblies or by wiping the surface with a cotton swab soaked in alcohol.

ADVANCE INFORMATION

functional block diagram



functional description

The image-sensing area consists of 165 horizontal lines containing 192 photosensitive elements or pixels in each line. As light enters the silicon in the image-sensing area, free electrons are generated and collected in the potential wells. Each pixel is 13.75 μm (horizontal) by 16.00 μm (vertical) as shown in the functional block diagram. The quantity of charge collected in each pixel is a linear function of the incident light and the exposure or integration time. After exposure and under dark conditions, the charge packets are transferred from the image area to the serial register one row at a time with each clock pulse applied to the image area gate.

The twelve columns to the right of the image area in the functional block diagram are shielded from incident light. The signal derived from these pixels can be used to generate the dark reference for restoration of the video black level. They appear at the end of each row but provide a valid reference for the subsequent line.

Every pulse at the image area gate causes an automatic fast clear of the serial register before the next row of charges is transferred in. After a row of charge packets is transferred into the serial register, the serial register gate may be clocked until all of the charges are moved out of the serial register to the charge detection node at the input of the amplifier. The automatic fast clear feature can be used to initialize the image area by transferring all 165 rows to the serial register gate under dark conditions without clocking the serial register gate.

The six dummy cells at the front of the serial register are used to transport charges from the register to the input of the amplifier. They are not cleared by the image area gate clock.

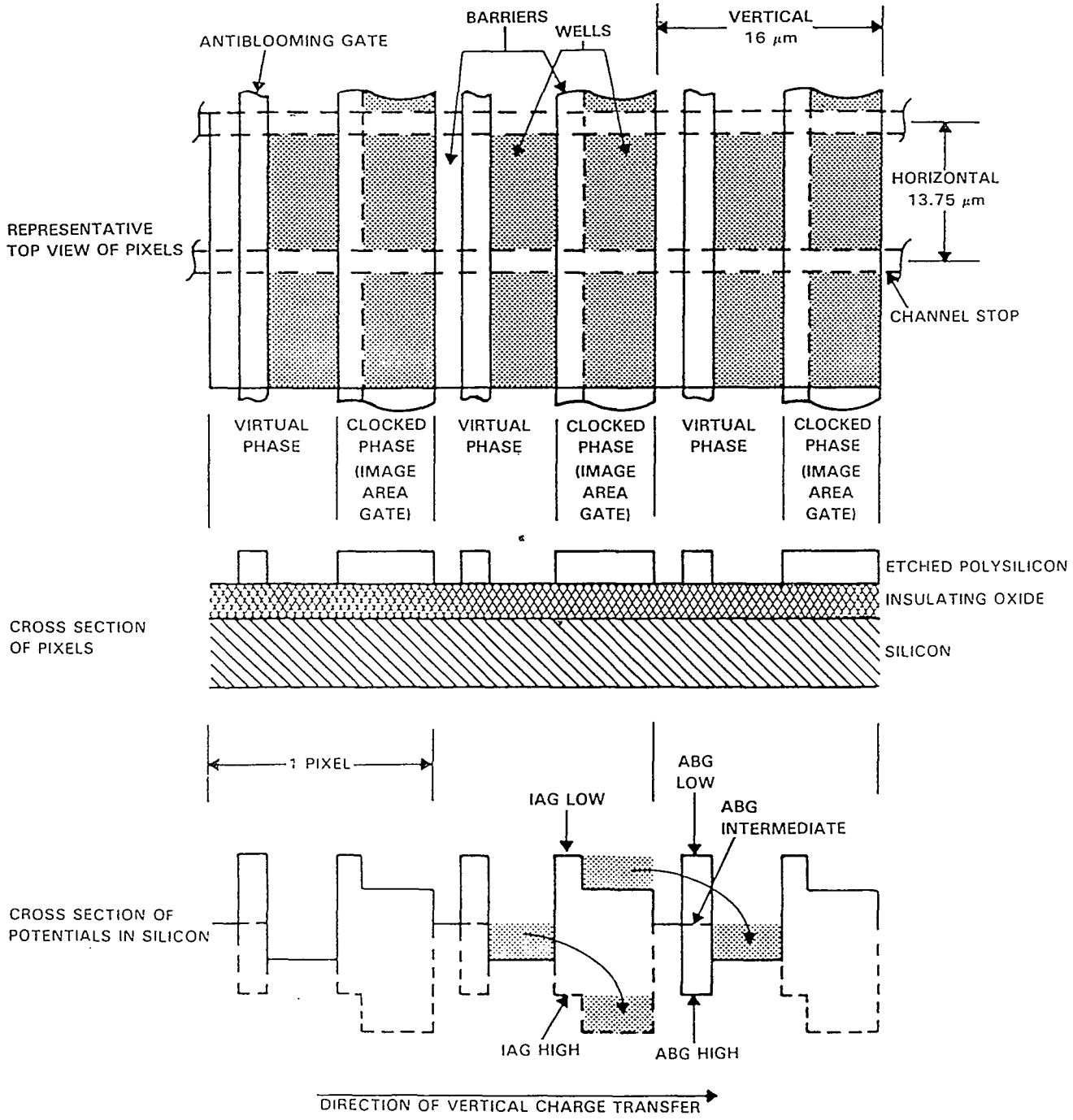


FIGURE 1. CHARGE ACCUMULATION AND TRANSFER PROCESS

ADVANCE INFORMATION

absolute maximum ratings

Supply voltage range, V_{DD} . . . . . 0 V to 15 V
Clock voltage range for IAG, SRG, ABG . . . . . −15 V to 5 V
Operating free-air temperature range . . . . . −10°C to 45°C
Storage temperature range . . . . . −30°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: All voltage values are with respect to the substrate (V_{SS}) terminal.

recommended operating conditions

			MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}			11	12	13	V
Supply current, I_{DD}				5	10	mA
Substrate bias				0		V
Clock voltages (see Note 2)	Image area gate	High level	0	1	2	V
		Low level	−10	−9.5	−8.5	V
	Serial register gate	High level	1.5	2	2.5	V
		Low level	−10	−9.5	−8.5	V
	Antiblooming gate	High level	2.5	3.5	4	V
		Intermediate level	−3	−2.5	−2	V
		Low level	−8	−7	−6	V
Clock rates	Image area gate				15.7	kHz
	Serial register gate				7.16	MHz
	Antiblooming gate				1	MHz
t_1	Time delay from SRG↓ to IAG↑		10			ns
t_2	Time delay from IAG↓ to SRG transfer pulse↑		10			ns
t_3	Pulse duration of the high level for IAG		100			ns
t_4	Pulse duration of the high level for SRG transfer pulse		100			ns
t_5	Time delay from IAG↓ to SRG transfer pulse↓		10			ns
t_6	Time delay from SRG transfer pulse↓ and SRG clock pulse↑		10			ns
Operating free-air temperature, T_A			−10		45	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for clock voltage levels.

ADVANCE INFORMATION

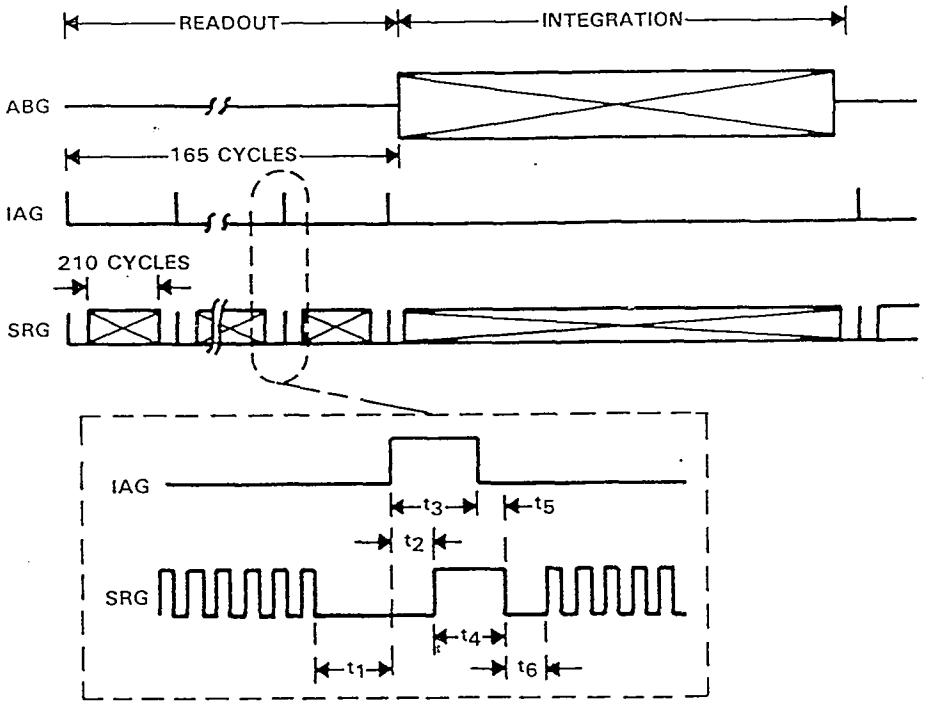


FIGURE 2. TIMING DIAGRAM

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		MIN	TYP†	MAX	UNIT
Dynamic range (see Note 3)	Antiblooming disabled (see Note 4)	60			dB
	Antiblooming enabled	57			
Signal response delay time (see Note 5)			25		ns
Gamma (see Note 6)		0.89	0.94	0.99	
Output resistance			700	800	Ω
Noise voltage	f = 5 kHz (see Note 7)		270		$nV/\sqrt{Hz}$
	f = 100 kHz		70		
Rejection ratios at 7.16 MHz	From V_{DD} to output (see Note 8)		39		dB
	From SRG to output (see Note 9)		37		
Capacitance	Image area gate		1600		pF
	Serial register gate		25		
	Antiblooming gate		780		

†All typical values are at T_A = 25°C.

NOTES: 3. Dynamic range is −20 times the logarithm of the mean noise signal divided by the saturation output signal.
4. For this test, the antiblooming gate must be biased at the intermediate level.
5. Signal response delay is the time between the falling edge of the SRG clock pulse and the output signal valid state.
6. Gamma is the value of the exponent in the equation below for two points on the linear portion of the transfer function curve.

$$\left(\frac{\text{Exposure(2)}}{\text{Exposure(1)}}\right)^{\text{gamma}} = \left(\frac{\text{Output signal(2)}}{\text{Output signal(1)}}\right)$$

The value above represents points near saturation.

7. Figure 7 shows a typical noise spectrum of the output amplifier.
8. V_{DD} rejection ratio is −20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at V_{DD}.
9. SRG rejection ratio is −20 times the logarithm of the ac amplitude at the output divided by the ac amplitude at SRG.

ADVANCE INFORMATION

optical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		MIN	TYP†	MAX	UNIT
Sensitivity (see Note 10)			280		mV/lx
Saturation signal	Antiblooming disabled	400	600		mV
	Antiblooming enabled	350	450		
Blooming overload ratio (see Note 11)	Strobe		5		
	Shuttered light		100		
Output signal nonuniformity (1/2 saturation) (see Note 12)			10%	20%	
Dark signal	T_A = 25°C		10	15	mV
Dark signal nonuniformity for entire field (see Note 13)	T_A = 25°C		4	15	mV
Modulation transfer function	Horizontal		50%		
	Vertical		70%		
Charge transfer efficiency			99.998%		

† All typical values are at T_A = 25°C.

NOTES: 10. Sensitivity is measured at λ = 550 ± 5 nm with Melles-Griot #03F1V079 filter and 16.6-ms exposure time.
11. Blooming overload ratio is the blooming exposure relative to the saturation exposure.
12. Output signal nonuniformity is the ratio of the maximum pixel-to-pixel difference in output signal to the mean output signal for exposure adjusted to give 1/2 the saturation output signal.
13. Dark signal nonuniformity is the maximum pixel-to-pixel difference in a dark condition.

PARAMETER MEASUREMENT INFORMATION

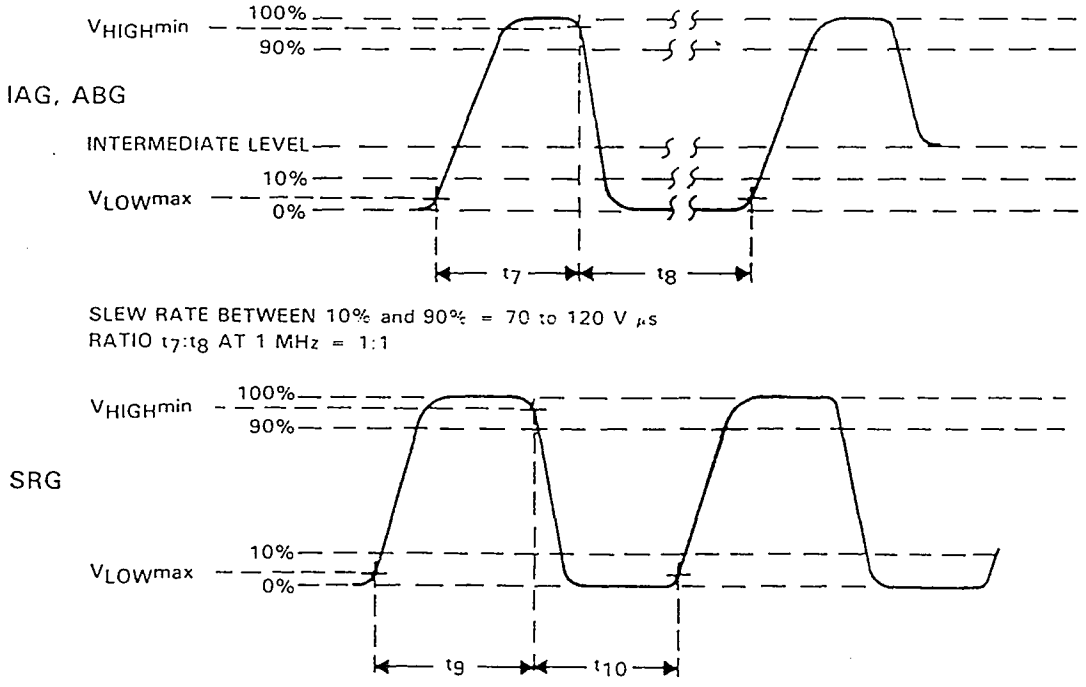


FIGURE 3. TYPICAL CLOCK WAVEFORM FOR IAG, ABG, AND SRG

ADVANCE INFORMATION

PARAMETER MEASUREMENT INFORMATION

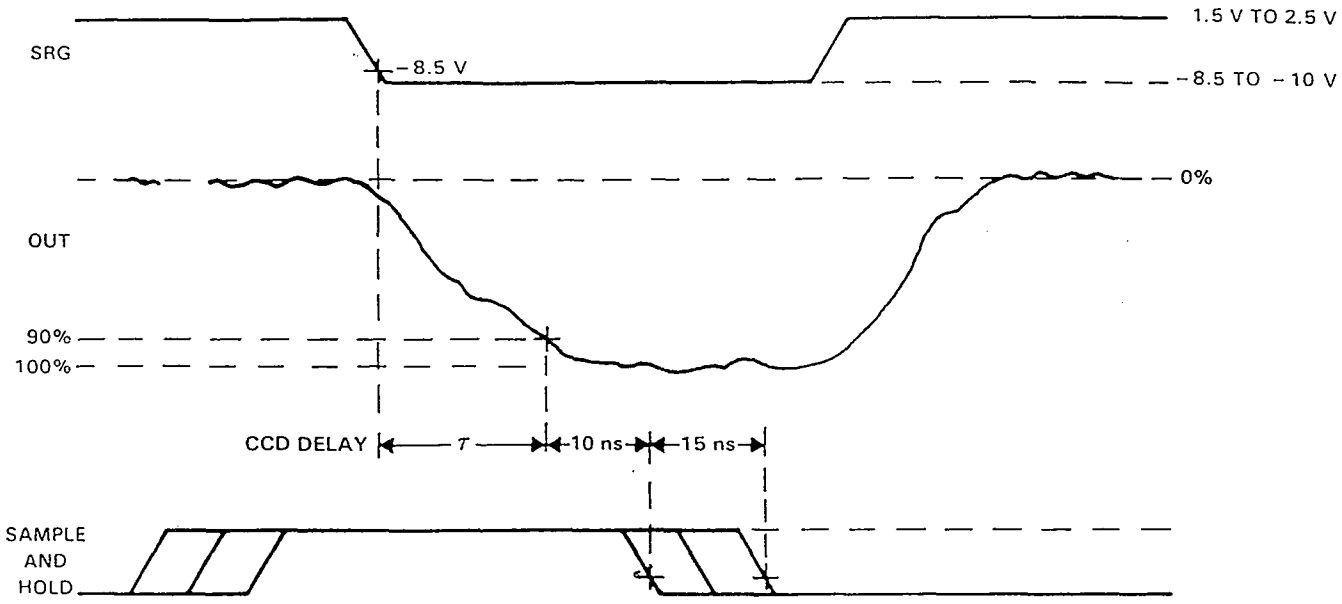


FIGURE 4. TYPICAL SRG AND VIDEO OUTPUT WAVEFORMS

TYPICAL CHARACTERISTICS

HORIZONTAL MODULATION
TRANSFER FUNCTION
(BARS PARALLEL TO SERIAL REGISTER)

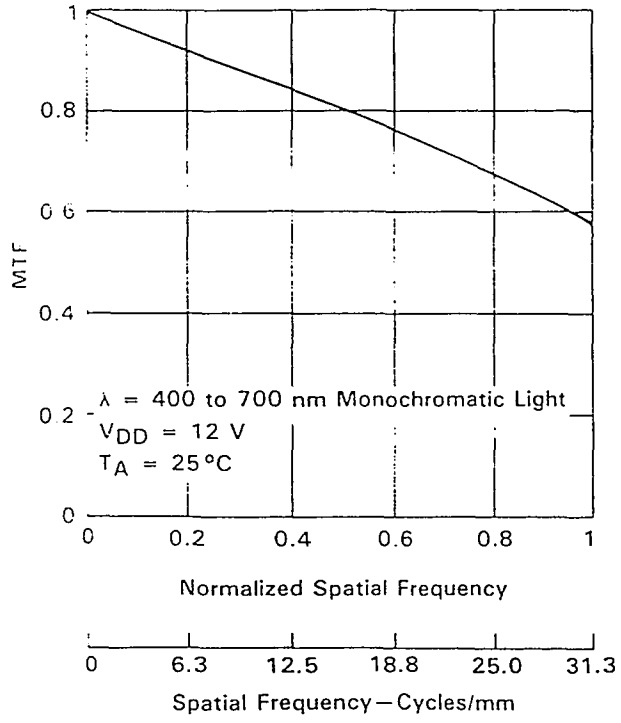


FIGURE 5

VERTICAL MODULATION
TRANSFER FUNCTION
(BARS PERPENDICULAR TO SERIAL REGISTER)

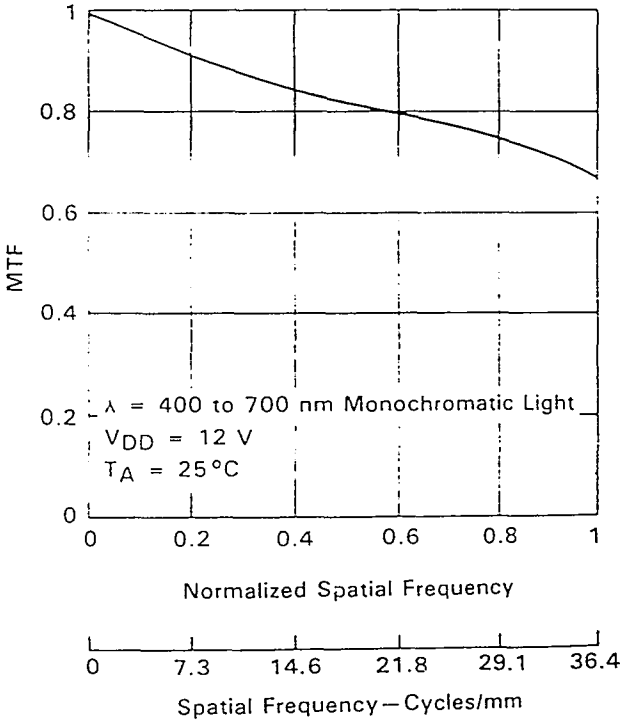


FIGURE 6

ADVANCE INFORMATION

TYPICAL CHARACTERISTICS

NOISE SPECTRUM OF OUTPUT AMPLIFIER

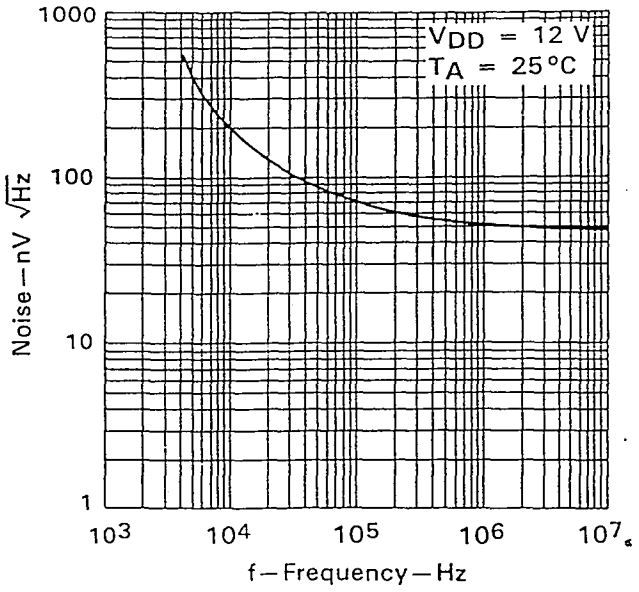


FIGURE 7

CCD SPECTRAL RESPONSIVITY

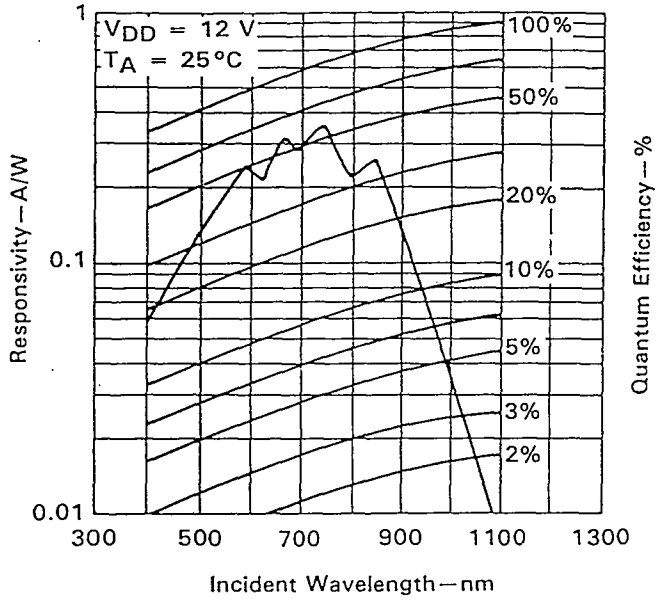
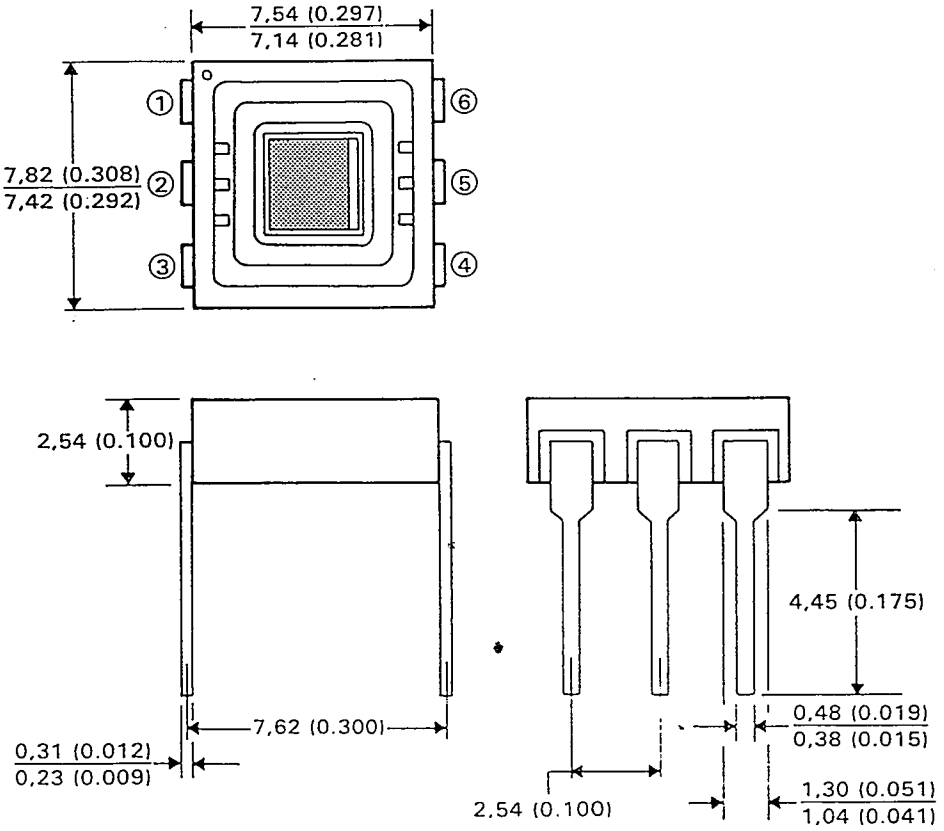


FIGURE 8

ADVANCE INFORMATION

MECHANICAL DATA



NOTES: 1. Dimensions are in millimeters and parenthetically in inches. Single dimensions are nominal.
2. The center of the package and the center of the image area are approximately coincident.
3. The distance from the top of the glass to the images sensor surface is typically 1-mm (0.040-inch). The glass is typically 0.020 inch thick and has an index of refraction of 1.52.

ADVANCE INFORMATION