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An investigation of OptoElectronic Integrated Circuit receiver

Dinar S. Gupte
New Jersey Institute of Technology

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ABSTRACT

Title of Thesis : An Investigation of OptoElectronic Integrated Circuit Receiver

Dinar S. Gupte, Master of Science, Electrical Engineering Department, 1990

Thesis directed by : Dr. N.M.Ravindra, Associate Professor.

This thesis report presents an investigation of an OptoElectronic Integrated receiver Circuit (OEIC). An OEIC on Silicon (Si) substrate is analyzed and simulated as part of this investigation. The OEIC is based on GaAs technology. The advantages of this are its compactness, high speed, low noise and high reliability in light wave communication systems. A higher output signal is required to make such devices suitable for practical applications. This is achieved by the use of a cascode stage. The fabrication techniques of the relevant semiconductor devices have also been discussed.

In light wave communication systems, the region of minimum losses is of most interest. This region lies between 1.3-1.55 μm wavelength range. Silica optical fibers exhibit minimum losses in this wavelength range and $In_{0.53}Ga_{0.47}As$ photodetector has maximum quantum efficiency in this range.

The fabrication of GaAs MESFETs on Si substrate using molecular beam epitaxy grown film is also discussed. The intention is to make possible the integration of GaAs based devices with Si devices and to reduce the complexity of the fabrication technique. The process of interest is the epitaxial lift-off where an appropriate epitaxial structure is selectively removed from the original GaAs substrate and reattached to a new Si substrate. This fabrication procedure is a substitute for hetroepitaxy of GaAs on Si substrate.

Finally, calculations of the transfer function, poles & zeros have been made by the use of small signal high frequency analysis technique. The circuit simulation of OEIC is completed using SPICE3C.1 in an Ultrix environment.

An Investigation of OptoElectronic Integrated Circuit Receiver

by

Dinar S. Gupte

Thesis submitted to the Faculty of the Graduate School of
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APPROVAL SHEET

Titel of Thesis : Investigation of OptoElectronic Integrated Circuit Receiver.

Name of the candidate : Dinar S. Gupte

: Master of Science in Electrical Engineering, 1990

Thesis and abstract approved :

12/5/90

Dr. N. M. Ravindra **Date**
Associate Professor
Department of Physics
New Jersey Institute of Technology

12/5/90

Dr. K. Sohn **Date**
Professor
Dept. of Electrical Engineering
New Jersey Institute of Technology

12/5/90

Dr. D. Misra **Date**
Assistant Professor
Dept. of Electrical Engineering
New Jersey Institute of Technology

VITA

Name	:	Dinar S. Gupte
Permanent address	:	
Degree and Date conferred	:	M.S.E.E., December'1990
Date of birth	:	
Place of birth	:	
Secondary education	:	Parle College of Science, Vile parle (East), Bombay India.

Collegiate institute attended	Degree	Date of degree
New Jersey Institute of Technology	M.S.E.E.	December'1990
Manipal Institute of Technology	B.E.	August'1987

Major	:	Electronics & communication Engineering
Posotion held	:	Quality Control & Instrumentation Engineer Advance Technology Devices (ATD), SEEPZ, Bombay, India.

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Chapter 1

INTRODUCTION

1.1 An Overview:

In light wave communication systems, the desired signal is transferred from one destination to another in the form of light energy attributed to particles known as photons. Recent developments provide the facility of fiber optic communication channel for this transfer. The advantage of the fiber optic channel is the minimum loss of signal and distortion at the receiver end. At the receiver end, this optical signal has to be converted to an electrical signal for its further use. High output signal level is required to make its use for practical applications. The conversion of optical signal to electrical signal is possible by the use of a transducer and the amplification is achieved with an amplifier. These two together form an important circuit in light wave communication systems known as OptoElectronic Integrated

Circuit receiver (OEIC). In this work, an investigation of such an OEIC is presented in terms of its design, simulation, fabrication and characterization.

The OEIC is based on Gallium Arsenide (GaAs) technology. The hetrojunction p-i-n diode is used as a transducer and the desired amplification of the electrical signal is achieved by the use of cascode amplifier. This amplifier has GaAs Metal Semiconductor Field Effect Transistor (MESFET) as its major component. In the past, developments have been made to achieve this amplification using multistage amplifier systems [1].

1.2 Devices:

In chapter 2, the basics and the principle of operation of the relevant semiconductor devices have been discussed. The advantages in using GaAs devices over that of silicon (Si) are their superiority in low field electron mobility (Si=1000 $cm^2/V-cm$, GaAs=5000 $cm^2/V-cm$) and saturation velocities (Si=0.7 $\times 10^5$ m/s, GaAs= 10^7 m/s). Higher electron mobility in GaAs leads to a substantial advantage in device performance such as smaller transit time which eventually minimizes the series resistance. These advantages are further enhanced by higher effective saturation velocities in GaAs which results in increased cutoff frequencies. Hence these devices can operate at frequencies (in GHz range) higher than Si devices. Due to high band gap (E_g= 1.42eV at 300K [Appendix])of GaAs, the GaAs substrate offers natural electrical isolation between active devices.

In this OEIC, p-i-n diode photodetector is used as a transducer. It receives the optical signal from fiber optic communication channel and converts it into an electrical signal of 1mv, 1GHz frequency. The carrier absorption is based on the theory of absorption of photons. This states that the energy of incident light has to be greater than or atleast equal to the energy gap of the material used for the

absorption process. This absorption produces electron-hole pairs. Hetrojunction p-i-n diode has an advantage of absorping the light of the desired wavelength. Indium Gallium Arsenide (InGaAs, Energy gap= .75eV at 300K [Appendix]) absorps light radiation in the 1.3-1.55 μm wavelength range. This is the region of minimum loss in dbs/km in the silica optical fiber. The dark current [Appendix] of p-i-n diode is also an important topic of discussion in this chapter. Dark current is in the subpicoampere range for InGaAs p-i-n diode.

The next device used in OEIC is GaAs MESFET. This is the most important component of the amplifier. The MESFET has three terminals namely Source, Gate and Drain. There are two types of MESFETs (i) Depletion mode and (ii) Enhancement mode MESFET. In this OEIC, depletion mode MESFETs are of most interest. MESFET has a metal semiconductor rectifying contact for gate electrode. The gate voltage modulates the width of the depletion region of metal-semiconductor schottky barrier. This eventually modulates the flow of mobile charges through the channel. The GaAs MESFET considered for OEIC has the following features; gate length L = 1μm, transconductance g_m = 135 mS/mm, drain saturation current I_{ds} = 130 mA/mm, pinch off voltage = -1.6V, cutoff frequency f_T = 12GHz and low output conductance [2]. GaAs MESFET channel properties can be characterized by the four basic parameters -channel length, channel width, channel thickness and channel doping.

1.3 Fabrication:

The fabrication technique and principle of operation of OEIC is explained in chapter 3. InGaAs & InP are the basic materials in the fabrication of the p-i-n diode. InP is optically transparent and nitride layer on the top behaves as an antireflection coating for the p-i-n diode. This antireflection coating increases the quantum

efficiency to about 60%.

Recently, lattice mismatched hetroepetaxial technology and its application for GaAs devices has been developed. In this fabrication technique of p-i-n diode, GaAs layer is directly grown on semi-insulating InP substrate [3]. Currently, there is increasing interest in achieving the integration of GaAs and Si devices on the same chip. The first such device was the GaAs shallow homojunction solar cell. This cell was developed in Lincon laboratory [4]. This nucleation of GaAs on Si becomes difficult with hetroepitaxy because of native oxide and other contaminations, defects (particularly Carbon) on Si surface. In order to improve the device performance and reliability, it is necessary that these defects be eliminated or reduced as much as possible. In this OEIC, GaAs MESFETs are fabricated using an alternate method to this known as molecular beam epitaxial lift off. In this technique, GaAs devices are selectively detached from GaAs substrate and are attached to Si substrate. This adhesion is possible with Van der Waal forces [appendix]. After fabrication of the chip, crosstalk between the adjacent devices is minimized. This phenomenon is known as Backgating [5].

1.4 Simulation and characterization:

The computer simulation of the OEIC is described in chapter 4. In any integrated circuit design, computer simulation plays an important role. This simulation gives the feeling of how the circuit is going to behave after fabrication or implementation and the required changes can be made to achieve the desired output. This is done by observing the performance of the chip on the computer terminal. This computer simulation of OEIC is carried out using the general purpose circuit simulation program SPICE. SPICE3C.1 is the most recent version of the SPICE. This was originally developed at the University of California, Berkley. In this simulation

technique, the OEIC is presented in the form of a computer program by defining the nodes of the circuitry. Necessary biasing of MESFETs is done to get the optimum output. The special features of SPICE3C.1 are also described in chapter 4 [6].

The small signal high frequency analysis is presented in chapter 5. Basically, it covers the transfer function, calculations of poles & zeros and the effect of body and parasitic capacitance on the output signal of OEIC. OEICs are very much attractive for application to high speed and large capacity optical communication systems because they have the potential advantage of reducing the parasitic reactance between an optical element and an electronic element. Scope of investigation is generally restricted by the difficulty of fabrication which will lead to large body and parasitic capacitance [7]. These considerably affect the response of OEIC.

Chapters 7 and 8 contain the appendix and bibliography respectively.

Chapter 2

P-I-N DIODE & GaAs MESFET

2.1 P-I-N DIODE:

2.1.1 Introduction:

In the operation of an optoelectronic integrated circuit, the photodetector plays an important role. A photodetector is a semiconductor device which converts an optical signal into an electrical signal. In this OEIC, a p-i-n diode is used as a photodetector. It receives an optical signal from fibre optic communication channel and converts it into an electrical signal. The receiver sensitivity depends upon the quality and dimensions of the photodetector and also on the fibre optic communication channel. There are different types of photodetectors avaliable but the hetrojunction p-i-n diode has an advantage of converting only the light of desired wavelength.

2.1.2 Basics of p-i-n diode:

The basic structure of a p-i-n diode is explained below. p-i-n diode has an intrinsic layer in between p-type and n-type regions. This intrinsic layer is responsible for the absorption of the light (photon) energy. The conversion of optical signal to electrical signal proceeds in 3 stages. When the photon energy is absorbed, carriers are generated by incident light. The second stage is the carrier transportation mechanism and the last stage is the interaction of carriers with the external circuit to produce an electrical signal.

The carrier absorption occurs when the energy of incident photon is greater than or atleast equal to the energy of the absorbing material. That is, $h\nu \geq E_g$ where h is the planck's constant ($h = 6.625 \times 10^{-34}$ Js), $\nu = c/\lambda$ where c is the velocity of light in vacuum and λ is the wavelength of the incident photon. The absorption of light in the semiconductor produces electron-hole pairs. Light absorption characteristics is shown in the fig. 2.1. Electron-hole pairs produced in the depletion region or within the diffusion length will eventually be separated by an electric field. For an intrinsic semiconductor, the conductivity is given by,

$$\sigma = q(\mu_n \eta + \mu_p p) \tag{2.1}$$

where, μ_n & μ_p are the mobilities of electrons and holes respectively. The increase in conductivity is mainly because of increase in number of carriers [8].

Photodetectors have broad range of application including infrared sensors in optoisolation and detectors for fibre optic communication. For these applications, the detector must have high sensitivity at the operating wavelength, high response

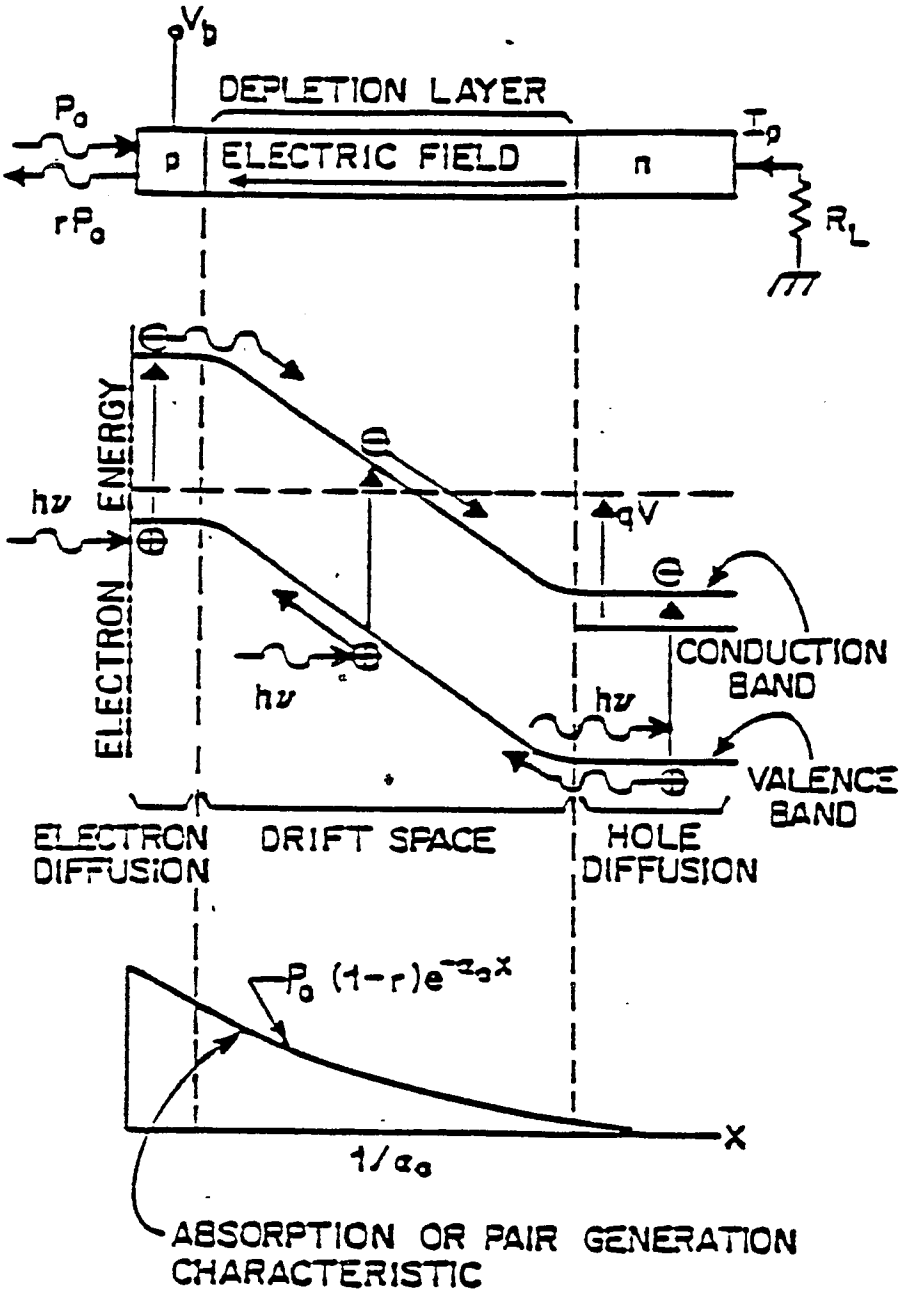


Figure 2.1: Light absorption charactristics [8].

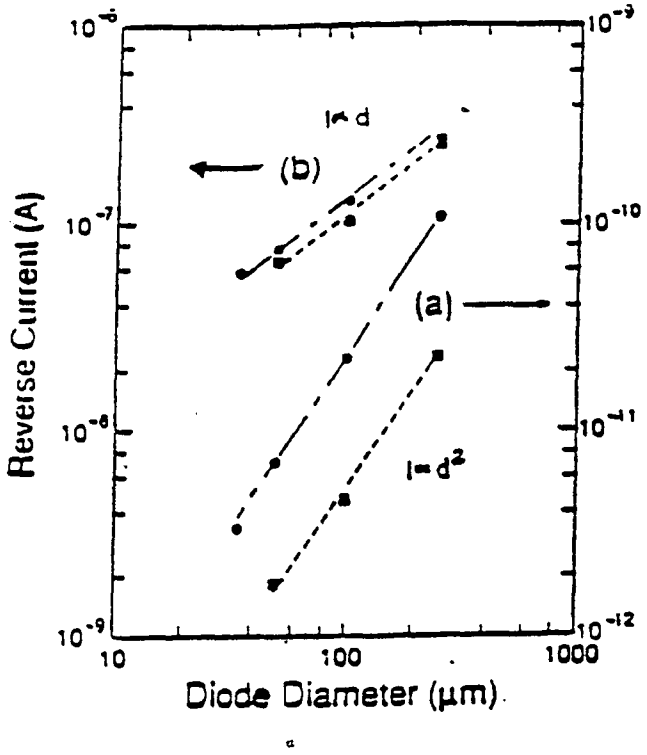


Figure 2.2: Area dependency of dark current [9].

speed and low noise. To use it as an integrated device, it should be compact and should be operated at low voltages or currents. p-i-n diodes have been characterized for their dark currents and the temperature dependency. Localised junctions reduce the area of periphery to reduce the dark current. The area dependency of the dark current is as explained in fig.2.2. The dark current is also a function of the reverse bias applied to the diode. As shown in fig.2.2, at low reverse bias (-10V, a) the dark current varies as I αd^2 and at large reverse bias (-25V, b) the dark current varies as I α d. The dark current in a p-i-n diode is defined as the carriers generated to produce a small electrical current without any external excitation. Normally, the dark current is the sum of the diffusion current, tunneling current and the bulk generation current in the hetrointerface. These components of the dark current can be analysed as follows.

A. Diffusion current : At high tempratures, the dark current of a p-i-n diode varies very little with the change in bias voltage. The dominant source of the dark current is the diffusion current and is normally due to the thermally generated minority carriers diffused into the depletion region.

$$I_{diffu} = I_s[\ 1 - \exp(-qV_R/KT)] \tag{2.2}$$

where, q is the electrical charge on minority carriers, K is the boltzman constant(1.38×10^{-23} J/K), T is the junction temperature and I_s is the saturation current which is;

$$I_s = q\ n_i^2\ (D_n/\tau_d)^{1/2} * A/\ N_A \tag{2.3}$$

where, τ_d is the minority carrier diffusion life time, A is the area of the depletion boundary, N_A is doping density and D_n is the minority carrier diffusion constant.

$$D_n/\mu_n = KT/q \tag{2.4}$$

D_n can be calculated from carrier mobility and n_i, the intrinsic carrier density. The graph of the dark current versus reciprocal of temperature is shown in fig.2.3 [10].

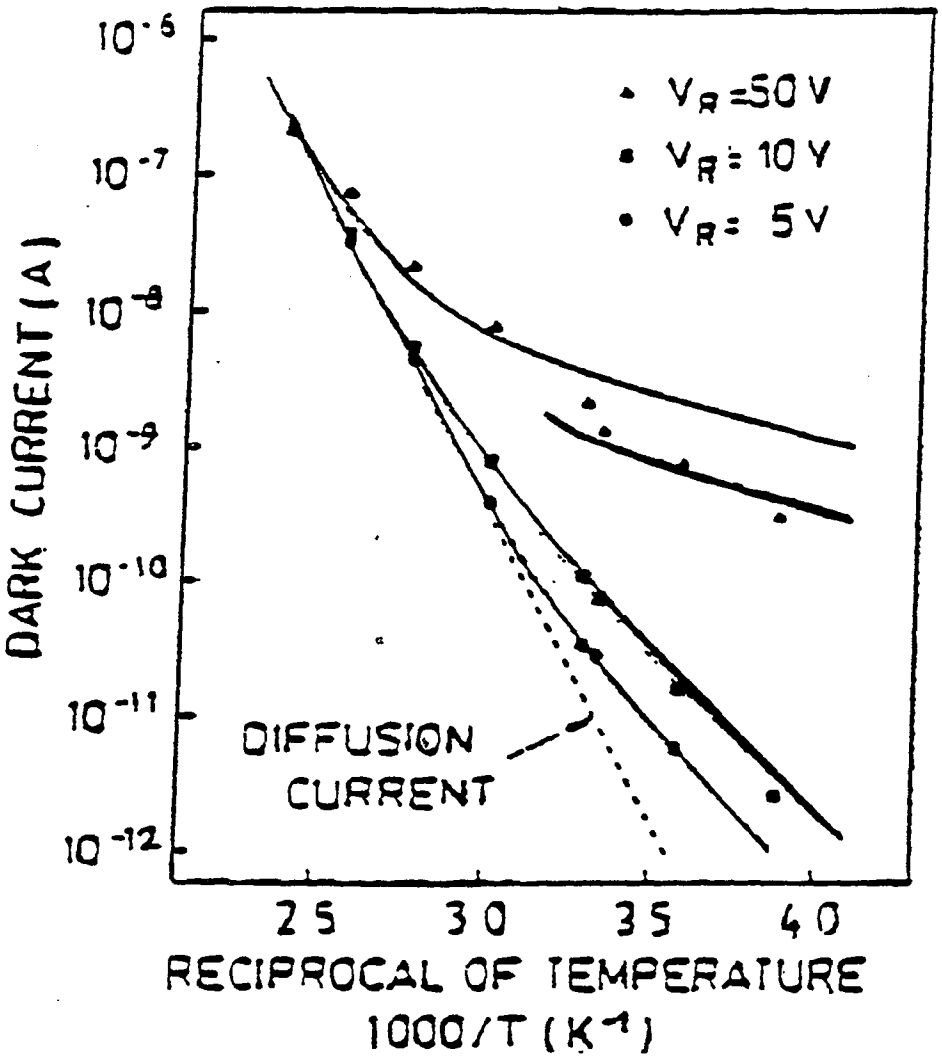


Figure 2.3: Dark current v/s Reciprocal of Temperature [10].

B. Bulk generation current : The bulk generation current dominates the dark current at low temperatures and is the current due to the generation of electron-hole pairs in the depletion region given by;

$$I_{gen} = qn_iAW/\tau_{eff}[\ 1 - \exp(-qV_R/2Kt)] \tag{2.5}$$

Where τ_{eff} is the effective life time and W is the depletion region width [10].

C. Tunneling current : The tunneling current dominates the dark current at high voltages and is given by the band to band tunneling of carriers through the barrier.

$$I_{tun} = [2m_e^{1/2}q^3E_mV_R/4\pi^2h^2E_g^{1/2}] * A \exp[-4(2m_e)^{1/2}E_g^{3/2}/3qE_mh] \tag{2.6}$$

Where h is the planck's constant & $\hbar = h/2\pi$

E_m = Maximum electric field.

$$E_m = [2(V_R + V_{bi})]/\ W. \tag{2.7}$$

Tunneling current is also a function of carrier density because it strongly depends upon E_m and

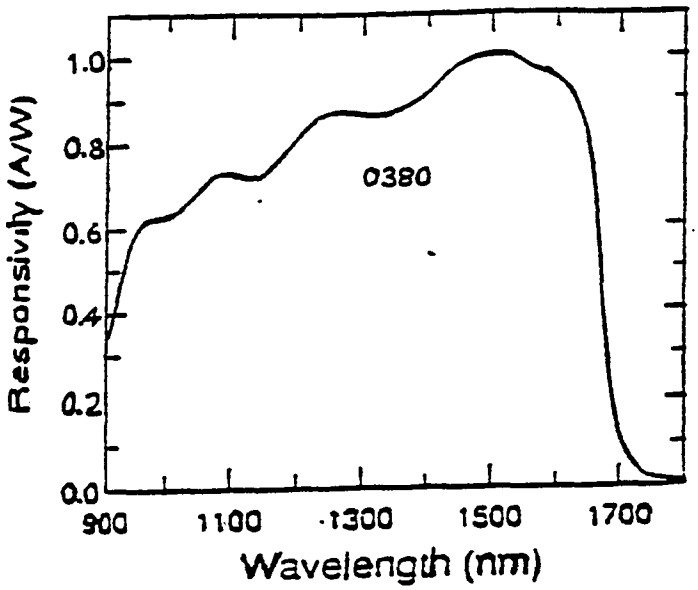


Figure 2.4: Spectral response of an InGaAs p-i-n diode [9].

$$E_m \alpha N_D^{1/2} \tag{2.8}$$

The spectral response of an InGaAs p-i-n diode is given in fig. 2.4. The responsivity increases monotonocally with the wavelength from 0.95μ to about 1.5μ. This exhibits a sharp cutoff at 1.65μ wavelength [9]. InGaAs parameters are given in the table [Appendix].

2.2 GALLIUM ARSENIDE MESFET

2.2.1 Introduction:

The MEtal-Semiconductor Field Effect Transistor (MESFET) was first proposed in 1966. The FETs are devices in which the flow of majority carriers between source and drain is controlled by a voltage applied to the gate. The principle of operation of a MESFET is similar to that of a JFET (Junction Field Effect Transistor). JFET uses the depletion region of one or more reverse biased p-n junctions. However MESFET has a metal semiconductor rectifying contact for a gate electrode. In a MESFET, the gate voltage modulates the width of the depletion region of metal-semiconductor schottky barrier and hence alters the cross section area and therefore the resistance of the channel through which mobile charges flow.

A perspective view of a MESFET is shown in the fig.2.5, where'z' is the channel width, 'L' is the length of the channel and 'a' is the channel depth. Channel properties can be characterized by the four basic parameters: Gate length, Gate width, Channel thickness and Channel doping. Most of the MESFET's are made of III-V compounds such as GaAs [Appendix]. For GaAs, the mobility of electrons is much more (about 15 times) than the mobility of holes which makes n-type devices of more interest.

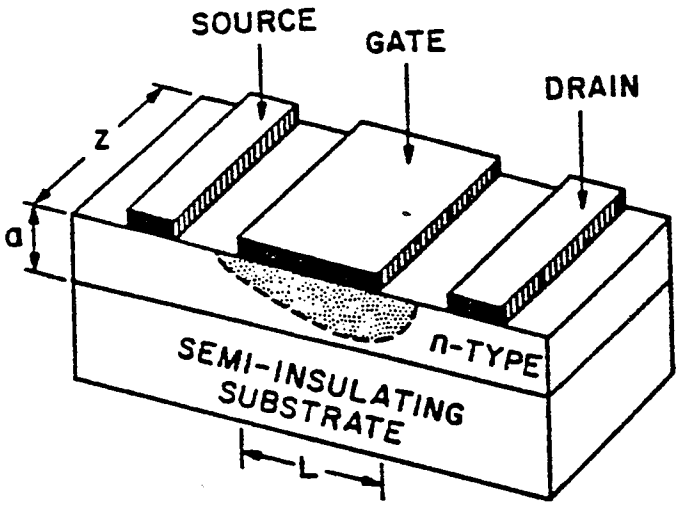


Figure 2.5: Perspective view of a MESFET [11].

2.2.2 Principle of operation of MESFET :

The principle of operation of the MESFET is as explained below. MESFET also has three terminals like drain, gate and source. When the drain voltage becomes positive with respect to source voltage, electrons flow from source to drain and the gate voltage modulates the flow of electrons, forming a rectifying junction with the channel. The gate voltage at which the depletion region reaches to the substrate closing the conducting channel between source and drain is called the threshold voltage (V_T)and the potential difference across the depletion region (V_{bi})at threshold conditions is known as the pinch-off voltage(V_P) [12]. Mathematically it is as shown below.

$$V_T = V_{bi} - V_P \tag{2.9}$$

where V_{bi} is

$$V_{bi} = \phi_{Bn} - 0.026\ln N_c/N_d \tag{2.10}$$

and V_P is

$$V_P = a^2 \text{ q } N_D \text{ / } 2 \epsilon_s \tag{2.11}$$

Eq.2.11 shows that V_P is a function of doping density. In practice, there are two types of MESFETs avaliable.

1. Enhancement mode : Normally-off devices.
2. Depletion mode : Normally-on devices.

Enhancement mode MESFET :

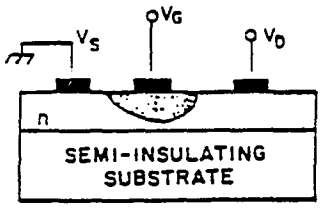
In these devices, the channel is completely pinched off at zero drain-source bias. The built in potential V_{bi} of the gate junction is sufficient to deplete the channel region. The application of forward bias to the gate reduces the depletion region to form a channel. The amount of gate bias determines the flow of majority carriers through the channel. The threshold voltage is positive for enhancement mode devices-fig.2.6.

Depletion mode MESFET :

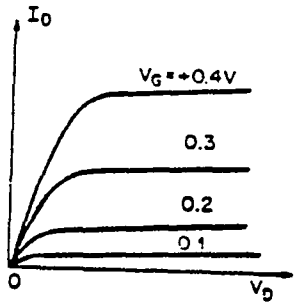
In these devices, the depletion region does not reach the substrate at zero gate bias. There is always a flow of majority carriers through the channel even at zero gate bias which keeps the device on. The threshold voltage is negative for depletion mode devices. In this OEIC, we have considered all devices of depletion mode and the pinch off voltage is considered to be -1.6V and the doping density in the channel is uniform ($10^{17} cm^{-3}$)-fig.2.7.

2.2.3 Advantages of GaAs:

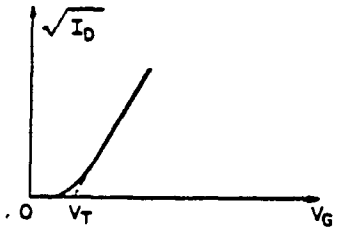
The basic advantages of using GaAs devices are;



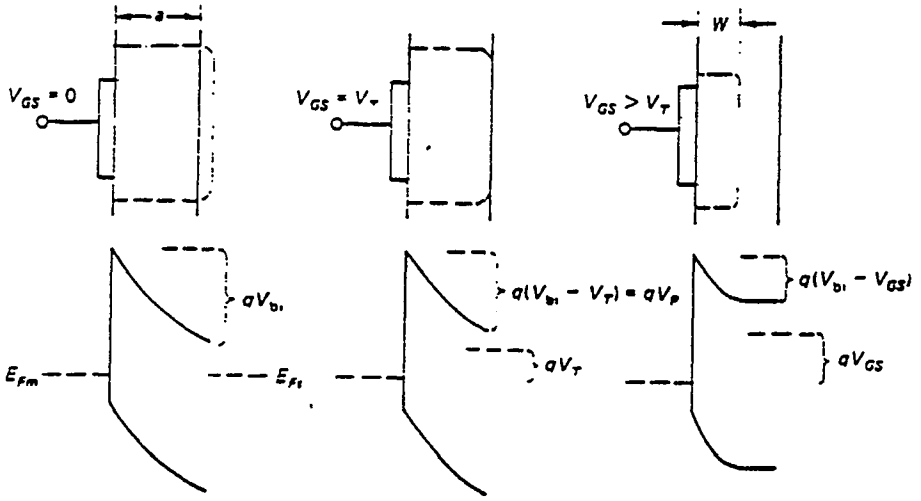
(a) Cross section of MESFET



(b) I-V Characteristics

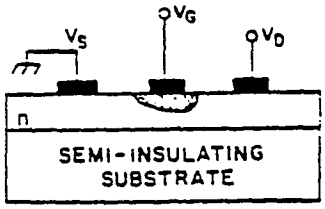


(c) I_d v/s V_T

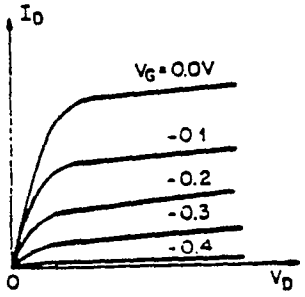


(d) Band diagram

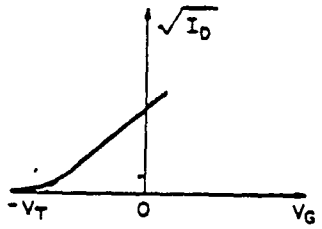
Figure 2.6: Enhancement mode device (a), (b), (c), (d) [12] [13].



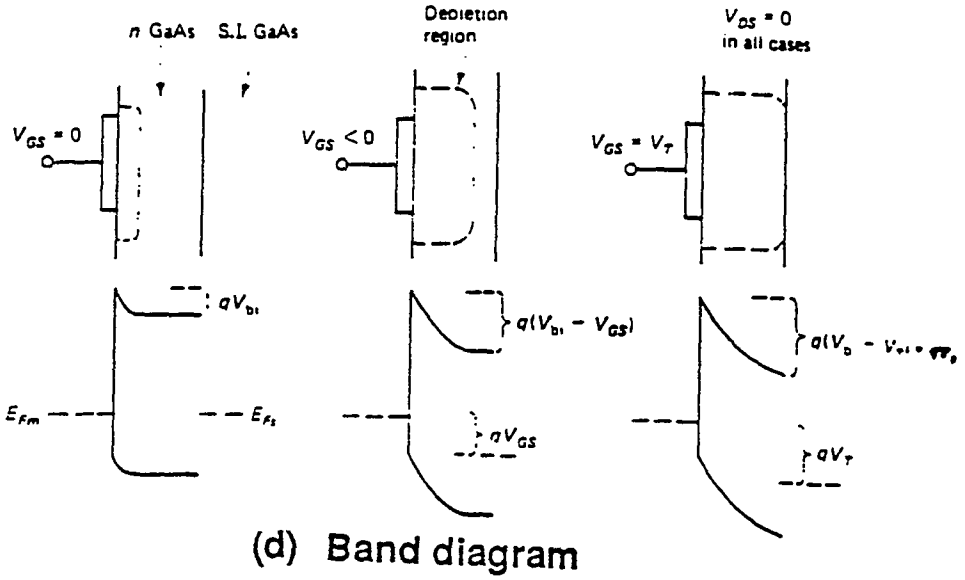
(a) Cross section of MESFET



(b) I-V Characteristics



(c) I_d v/s V_T



(d) Band diagram

Figure 2.7: Depletion mode device (a), (b), (c), (d) [12] [13].

1. Higher electron mobility is of interest, which leads to,

(A) Smaller transit time resulting in faster response of the circuit.

(B) Minimizing the series resistance.

2. High saturation velocities result in increased cutoff frequencies.

3. It provides a perfect lattice matched dielectric insulated substrate which allows decreased parasitic capacitance and simplifies the fabrication process.

4. The semi-insulating substrates offer a natural isolation between active devices on a single substrate.

However, it also has the following disadvantages;

1. Very short minority carrier life time.

2. Lack of a stable passivating native oxide.

3. Crystal defects are many orders of magnitude i.e. higher than in silicon.

All the above disadvantages have prevented the development of bipolar devices and MOS technology using Gallium Arsenide. Thus the main emphasis of GaAs IC technology is in the MESFET area in which majority carriers are transported across the metal-semiconductor contact.

Hence, all the above advantages have led to the selection of n-channel GaAs MESFET as the most appropriate device for the first generation GaAs digital and analog IC's.

2.2.4 Current-voltage characteristics of a MESFET :

Current-voltage characteristics (I-V characteristics) is the best approach to analyze the performance of any device in the actual circuit. The I-V characteristics of a MESFET can be simulated as explained below. The circuit considered for the analysis is shown in fig.2.8. This analysis is done by using SPICE3C.1 [Ref. Chapter 4].

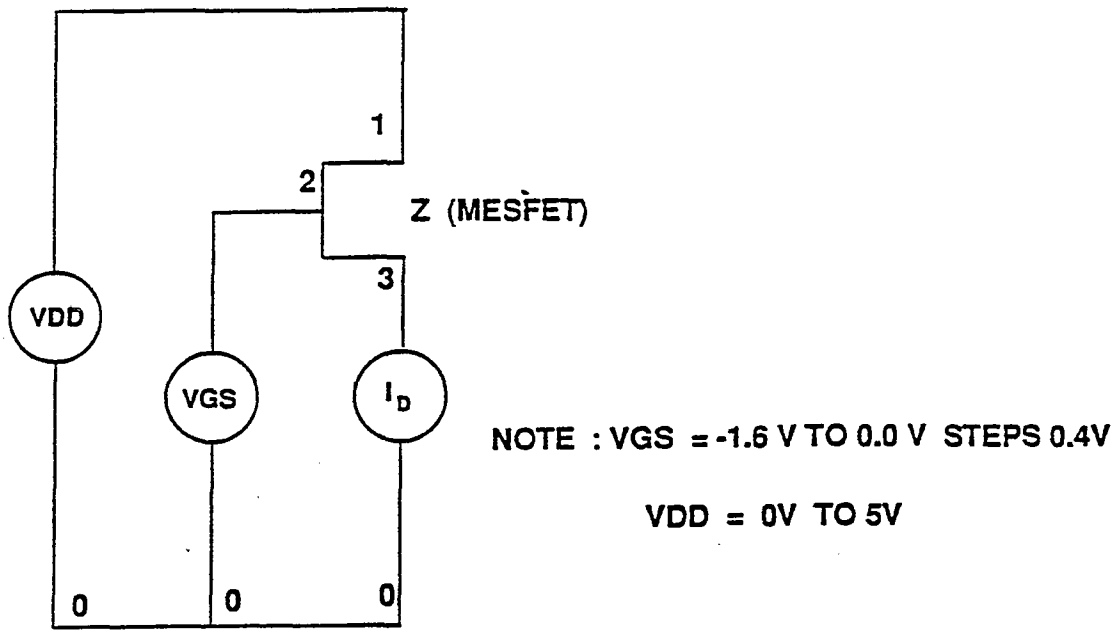


Figure 2.8: Circuit for I-V charactristics.

As shown in fig.2.8, there is a voltage source (V_{DD}) connected to drain. V_{DD} is increased from 0V to 5.0V in steps of 0.2V and the corresponding change in drain current (ID) is measured at different gate-source voltage (V_{GS}) from -2.0V to 0V. As seen from the I-V characteristics, for lower values, near to the threshold voltage, the channel saturates at low drain voltages and value of the saturation current is also very small. Now, any increase in the gate-source voltage increases the saturation current. Channel breakdown occurs at very large drain or gate voltages and very high current flows through the device (channel) which can damage other circuitry in the system. Hence these devices are operated in the region well below the breakdown voltage. Since values of saturation currents are very small near the threshold voltage, the device is operated well above the threshold voltage to have sufficient current flowing in the circuit.

The I-V characteristic shown in fig.2.9 is for any general GaAs MESFET (parameters default by SPICE). The I-V characteristic for the GaAs MESFET used in the OEIC is shown with the desired parameters. The SPICE input of I-V

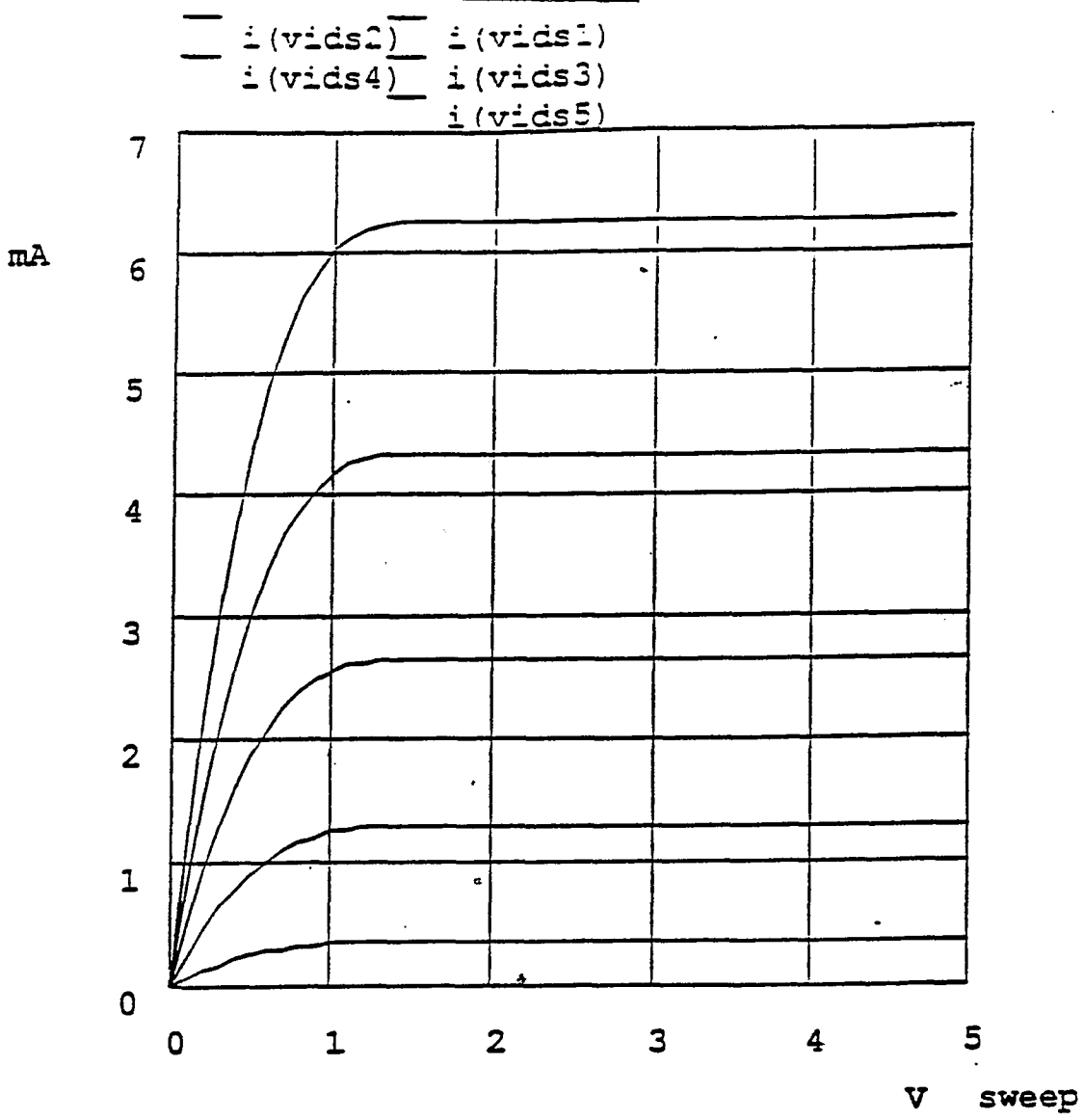


Figure 2.9: I-V charactristics of a MESFET (by default).

characteristics is also shown [Ref. chapter 4].

Chapter 3

Circuit Description & Fabrication Techniques

3.1 INTRODUCTION:

Recently, there has been considerable interest in optical fiber communication in the wavelength range of 1.3 to 1.55 μm. It is in this wavelength range that the silica germania optical fibers exhibit minimum losses. In optical fiber communication, the signal is transferred from one point to another through an optical channel. This optical channel is the optical fiber. At the receiver end, this optical signal is converted into an electrical signal which is further amplified and can be used to operate different kinds of loads. This conversion and amplification of the optical signal is achieved by the use of a photodetector and a pre-amplifier circuit. These two together form an OptoElectronic Integrated Circuit receiver (OEIC). This project is

based on Gallium Arsenide (GaAs) technology. The advantage of GaAs OEIC is its compactness, high speed, low noise and high reliability in light wave communication system. A higher output signal is required to make this device suitable for practical applications. This amplification is achieved by using a cascode stage.

3.2 CIRCUIT DESCRIPTION:

The OEIC is mainly divided into two sections-the photodetector (p-i-n diode) & the pre-amplifier. When the signal is received by the OEIC, it should undergo minimum losses in the fiber optic channel. The ideal graph of loss in db vs wave length of the incident light at the photodetector is shown in fig.4.1. As seen from the graph, the region of minimum loss is of most interest and lies between 1.3 to 1.55 μm wavelength range. As explained earlier, for photon absorbtion, the energy of the photon has to be greater than or equal to the energy gap of the material used i.e. $h\nu \geq E_g$ where E = Energy gap in eV, h = Plancks constant, c = velocity of light in vacuum and Λ is the wave length of the incident photon. Hence, to satisfy the above condition for absorbtion, the material for p-i-n diode is chosen accordingly to absorb most of the incident energy from fiber optic channel. InGaAs p-i-n diodes have been investigated because of their low dark current and good temperature dependent characteristics. The properties of InGaAs are listed in the table, in appendix.

The photodetector structure is depicted in fig.3.2. InGaAs, a III-V compound, severs as an optimum material for photon absorbtion in the desired wave length range. This hetrojunction photodiode is formed by depositing large bandgap material on a small bandgap semiconductor. Advantages of hetrojunction photodiodes are the quantum efficiency does not depend on the distance of the junction from the

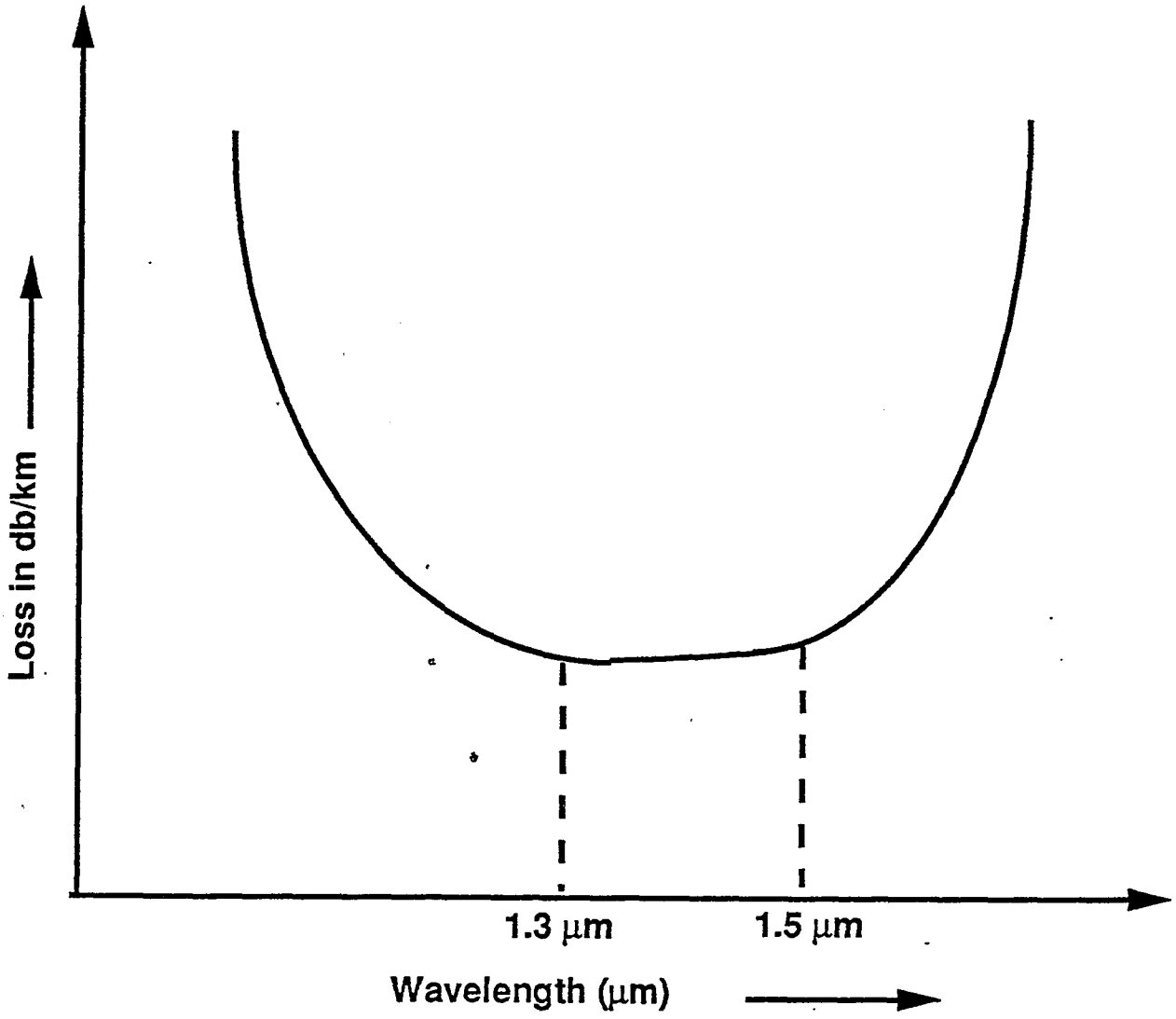


Figure 3.1: Ideal graph of loss in dbs/km vs wavelength.

surface and it can provide unique material combination so that quantum efficiency and the response speed can be optimized for a given range of optical wavelength. To obtain a hetrojunction with low leakage currents, the lattice constant of the two semiconductors should be closely matched. InGaAs epitaxially grown on a InP film forms perfectly matched lattice to reduce all possible types of dark currents.

3.3 PHOTODETECTOR STRUCTURE:

The energy gap of InGaAs is .75eV which is sufficient to absorb the photon energy in the 1.3 to 1.55μm wavelength range. As shown in fig.3.2, the thickness of the absorbing layer is 2μ = 20,000$\mathring{A}$ which forms the intrinsic layer of a p-i-n- diode. This region separates the P and N electrodes of a p-i-n diode. InP has large band gap of 1.35eV and hence cannot absorb any radiation of the required range and hence is optically transparent. These P^+ & N^+ regions in InP have thickness of 1000$\mathring{A}$. The Nitride layer of thickness 200nm is the antireflection coating. This Nitride layer is deployed to increase the depletion region thickness which eventually optimizes the quantum efficiency. The use of 100$\mathring{A}$ InGaAs layer (see fig.3.2)is to avoid reaction of ammonia (NH_3) and silane (SiH_4) which are the reaction agents in the fabrication process. The junction is localized by the P^+ region which defines the device area for light absorbtion.

3.3.1 p-i-n diode fabrication:

The fabrication steps for the p-i-n detector are as follows [14].

1. Deposition of 200nm thick SiN_4 layer using Plasma Enhanced Chemical Vapour Deposition (PECVD).

2. Detector active area definition by photolithography and subsequent removal of nitride from the area thus defined.

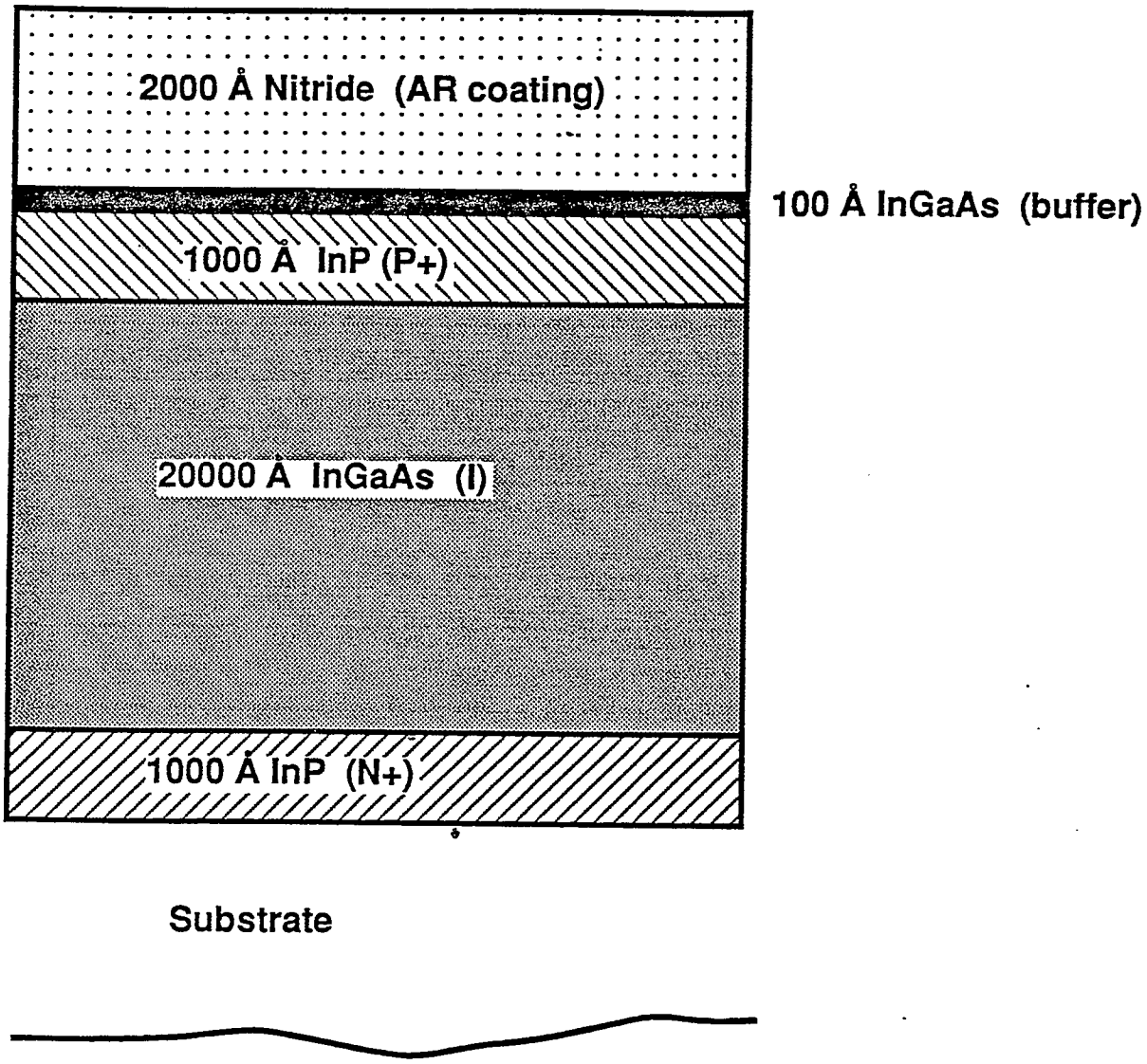


Figure 3.2: Photodetector structure.

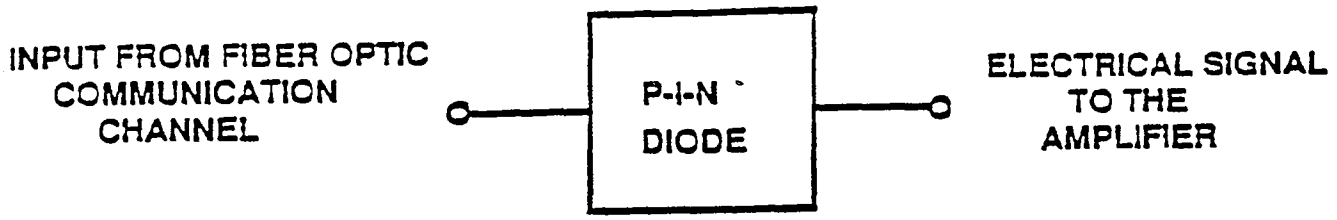


Figure 3.3: Block diagram of photodetector.

3. Deposition of six monolayers of cadmium arachide film by Langmuir-Blodgett technique [15].

4. Removal of hydrocarbons from LB deposited Cd-Ar film by oxyplasma processing.

5. Deposition of 200nm thick SiO_2 cap by PECVD on both sides of the substrate.

6. Diffusion of cadmium into the substrate at 600 C in an argon ambient.

7. Ohmic contact formation to the top p-type layer by photolithography, Cr/AuZn/Au evaporation lift-off and alloying.

8. Backside ohmic contact formed by lithography, gold plating and lift-off.

The p-i-n diode fabricated by the above steps is reverse biased and the absorbed photons generate electron-hole pairs to make the current to flow.

3.4 FRONT-END-AMPLIFIER:

Front end amplifier is the next stage of the OEIC and it is shown in fig.3.4. The front end amplifier is basically divided into following stages.

1. Pre-amplifier-(cascode stage)
2. Source follower.
3. High impedance stage. (Output stage).

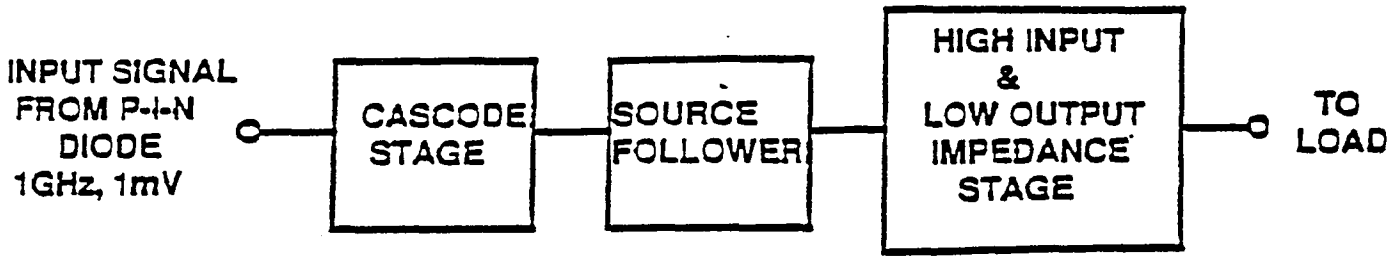


Figure 3.4: Block diagram of a Front end amplifier.

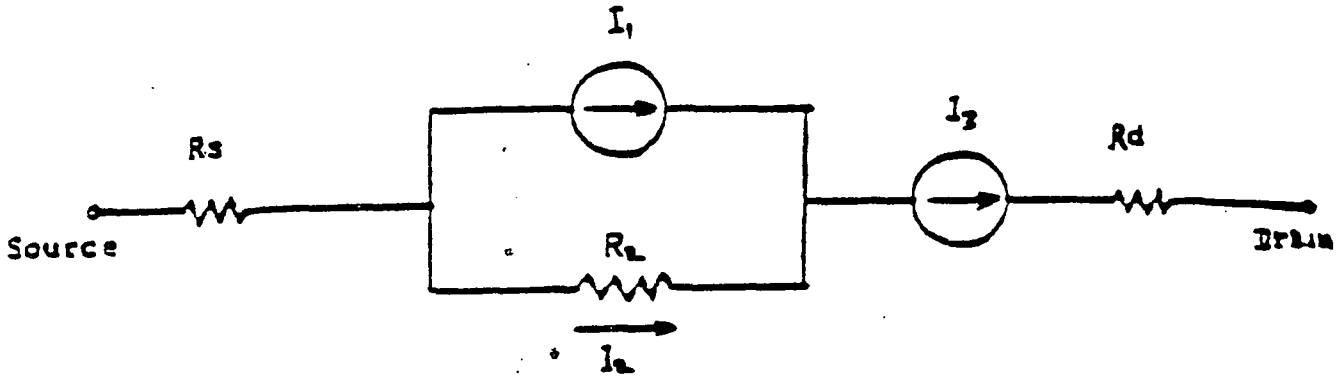


Figure 3.5: Equivalent circuit of GaAs MESFET [16].

The front end amplifier consists of GaAs MESFETs, Diodes, a feedback resistor and parasitic & body capacitances (explained in sec3.7.1). The GaAs MESFETS used are of depletion mode meaning these MESFETs are normally on. The threshold voltage is taken to be -1.6v and the length of these GaAs devices is 1μ and the widths of these devices are calculated as explained in section 3.4.1. The MESFETs considered in the pre-amplifier stage exhibit I-V characteristics as shown in fig.3.5 and the parameters of these MESFETs are given below. Equivalent circuit of a GaAs MESFET is shown in fig.3.5.

GaAs MESFET PARAMETERS AT 300 K:

1. Doping density = $N_D = 10^{17} cm^{-3}$

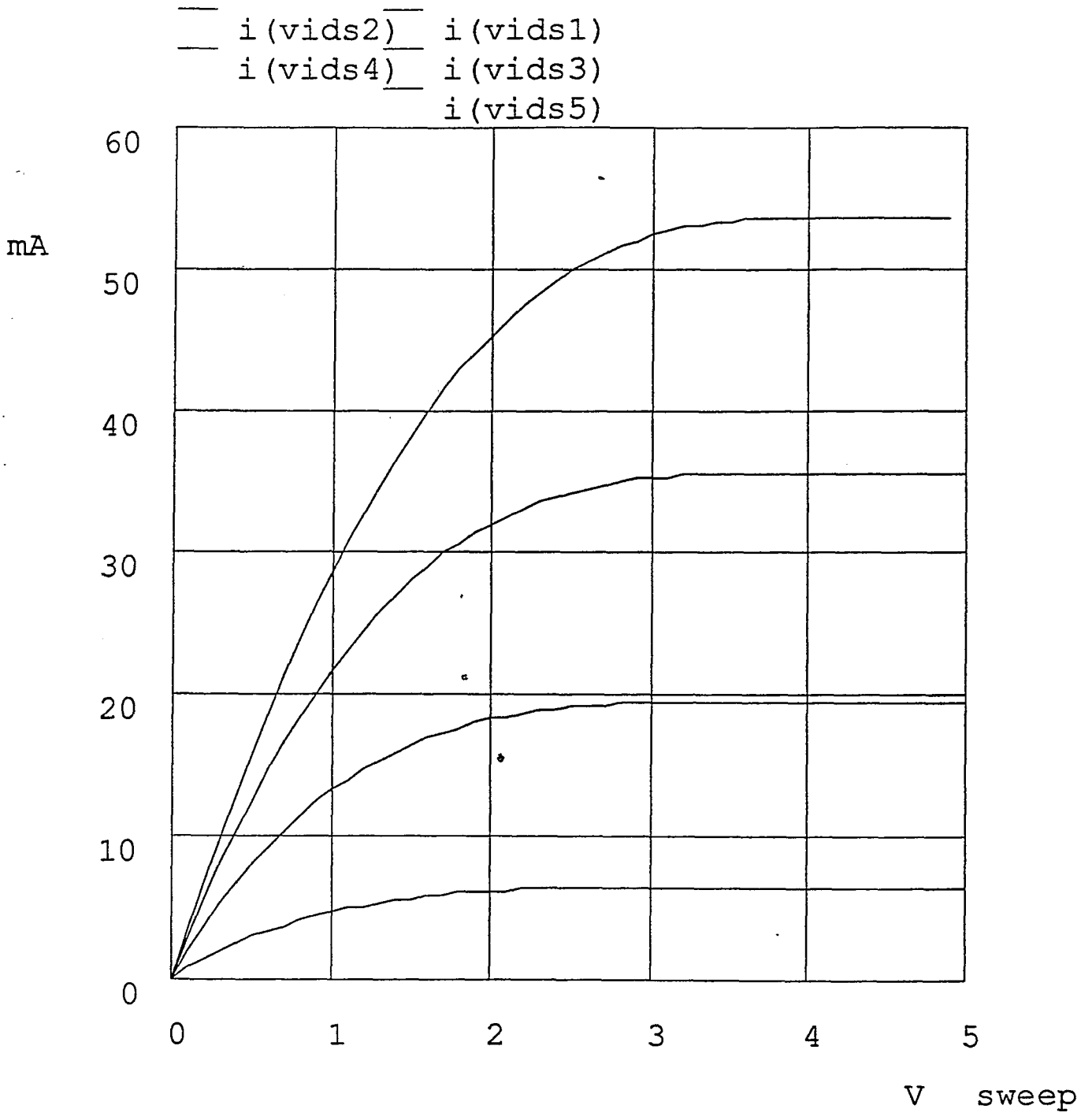


Figure 3.6: I-V charactristics of a MESFET.

2. Gate length = L = 1μm.

3. Gate widths = W = 50, 100, 200 μm.

4. Built in potential = V_{bi} = 0.7volts.

5. Saturation velocity = $V_s = 10^7$m/s

6. Mobility = μ_n = 5000 cm^2/V-cm

7. Source resistance = 2 Ω/mm.

8. Drain resistance = 2 Ω/mm.

9. I_{DSS} Saturation channel current = 130 mA/mm

11. Pinch off voltage = V_P = -1.6 volts.

12. C_{gs} = 0.1 pf/100μm.

13. C_{gd} = 0.1 pf/100μm.

14. Transconductance = g_m = 135 mS/mm

15. Energy gap = E_g = 1.42 eV.

16. Intrinsic carrier concentration = $n_i = 2.25 \times 10^{-6} cm^{-3}$

17. Conductivity = $\rho_i = 3.0 \times 10^{-9} (\Omega.cm)^{-1}$

3.4.1 Explanation of parameters:

The doping density of the channel is considered to be $10^{17} cm^{-3}$.

The gate length of the depletion mode MESFET is 1μm.

Calculation of gate width:

The Gate width calculation of the MESFET is based on the transconductance (β) parameter value used in SPICE input. The following equations are used to determine the MESFET gate width.

Where ϵ_s = Dielectric permitivity = 1.16 $\times 10^{-12}$ F/cm.

a = Channel thickness = 0.182 $\times 10^4 \mu$m. (by calculations)

N_c = Density of states in the conduction band = $4.7 \times 10^{17} cm^{-3}$

Now by solving equations 2.9, 2.11, 3.1 & 3.7 and substituting the values of the required parameters we get the relations as given below.

$$I_{dss} = \beta(V_{gs} - V_T)/\ 1 + b(\ V_{gs} - V_T) \tag{3.1}$$

where b = Doping tail extending parameter = 0.3volts.

W = $[2.27 \times 10^4]\beta\mu$m.

Calculation of diode width:

The diode width is determined by the SPICE parameter I_s which is the saturation current of the diode in Amp. The equation which is used to find the relationship between I_s and the diode width is given below.

$$I_s = W_d\ a\ A^*T^2e^{-\phi_{Bn}/KT} \tag{3.2}$$

where W_d = diode width in μm.

a = Channel thickness = $0.182 \times 10^4\mu$m.

A^* = 1.2 × Richardson constant = 8 amp/$cm^2.K^2$

T = Absolute temperature in degree kelvin.

and ϕ_{Bn} = Diode junction potential = 0.7 volts.

Now, by substituting these values in eqn.3.2, we get the following relation between the diode width and the diode saturation current.

$$W_d = [\ 3.81 \times 10^{14}]\ I_s \mu m. \tag{3.2}$$

There are parasitic capacitances involved in the MESFET. Capacitance between gate & source (C_{gs}) and gate & drain (C_{gd}) are given below [12].

$$C_{gs} = C_{gso}/(1 - V_{gs}/V_{bi})^{1/2} \tag{3.3}$$

$$C_{gd} = C_{gdo}/\ (1 - V_{gd}/V_{bi})^{1/2} \tag{3.4}$$

where

$$C_{gso} = C_{gdo} = \mathrm{WL}/2\ (\ \epsilon q N_D/2V_{bi})^{1/2} \tag{3.5}$$

C_{gso}&$C_{gdo}$are the capacitances at zero gate to drain & gate to source voltage respectively. The total capacitance (C_{go}) is equal to the capacitance of the space charge region depleted by the built in potential and is given by,

$$C_{go} = \epsilon WL/A = \mathrm{WL}\ (\ \epsilon q N_D/2V_{bi})^{1/2} \tag{3.6}$$

The above capacitance gets equally divided between the source (C_{gso}) and drain (C_{gdo}) because the space charge distribution is symmetrical. For non zero V_{ds} & V_{gs}, the capacitances C_{ds} & C_{gs} behave almost as the capacitance of equivalent schottky diode connected between the gate and source. Now, from eq.3.5 it is seen that these capacitances are functions of width, length, & channel doping [17].

$$\beta = I_{ds}/V_T^2 = 2\epsilon\mu V_s \mathrm{W/A}(\mu V_{po} + 3V_s L) \tag{3.7}$$

From eq.3.7, it is also seen that β increases with decrease in device thickness and increase in doping concentration. This is accomplished by similar increase in device capacitances C_{gs} and C_{gd}. However, thin & highly doped layers should lead to higher speed of operation. In GaAs MESFET, the conducting channel is confined on one side by space charge region and on the other side by semi-insulating region. Under normal operating conditions, the gate to source capacitance is very much larger than the gate to drain capacitance. At zero drain to source voltage, both capacitances are about equal.

For constant channel doping, the saturated drain current I_{ds} varies as,

$$I_{ds} = \mathrm{W}V_{sat}(2\ \epsilon q N_D)^{1/2} * (\ \mathrm{X} - \mathrm{Y}\ ) \tag{3.8}$$

where,

$$X = [V_t + V_{bi}]^{1/2}$$

and

$$Y = (V_{gs} + V_{bi})^{1/2}$$

where W is the channel width, V_{sat} is the saturated electron velocity and is given by,

$$V_{ds} = E_{sat} * L$$

where L is the channel length, E is the dielectric constant, q is the electron charge, N_D is the donor density, V_T is the threshold voltage and V_{bi} is the built in potential. Near pinch-off voltage,

$$I_{ds} = \beta(V_{gs} - V_T)^2 \tag{3.9}$$

The transconductance (g_m) is given by,

$$g_m = 2\ \beta(V_G - V_T) \tag{3.10}$$

Considering all the above equations, device parameters are calculated and are shown in fig3.8.

3.5 CIRCUIT DESCRIPTION:

The OEIC circuit diagram is shown in fig.3.7. The optical signal from fiber optic communication channel of 12GHz frequency is sensed by a photodetector. This signal is then converted into an electrical signal of 1mv, 1GHz frequency which is

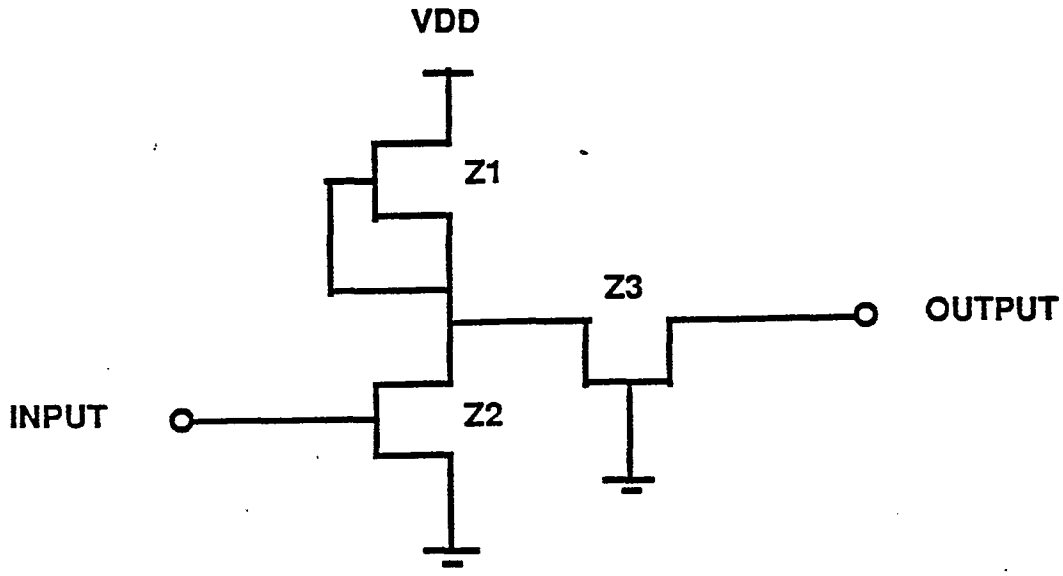


Figure 3.7: Cascode stage connection.

the input signal to the front end amplifier. This signal is amplified in the first stage i.e. the cascode stage The cascode connection is shown in fig.3.6.

It has Z1, Z2, Z3 as its components. Z1 is the load of the cascode connection Z2 and Z3. The cascode connection means the drain of one of the MESFETs which is in common source configuration is connected to the source of another MESFET which is in common gate configuration. This circuit configuration was originally developed to achieve improved high frequency performance in amplifiers. It not only improves the output to input isolation but also greatly improves the high frequency stability by reducing the feedback capacitance within the amplifier stage. This amplified electrical signal is fed to the high impedance stage through a source follower (Z4). Source follower is the MESFET whose gate and source are shorted. When this MSEFET is ON, it represents just a resistor. The high impedance stage consists of Z5 & Z6 and is in common drain configuration. It has three diodes included to reduce the voltage to operate the next MESFET i.e Z7 at required bias as obtained from the I-V characteristics, to get equal swings of the output. The output stage

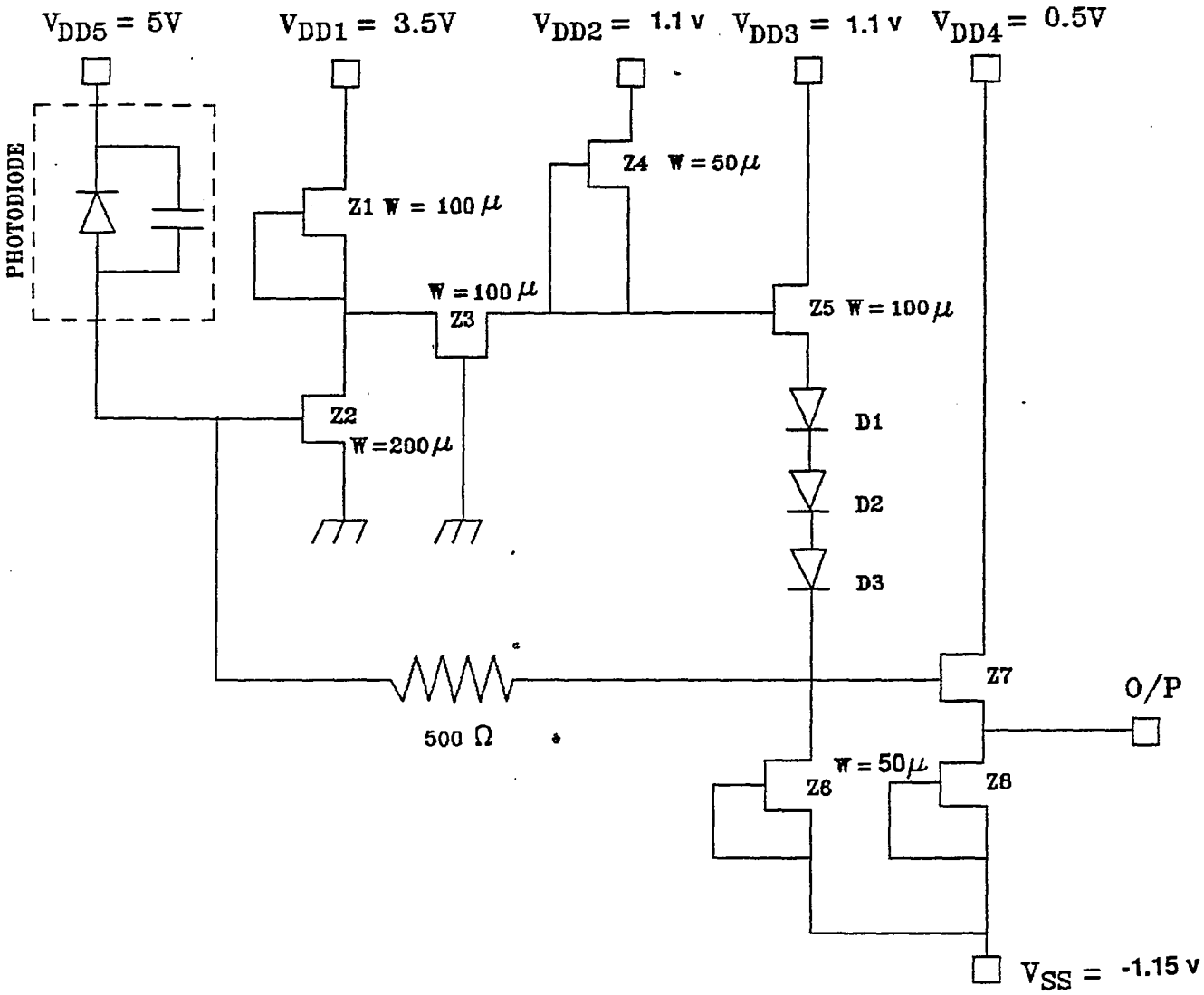


Figure 3.8: OEIC circuit diagram.

is also connected in common drain configuration, just because this has very high input impedance and low output impedance which affects the effective load of OEIC which normally is the transmission line with impedance of 500Ω.

The basic advantages of GaAs devices in the integrated circuit technology are [21];

1. high electron mobility which leads to smaller transit time due to minimum series resistance.

2. high saturation velocities resulting in increased cut off frequencies.

3. decreased parasitic capacitance.

4. semi-insulating Gallium Arsenide (SI GaAs) substrate offers a natural electrical isolation between active devices (high band gap 1.42eV., resistivity approaching $10^7\Omega$-cm.

3.6 FABRICATION TECHNIQUE:

The capability of GaAs devices to operate at high speeds has lead to increasing interest in integrating these devices on inexpensive substrates such as silicon. However, attempts have been made to achieve this with GaAs substrates but the fabrication technique becomes expensive and complicated as compared with Si substrates. The fabrication technique suggested has been hetroepitaxial growth of GaAs/AlGaAs on Si.

There are some intrinsic problems involved in hetroepitaxial growth such as large lattice mismatch resulting in a large density of dislocations. This can be reduced by a thick buffer layer or by selective area growth. Stresses from thermal expansion mismatch cannot be eliminated completely. This also makes the fine line lithography technique difficult. The alternate method for this is the epitaxial lift-off [2], in which the appropriate epitaxial structure is selectively removed from GaAs

substrate and is re-attached with Van der Waal forces to a new substrate.

3.6.1 Van der Waal bonding forces:

In epitaxial lift off technique, the adherence property of epitaxial film is of most importance. The epitaxial film tends to adhere to any smooth surface. This surface could form a permanent bond without the need of any adhesives. There can be three types of bonds possible - ionic, covalent and metallic. The Van der Waal bonding is due to the presumed role of interfacial forces. These bonds are weaker than the above three. Van der Waal bonds have following advantages [22];

1. Adherence can be achieved without any adhesives and makes the thermal processing of the bonded films at normal semiconductor processing temperatures easily possible. However, most adhesives could not tolerate these temperatures

2. Very close contact between the film and the substrate is possible for good thermal conduction.

3. For highly doped semiconductors an ohmic contact between the film and the substrate is the most important parameter. A low ohmic resistance is a good characteristic of an ohmic contact. This is possible only if the tunnel barrier is thin enough to allow electrical conduction. Van der Waal forces reduce the thickness of the adhesive to allow minimum ohmic resistance.

Normally, a Van der Waal bonding between GaAs film and Si substrate appears as shown in the fig.3.9

Since, in an integrated circuit, many devices are involved, it becomes difficult to lift off every device separately and make interconnections on another substrate. An alternate method to do this is to transfer completely the grown film on to another substrate and then fabricate devices there. The processing steps followed to fabricate GaAs MESFET are as follows [14].

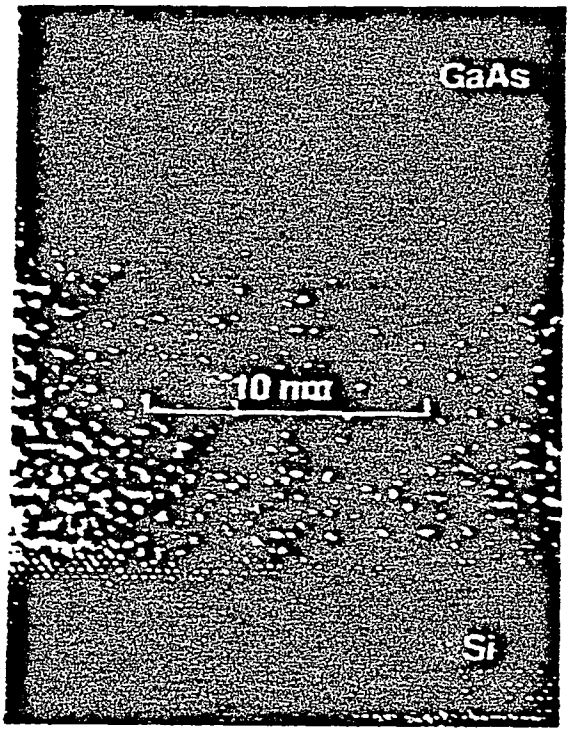


Figure 3.9: Van der waal bonding in Si & GaAs substrates [22].

1. AlAs film is grown on GaAs substrate with a sacrificial AlAs layer.
2. The sample is waxed and the AlAs is selectively removed in HF.
3. The film is detached from the parent substrate.
4. Deposit Silicon Nitride or SiO_2 on silicon substrate.
5. The detached film from GaAs substrate is then kept on the SiO_2/Si or Si_3N_4/Si.
6. This is kept to dry so that Van der Waal forces act on it to form permanent bonds with the surface.
7. Wax is removed.
8. Mesas are chemically etched.
9. Ohmic contacts are made to the dielectric layer.
10. The gates are formed by a gate recess etch.
11. Gate metal is deposited on it.

All the above steps are explained in fig.3.9

3.7 FABRICATION OF OEIC:

Fig.3.9 explains the basic technique followed in fabrication of GaAs devices on SiO_2 substrate. In fabrication of OEIC, first the photodetector is fabricated on InP substrate as explained in sec3.3.1. Then SiO_2 is grown epitaxially on this structure.

The epitaxial growth process is a means of depositing a thin layer (0.5 to 20 μm.) of single crystal material upon the surface of a single crystal substrate. If the film is the same material as the substrate the process is called homoepitaxy. If, on the other hand, the deposit is made on a substrate that is chemically different, the process is termed as heteroepitaxy. The term epitaxy is derived from Greek word meaning 'arranged upon'. Epitaxial growth can be achieved from the Vapor Phase (VPE), Liquid Phase (LPE) or Solid Phase (SPE). Liquid phase deposition has found its widest use in producing epitaxial layers of III-V compounds.(eg. GaAs,InP). In this epitaxial growth the epitaxial layer thickness is a critical parameter and therefore must be accurately measured and controlled [32].

SiO_2 layer serves the purpose of dielectric. This layer also prevents the shorting of MESFETs, which will be fabricated on this by hetroepitaxial lift off technique and the underneath photodiode. After growing SiO_2 of 1.5μm thickness, MESFETs are fabricated on this layer using the processing steps in sec.3.6. The detached film from GaAs substrate is kept on this SiO_2 layer and the fabrication steps are followed. The ohmic contacts to these are made by forming a window. Hence every MESFET structure forms a capacitor of which, one plate is the MESFET itself and the other is the photodetector. SiO_2 layer in between these two behaves as an intrinsic layer of the capacitor as shown in fig3.11.

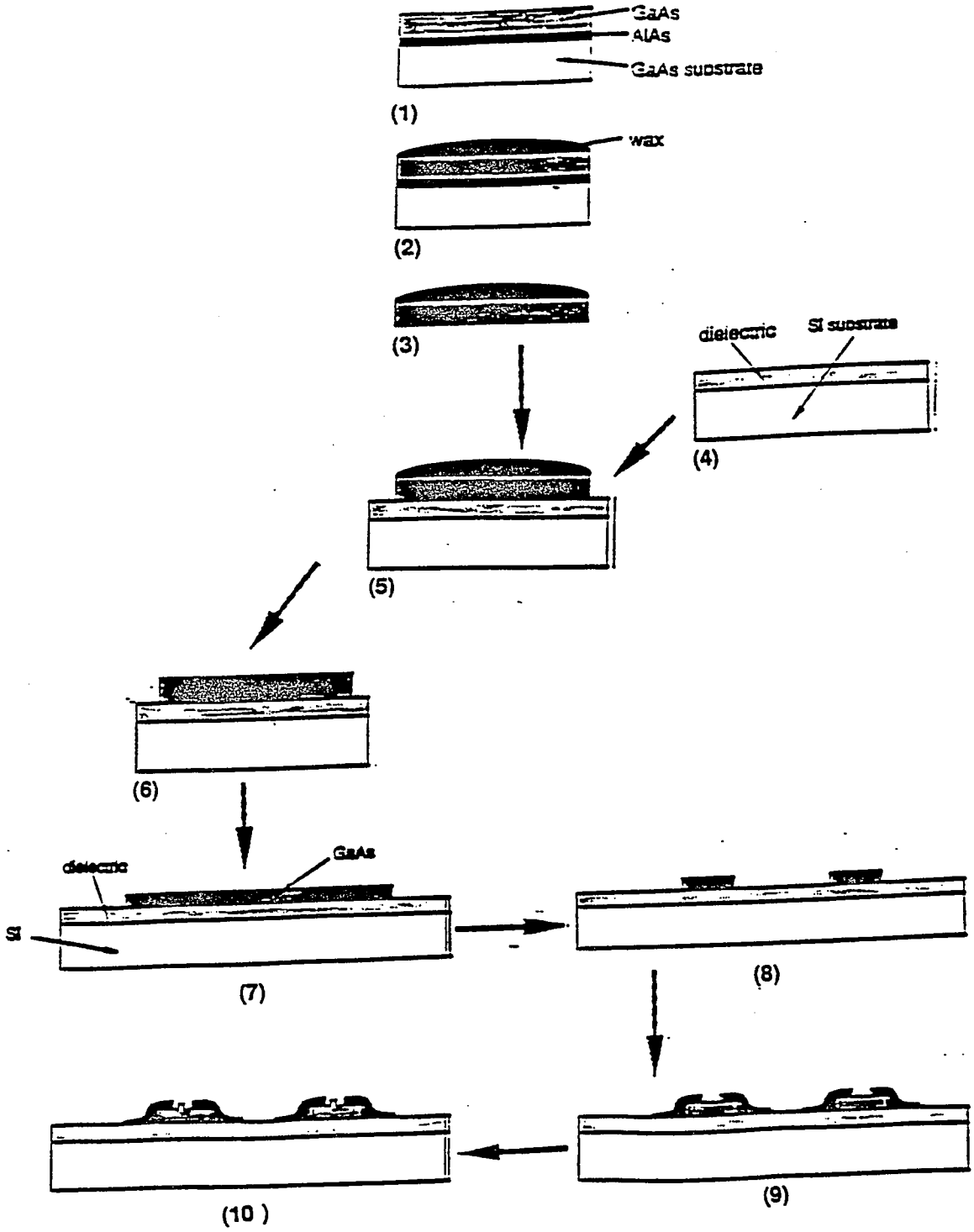


Figure 3.10: GaAs MESFET fabrication using liftoff technology [14].

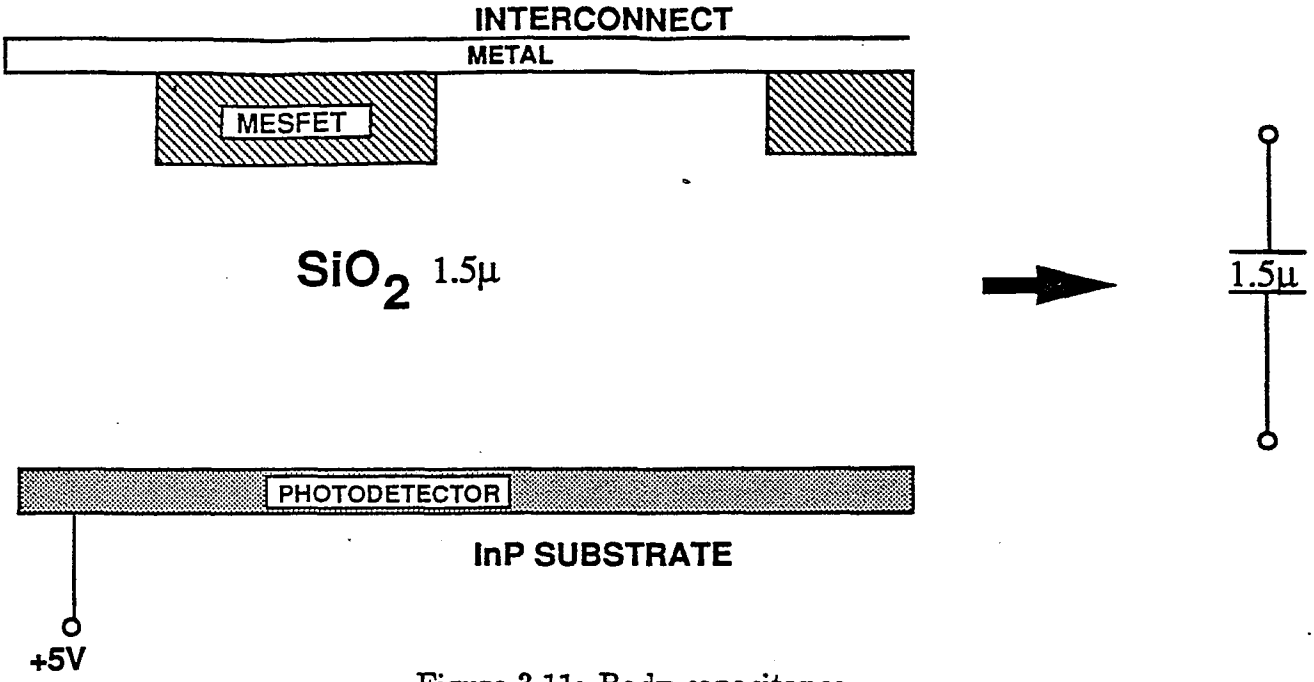


Figure 3.11: Body capacitance.

3.7.1 Body capacitance

This capacitance formed by MESFET, SiO_2 and p-i-n diode is known as a 'body capacitance'. It plays an important role in high frequency analysis. The value of this is calculated by using following equation.

$$C = \epsilon_{ox} A/d \tag{3.11}$$

Where C is the Body capacitance, ϵ_{ox} is the dielectric permitivity which is given by $\epsilon \times \epsilon_0$ where ϵ is the dielectric constant and ϵ_0 is the permitivity in vacuum. The value of dielectric constant is 3.9. A is the area of the device and is calculated from the layout [14]. d is 1.5μm, which is the thickness of the SiO_2 layer. Now substituting these values of ϵ_{ox}, A and d values of body capacitances are calculated and are shown in the table in fig.3.12

NOTE :

Length of the device (MESFET) = 40 μ

Thickness of dielectric = 1.5 μ

Length of the device (Diode) = 125 μ

* From layout C3 +C5 = .184 pf

$$C = \frac{\varepsilon_{ox} A}{d}$$

MESFETs #	width μ	Area μ2	C pf
Z1	100 μ	$4X10^3$ μ2	.092 pf
Z2	200 μ	$8X10^3$ μ2	.184 pf
Z3 * C3	100μ	$4X10^3$ μ2	.092 pf
Z4	50 μ	$2X10^3$ μ2	.046 pf
Z5 *C5	100 μ	$4X10^3$ μ2	.092 pf
Z6	50 μ	$2X10^3$ μ2	.046 pf
Z7	200 μ	$8X10^3$ μ2	.184 pf
Z8	100 μ	$4X10^3$ μ2	.092 pf
D1,D2,D3	20 μ	$5X10^3$ μ2	.115 pf

Figure 3.12: Body capacitance values

Chapter 4

SPICE SIMULATION

4.1 INTRODUCTION:

In any integrated circuit design, circuit simulation plays an important role. After completing a proper design of the circuit, before fabricating or implementing it, one usually starts with the computer simulation of the circuit to be built. In computer simulation, facilities have been provided to represent the required circuit in terms of a program. The desired input & output can be observed on the terminal and the necessary changes can be made in design to get the required output. If the circuit consists of not more than few hundred devices, then the well known software SPICE, originally developed at the University of California, Berkeley is often used. SPICE is a general purpose circuit simulation program which accepts a description of a circuit and provides several forms of accurate and detailed simulation including

small signal ac, dc, and time domain transient solutions. Versions of this program have been in use for almost more than twenty years. Normally SPICE is avaliable in UNIX, VMS, MS-DOS and IBM tapes environment. SPICE can model the required devices at different levels of complexity and usually gives the output with great reliability. It was written originally for Si devices, but now the recent versions of SPICE also defines GaAs devices. The SPICE3 version is based on SPICE2G.6. The most recent version of SPICE is SPICE3D.1 which has some excellent facilities to work in Xwindows to plot the required curves and to perform frequency analysis. This is the improved version of SPICE3C.1 which can be run in NJIT only on Ultrix environment.

4.2 REQUIRED MODELS IN OEIC:

4.2.1 GaAs MESFET model :

SPICE has excellent facility to have built in models for the semiconductor devices. The user needs to specify only the pertinent model parameter values. The GaAs MESFET model is based on FET model of Shichman and Hodges and is shown in fig.4.1.[30] [31].

Often, many devices in a circuit are defined by the same set of device model parameters and hence are defined on a separate .model cards. These cards are assigned a unique model name. To run any SPICE program, the device element card has to refer to the specific model name. Each device element contains the device name, the nodes to which the device is connected and the device model name. In addition, optional parameters which makes the device to behave different than the default models in SPICE may be specified. The optional parameters may be the geometric factors and an initial conditions. In MESFET, the area of the

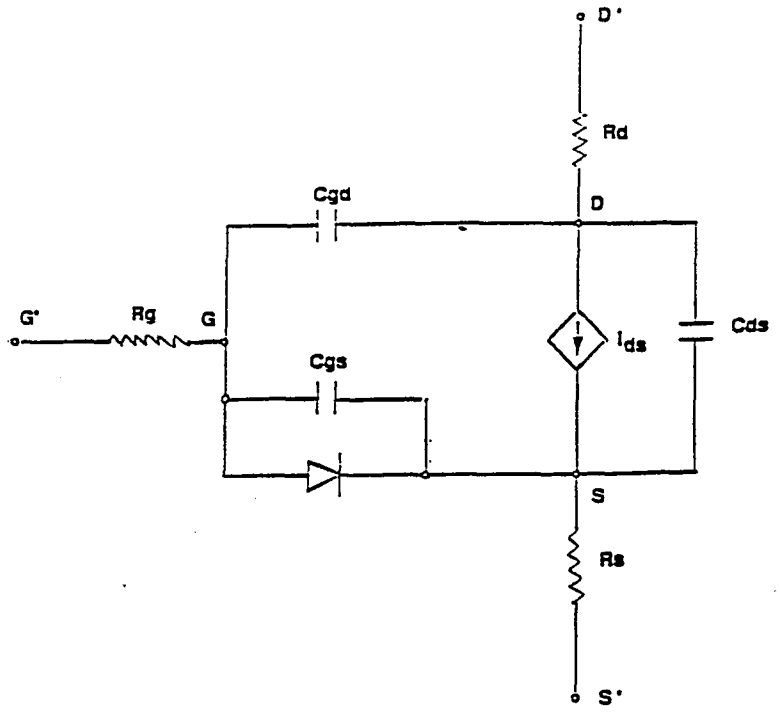


Figure 4.1: Schichman and Hodges GaAs model.

device has to be specified for SPICE to consider its length & width. Two different forms of initial conditions may be specified either 'on' or 'off'. Since the MESFETs considered in the OEIC are depletion mode devices, these will refer to normally 'on' MESFET. Hence, we don't have to specify the initial condition.

The general form to represent a MESFET in SPICE is as follows.

$$ZxND, NG, NS, MNAME < AREA >< OFF > \tag{4.1}$$

where Zx is the MESFET, ND, NG and NS are the drain, gate and source nodes respectively. MNAME is the device model name, AREA defines the area of the device and OFF represents the initial condition of the device for dc analysis.

The MESFET model in SPICE3 is derived from the GaAs FET model of Statz et. al. and is given in fig.4.1. The dc characteristics of MESFET are defined by the parameter VTO, the doping tail extending parameter b and beta, which determines the variation of drain current with respect to the gate voltage. ALPHA determines the saturation voltage and LAMBDA refers to the output conductance. Two ohmic

resistances RD and RS are also included. Charge storage is modeled by total gate charge as a function of gate-drain and gate-source capacitances and is defined by C_{gd} and C_{gs} parameters.

The main dissimilarity in GaAs & Si devices is the electron saturation velocity. In GaAs, the electron velocity saturates near 3×10^3 V/cm which is rather low as compared with Si because for Si the value is almost 10 times larger. In GaAs, the saturation of the drain current with increasing drain voltage is caused by carrier velocity saturation where as in Si based devices it is the channel pinch off that causes the drain current to saturate. The drain current in SPICE is calculated by the following equation.

$$I_d = \beta \, (\, V_{gs} - V_T)^2 \, (\, 1 + \lambda V_{ds}) \, \tanh(\alpha V_{ds}) \tag{4.2}$$

where, I_d is the drain current, β is a transconductance parameter, V_{gs} is gate to source voltage, V_{ds} is the drain to source voltage, V_T is the threshold voltage, λ is the parameter related to drain conductance & α determines the drain current. The saturation of the drain current considers the effect of channel doping density [Ref. eqn. 3.8]. The transconductance at any point is approximately inversely proportional to the distance between the gate and the channel edge [30].

The parameters considered for SPICE simulation of the OEIC are as given in the program and the results are compared with the parameters defined by default in SPICE. These can be compared by I-V characteristics of the MESFET using both the parameters as shown in fig.4.2. The SPICE program and the circuit diagram for I-V characteristics are also listed. The I-V curves show the difference in saturation currents and the pinch-off voltage.

Vgs in volts. , I_{dss} in mA

Volts / mA	- 1.6V	- 1.2V	- 0.8V	- 0.4V	0.0V
Default RS,RD	.357	1.29	2.64	4.32	6.25
RS=40,RD=40	0.0	3.69	9.6	16.2	23.2
RS=20,RD=20	0.0	5.09	14.3	25.1	36.8
RS=10,RD=10	0.0	6.40	19.41	35.5	53.4

Figure 4.2: Comparison of saturation currents

4.2.2 GaAs diode model:

The general form of a GaAs diode is as shown below.

$$DxN + N - MNAME < AREA > \tag{4.3}$$

where, Dx is the diode, N+ & N- are the positive and negative nodes of a diode. MNAME is the model name & AREA is the area of the diode. The diode characteristics are determined by the saturation current (IS) and coefficient (N). An ohmic resistance RS is included and the junction potential is the most important parameter in calculation of the width of the diode as explained in eqn.3.2 and is denoted by VJ (ϕ_{Bn})

4.2.3 Resistors & Capacitors:

General form of representing a resistor in SPICE is given by,

$$RxN1N2[Value] \tag{4.4}$$

where, Rx is the resistor, N1 and N2 are the two nodes of the resistor and [Value] is the resistance in ohms.

General form of a capacitor is as given.

$$CxN + N - [Value] \tag{4.5}$$

where, Cx is the capacitor, N+ N- are the positive and Negative nodes resp. and [Value] is the capacitance.

4.2.4 Independent Sources:

The input signal which is an independent source is assigned a time dependent value for transient analysis. There are five independent source functions avaliable in

SPICE3 such as Pulse, Exponential, Sinusoidal, Piece-wise linear and Single frequency FM. In OEIC, the pulse input is made use of and has the general form as given below

$$VxN1N2PULSE(V1V2TDTRTFPWPER) \tag{4.6}$$

where, Vx is the voltage source, N1 & N2 are the node numbers through which the input is applied, PULSE represents the pulse input, V1 & V2 are the initial and pulsed values of the input respectively, TD is the initial time delay in sec.; by default it is considered to be zero., TR & TF are the rise and fall times respectively. in sec., PW denotes the pulse width & PER is the period of the input signal which can be calculated by the frequency of the input signal. VDD & VSS are the independent dc voltage sources which are defined in following way in SPICE.

$$VDDN1N2[dcvalueinvolts] \tag{4.7}$$

Where N1 & N2 are the positive and negative nodes respectively. Note that voltage sources need not be grounded. In OEIC VDD & VSS values are measured with respect to ground.

4.3 SPICE simulation of OEIC:

Considering all the rules of SPICE3 and the general form of the devices included in OEIC, as shown in fig3.9, its SPICE simulation is performed in the following way.

Represent the OEIC circuit given in fig.3.8 in the program. The first step is to represent all the possible nodes by respective numbers and then considering the values of independent voltage sources, MESFET, diode & capacitors, the SPICE program is written as shown in fig.4.2 and the transient analysis is performed. Taking into consideration the voltages limitations of GaAs MESFET, VDD is considered to be not more than 3.5volts and VSS is adjusted to get the proper biasing

of MESFETs. The output & input waveforms of OEIC are given. The effects of C_{gs} & C_{gd} and body capacitances are also shown by the respective waveforms. The variation in the output with respect to the position of the body capacitances either in drain, gate, or source is given in fig.4.3

Following steps are followed to run SPICE3 in Ultrix:

1. Write the SPICE program in tex.

2. > SPICE : SPICE directory is created from the system.

3. SPICE3.1 > source [file name] : Creates the file to be run in SPICE directory and reads commands from the file name. Lines beginning with the character * are comments and are ignored.

4. SPICE3.2 > run : SPICE3 will run the requested analysis and will prompt again upon finishing. Data will be avaliable in the form of active nodes, voltage conditions of the required nodes at that the requested time, asciiplot of voltage vs time interval of the node of interest and the dataplot. All the above mentioned plots are achieved as follows:

A. SPICE3.3 > display [v(node no.)] will print the summary of currently active nodes

B. SPICE3.4 > asciiplot [v(node no.)] gives the asciiplot of the requested node w.r.t time.

C. SPICE3.5 > plot [v(node no.)] creates a xwindow (only the terminal has the facility) plots the dataplot w.r.t time.

NOTE:

If different plots of node with respect to some other nodes are made on the same axis. The respective node numbers are separated by commas.

eg. plot v(3), V(9), V(11)

will plot voltage graphs of node 3, 9, 11 on the time axis.

```
          #----------INPUT PROGRAM OF OEIC-----------#

**OptoElectronic Integrated Circuit Reciever**

************** Supply voltages ****************
vdd1 1 0 3.5v
vdd2 5 0 1.1v
vdd3 12 0 1.1v
vdd4 13 0 0.5v
vdd5 14 0 5.0v
vss1 10 0 -1.15v
************** Input signal from the p-i-n diode ************

vin 3 0 pulse(0v 1mv 0ns .05ns .05ns .5ns 1ns)

************** GaAs MESFETs ( Cascode & source follower configuration )********

z1 1 2 2 dfet1 area=100
z2 2 3 0 dfet2 area=200
z3 2 0 4 dfet1 area=100
z4 5 4 4 dfet3 area=50
z5 5 4 6 dfet1 area=100

************* Parasitic ( Body ) Capacitances **********

c1 2 14  0.092pf
c2 3 14  0.184pf
c3 0 14  0.184pf
c4 4 14  0.046pf
cd 6 14  0.345pf
c6 10 14 0.046pf
c7 9 14  0.184pf
c8 10 14 0.092pf

***************** Diodes to drop the voltage *****************

d1 6 7 diode area=2500
d2 7 8 diode area=2500
d3 8 9 diode area=2500

**************** Feedback Resistor **************
r1 9 3 500ohms

**************** Output Stage MESFETS ****************

z6 9 10 10 dfet3 area=50
z7 13 9 11 dfet2 area=200
z8 11 10 10 dfet1 area=100

*************** Internal Gate-source ( Cgs ) Capacitances **********

cgs1 2 2 0.1pf
cgs2 3 0 0.2pf
cgs3 2 0 0.1pf
cgs4 4 4 0.05pf
cgs5 4 6 0.1pf
cgs6 10 10 0.05pf
cgs7 9 11 0.2pf
cgs8 10 10 0.1pf

************* Internal Gate-Drain ( Cgd ) Capacitances **********

cgd1 2 1 0.1pf
cgd2 3 2 0.2pf
cgd3 4 0 0.1pf
```

```
cgd4 4 5 0.05p
cgd5 12 4 0.1pf
cgd6 9 10 0.05pf
cgd7 13 9 0.2pf
cgd8 11 10 0.1pf

******************** GaAs SPICE models *************

.model dfet1 nmf  (vto=-1.6v rs=20 rd=20 alpha=1v beta=.0625 pb=0.6 b=0.3)
.model dfet2 nmf (vto=-1.6v rs=10 rd=10 alpha=1v beta=.0625 pb=0.6 b=0.3)
.model dfet3 nmf (vto=-1.6v rs=40 rd=40 alpha=1v beta=.0625 pb=0.6 b=0.3)
.model diode D ( vj=0.7 is=10E-13 rs=15 )

****************** Transient output response *************

.tran .2ns 2ns
.print tran v(3) v(9) v(11)
.plot v(3) v(9) v(11)
.width out = 100
.end
```

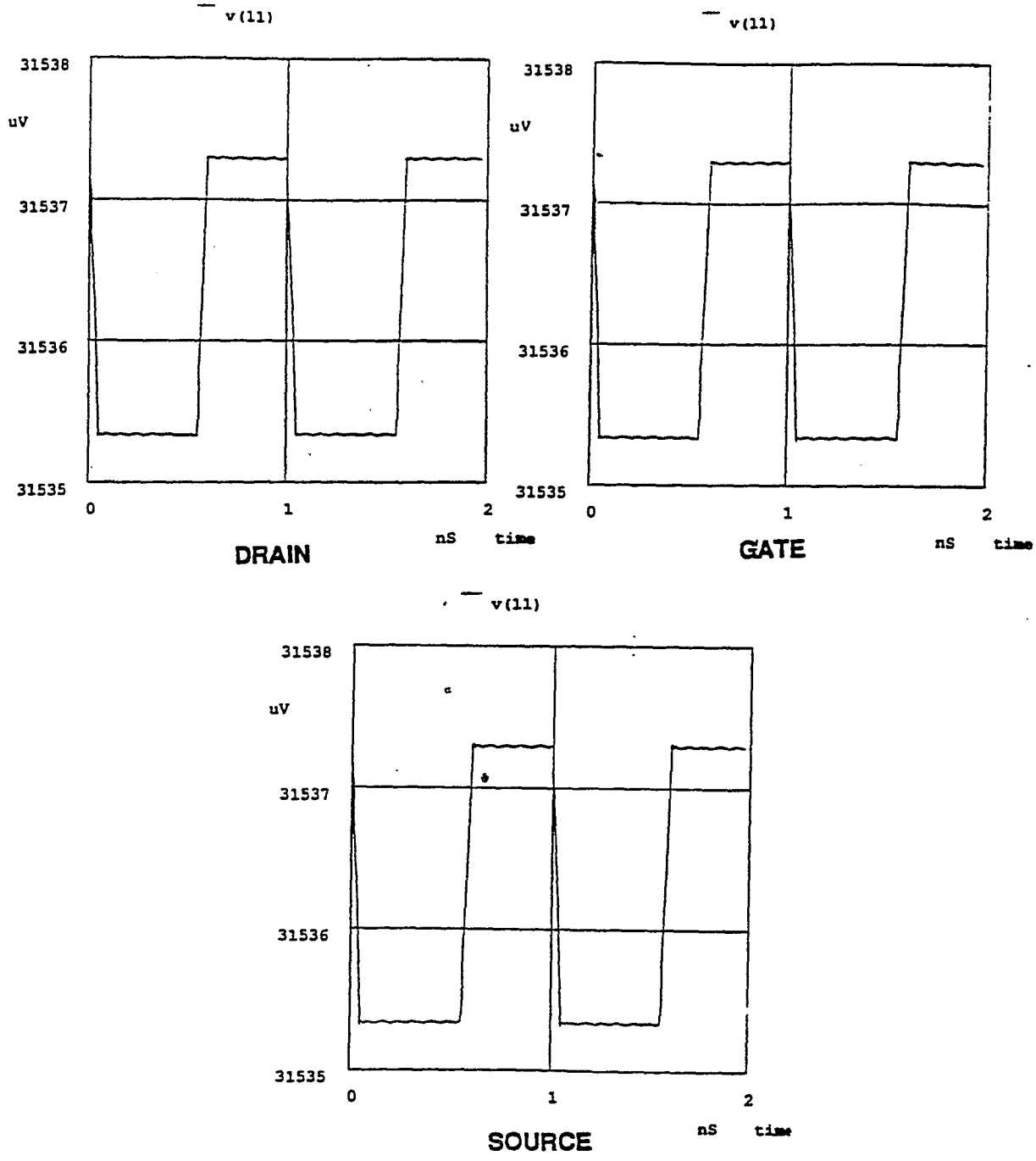
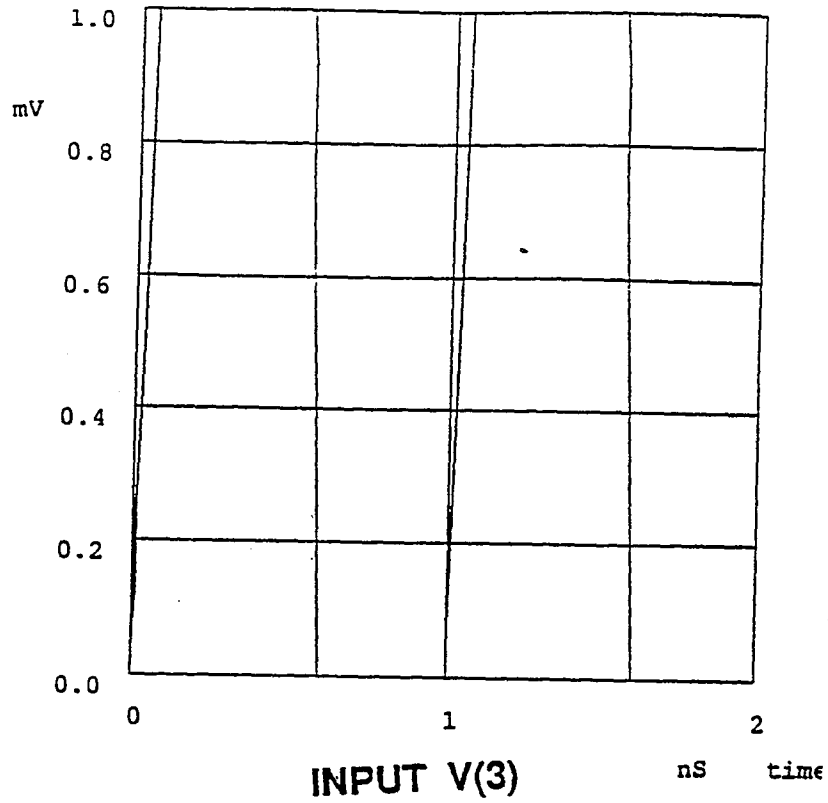
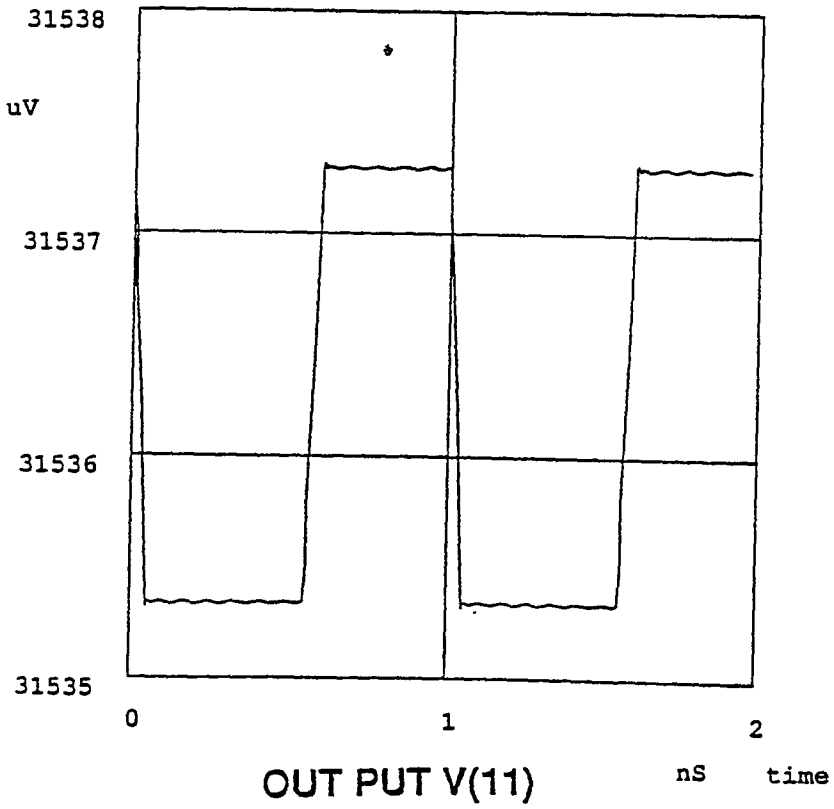


Figure 4.3: Variation in output w.r.t. position of body capacitance



INPUT V(3)

v(11)



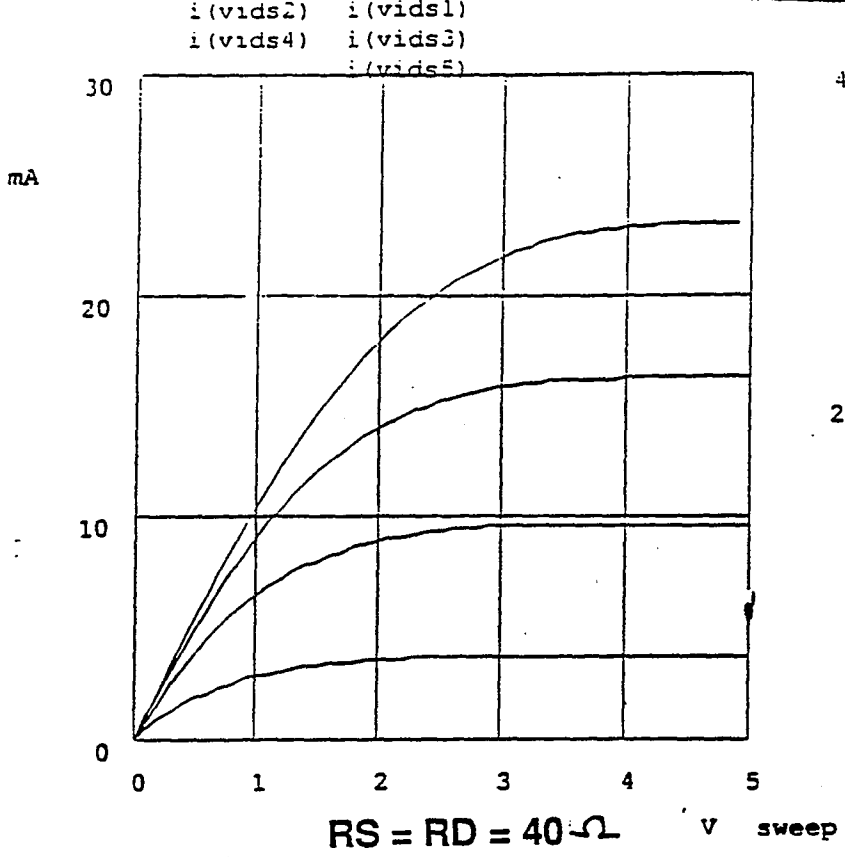
OUT PUT V(11)

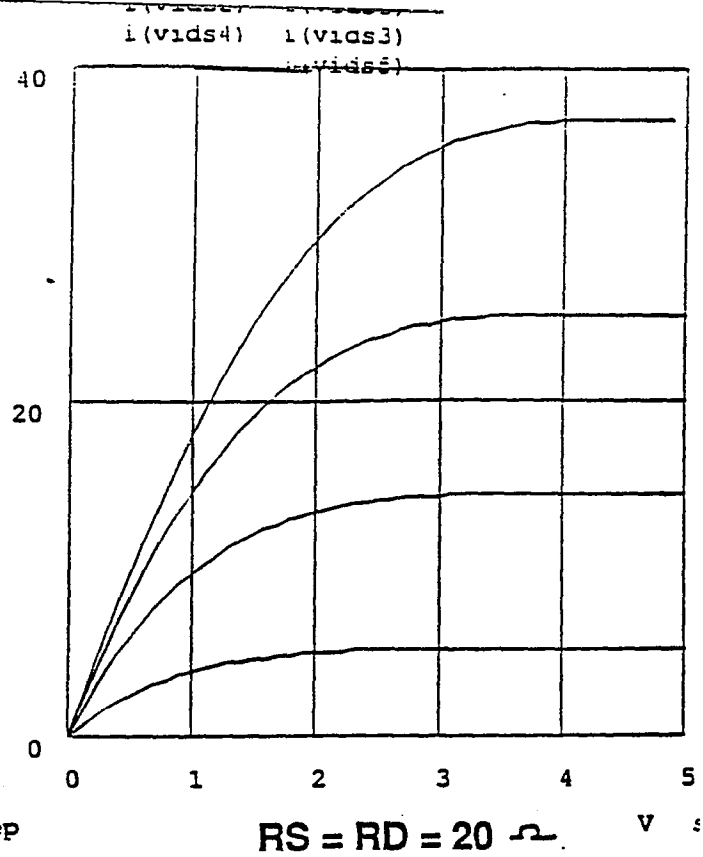
#---------- INPUT PROGRAM OF I-V CHARACTERISTICS ---------#

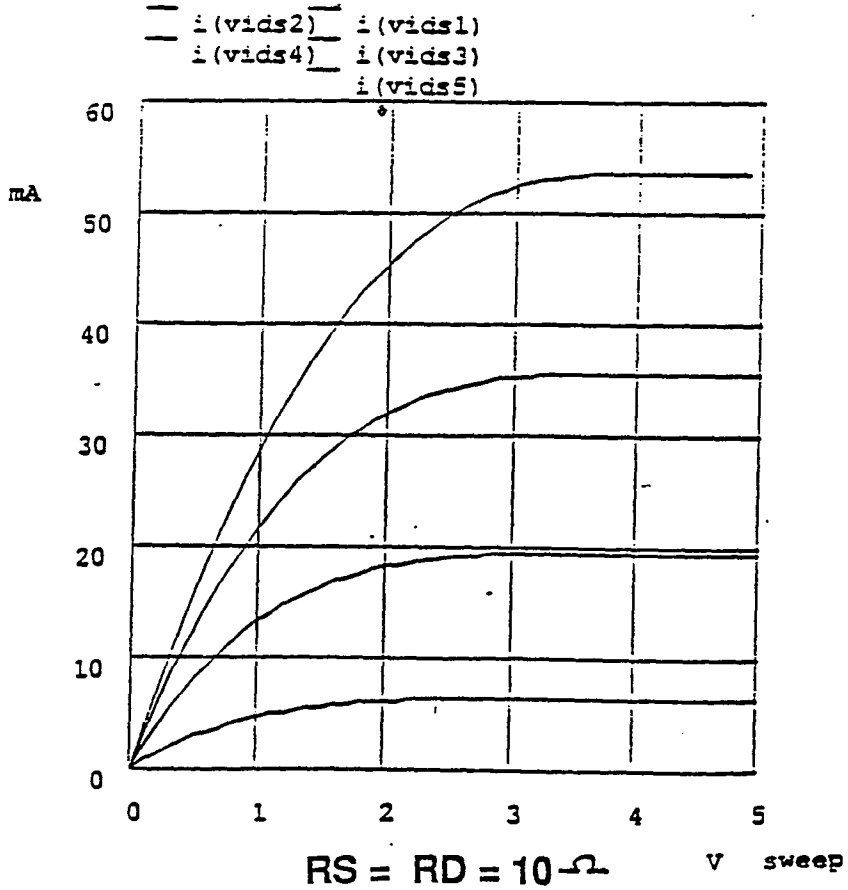
```
* i-v characteristics of GaAs MESFET
vdd 1 0
vgs 2 0 -1.4v 1.0v 0.2
vids 3 0 0V

z1 1 2 3 dfet
.model dfet nmf (vto=-1.6v rs=20 rd=20 alpha=1v beta=0.0625 pb=0.6 b=0.3)

.dc vdd 0.0 5.0 .1
.print dc v(1) v(2) i(vids)
.end
```


i(vids2) i(vids1)
i(vids4) i(vids3)
i(vids5)
mA
30
20
10
0
0 1 2 3 4 5
RS = RD = 40Ω
V sweep


i(vids4) i(vids3)
i(vids5)
40
20
0
0 1 2 3 4 5
RS = RD = 20Ω
V


i(vids2) i(vids1)
i(vids4) i(vids3)
i(vids5)
mA
60
50
40
30
20
10
0
0 1 2 3 4 5
RS = RD = 10Ω
V sweep

4.4 Conclusion:

Within experimental errors, these SPICE results are expected to be compatible with the actual OEIC chip after fabrication.

Chapter 5

HIGH FREQUENCY ANALYSIS

5.1 INTRODUCTION:

Any amplifier can be analysed in two ways by performing its small signal low frequency as well as high frequency analysis. This is done by calculating the transfer function of the system of interest and its response at low and high frequencies. The stability of the system can be found out by calculating its poles and zeros from the transfer function. The transfer function may consists of contributions from parasitic capacitances, internal resistances and the transconductance. These parameters depend upon the system. In this discussion, OEIC is the system which has GaAs MESFETs as its components. The GaAs MESFET small signal equivalent circuit is shown in the fig.5.1. At low frequencies, the parasitic capacitances in the circuit behave differently than at high frequencies. At low frequencies they don't exhibit

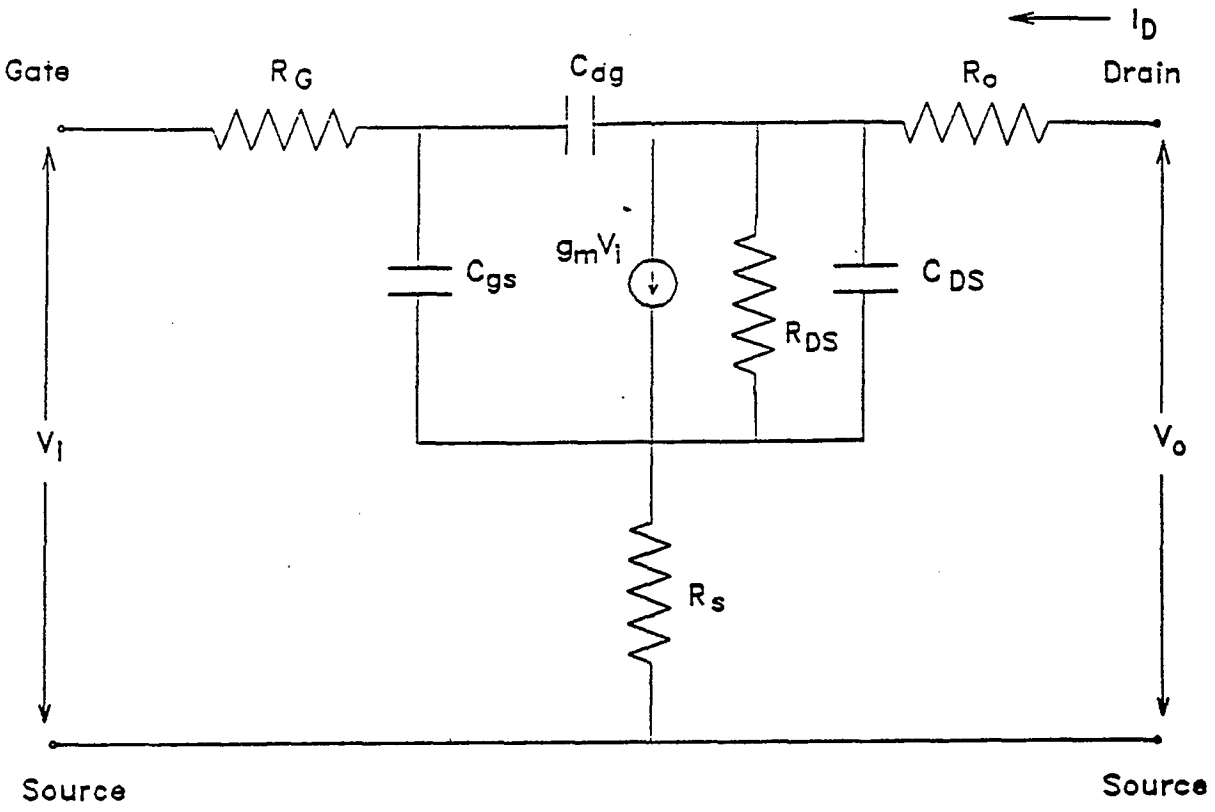


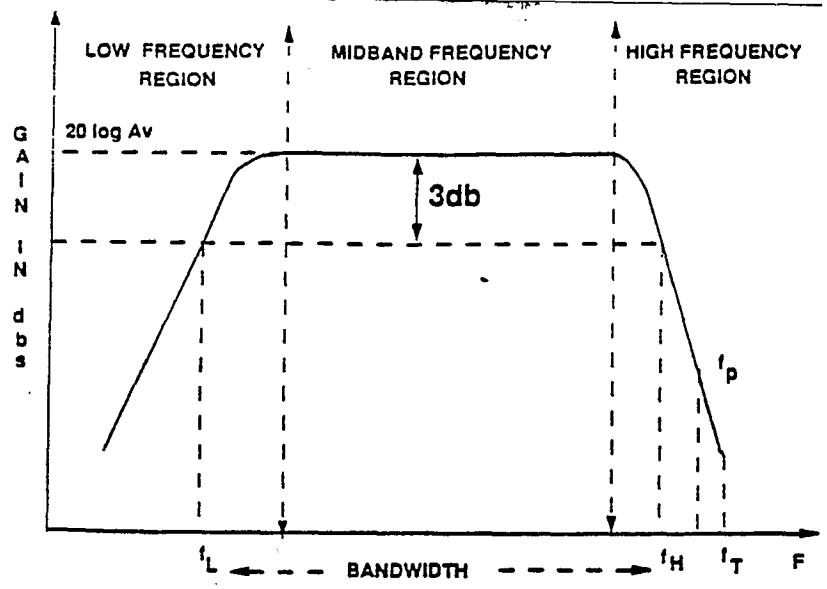
Figure 5.1: Small signal equivalent circuit of a MESFET.

any significant impedance, but at high frequencies, they become the dominant poles which decide the stability of the system.

Amplification can be analyzed by considering its effects in the required frequency range (i) low frequency region, (ii) midband frequency region, (iii) high frequency region. In low frequency region, the amplifier behaves like a high pass circuit and the response increases with increase in frequency and the output approaches to zero at f=0. In the midband frequency region, the amplification is reasonably constant. In high frequency region, the amplifier stage behaves as a low pass circuit by decreasing the response with increase in frequency as shown in fig.5.2.

5.1.1 Explanation of the terms used in frequency analysis:

1. 3 db frequency:



NOTE : dbs = 20 log | Av

Figure 5.2: Frequency response of an amplifier

Low frequency region:

$$A_{L(jf)} = A_v / \sqrt{[1 + (f_L/f)^2]} \tag{5.1}$$

At f=f_L, $A_{vL} = 1/\sqrt{2} = 0.707$ where as in midband region $A_{vL} = 1$.

Hence f_L is that frequency at which the gain falls down to 0.707 times its midband value(A_o). This drop in signal corresponds to a decibel reduction of 20log$1/\sqrt{2}$ or 3db and f_L is referred to as lower 3-db frequency.

High frequency region:

$$A_{H(jf)} = A_v \; / \; \sqrt{[1 + (f/f_H)^2]} \tag{5.2}$$

In high frequency region at f=f_H gain reduces by $1/\sqrt{2}$ times its midband value and F_H is known as upper 3db frequency.

Band width:

Frequency range from F_L to f_H is called the bandwidth.

Gain-bandwidth product:

Gain-bandwidth product is the product of gain of the amplifier in midband region and its bandwidth.

Figure of merit:

Figure of merit is used to compare the high frequency performance of the amplifier and is given by $g_m/2\pi C_{in}$

The major parameter required in the frequency analysis is the transfer function of the circuit of interest. Transfer function (A_v) is the ratio of the output voltage (V_o)to the input voltage(V_i) i.e. $A_v = V_o/V_i$. The transfer function of the multistage amplifier is given by the product of individual voltage gains.

The stability of the circuit depends upon the number of poles & zeros of the response. Stability of the circuit means, for small change in input signal there should not be large fluctuations in the output signal. i.e its tendency to oscillate. Since s=j2πf with f=f_p where f_p is the frequency equal to the frequency of the pole. f=f_z where f_z is the frequency of the zero. A single zero transfer function is unrealistic because it indicates a response which increases without limits. Hence a practical circuit has a transfer function consisting of one or more poles and zeros. A transfer function with number of poles are larger than number of zeros indicates a practical circuit. If, in a transfer function, which has several poles determining high frequency response and smallest of these frequencies is f_{p1} and each of the other pole is atleast two octaves higher (f/f_p = 2) then the amplifier behaves essentially as a single time constant circuit whose 3db frequency is f_{p1}. f_{p1} is known as the dominant pole [28].

5.2 TRANSFER FUNCTION OF OEIC:

As explained in chapter(3), OEIC has three stages (i) Cascode stage (ii) Source follower (iii) High impedance stage. The term cascode describes an amplifier stage

consisting of a common source stage, followed by a common gate stage. The MESFET Z_1 is the load for the common source and the source follower behaves as the load for the common gate configuration. The first stage i.e. common source, has very low input impedance and large gain. For this reason, this stage is normally at the input of the amplifier. The common gate configuration also has high voltage gain and low input impedance. Hence, the overall gain of the cascode is the product of these two voltage gains. The source follower does not contribute to the gain. The output stage is the common drain configuration. This stage has high input impedance and the most importantly it has very low output impedance. Gain incurred by this is very much low and hence the total gain of the OEIC is because of the cascode stage.

Every stage of OEIC has C_{gs}, C_{gd} and body capacitance C_{sn}. Each of them contribute to find the frequency of the pole. These capacitances can be minimized by metallization.

5.2.1 Transfer function:

Calculations for the transfer function are started from the last stage of OEIC. The reason for this is, it is connected to the load whose value is known. This helps in finding the input impedance of this stage.This input impedance is in parallel with the parasitic capacitance of the previous stage, which eventually gives the output impedance of this stage and so on. The input impedance of the cascode stage can hence be found out.

5.2.2 Common drain configuration (stage 4 of OEIC):

This is the output stage of the OEIC and has very low output impedance & high input impedance. The gain involved in this stage is negligible.

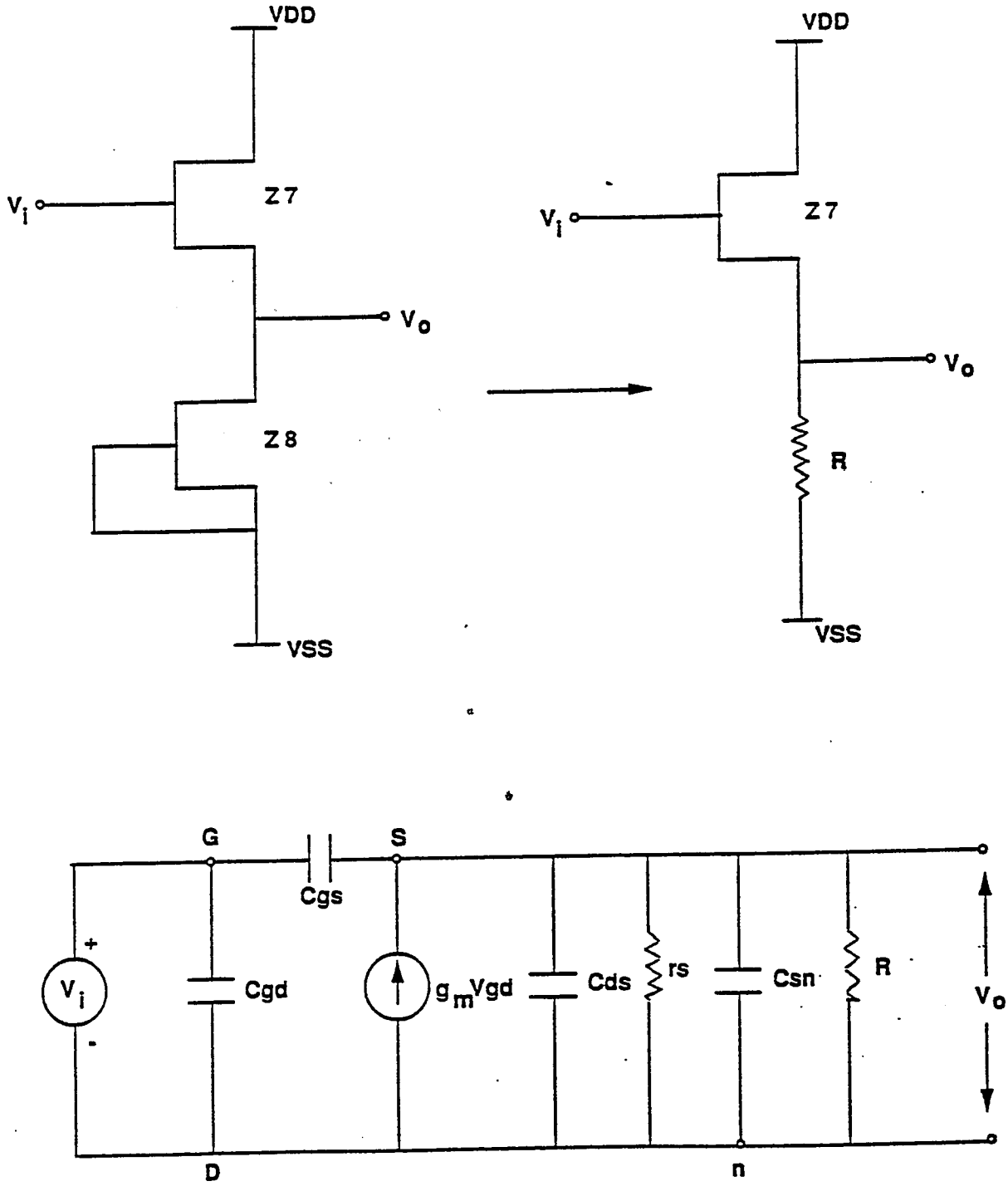


Figure 5.3: Stage 4 of OEIC & its small signal equivalent circuit

From fig.5.3 we have

$$g_m V_{gs} = -j\omega C_{gs} V_{gs} + (1/r_s + 1/R + j\omega C_T)\, V_o \tag{5.3}$$

where $C_T = C_{gs} + C_{ds} + C_{sn}$

Now solving the above eqn.5.3. for $A_{v4} = V_o/V_i$ we get

$$V_o/V_i = A_{(v4)} = g_m + j\omega C_{gs}/\ (1/r_s + 1/R + j\omega C_T) \tag{5.4}$$

zero calculation:

From eq.5.4. we get,

$$g_m + j\omega C_{gs} = 0 \tag{5.5}$$

$$S_{0(4)} = j\omega = -g_m/C_{gs} \tag{5.6}$$

pole calculation:

From eq.5.4. we get,

$$S_{p4} = j\omega = -(r_d^{-1} + R^{-1})/\ C_T \tag{5.7}$$

Input admittance : $y_i = j\omega C_{gd} + j\omega C_{gs}(1\text{-}A_{v4}) + J\omega C_T$

Output admittance : $y_o = y_{gd} + j\omega C_T$

Previous stage to this is also in a common drain configuration with some voltage drop incurred. This voltage is introduced to operate MESFET 7 near its Q point at -0.5v. This is achieved by the use of diodes in series as shown in fig 5.4. Each diode in on condition represents a resistor.

5.2.3 Common drain configuration (stage 3 of OEIC):

From figure 5.4 the nodal equation is written as,

$$g_m V_{gs} = -j\omega C_{gs} V_{gs} + (1/r_s + j\omega C_T + 1/[R_1 + R_2]) V_o' \tag{5.8}$$

where $C_T = C_{gs} + C_{ds} + C_{sn}$ and $V_o' = V_o/R_2 \times R_1 + V_o$

Now substituting the above eqs. and solving it for A_v we get the same transfer function as equation 5.4, except for the change due to voltage drop incurred by diodes. The total resistance of three diodes is represented by R_1.

$$A_{(v3)} = g_m + j\omega C_{gs}/ (1/r_s + 1/R_1 + R_2\ j\omega C_T) \times (1 + R_1/R_2) \tag{5.9}$$

zero calculation: From eq. 5.9, we get

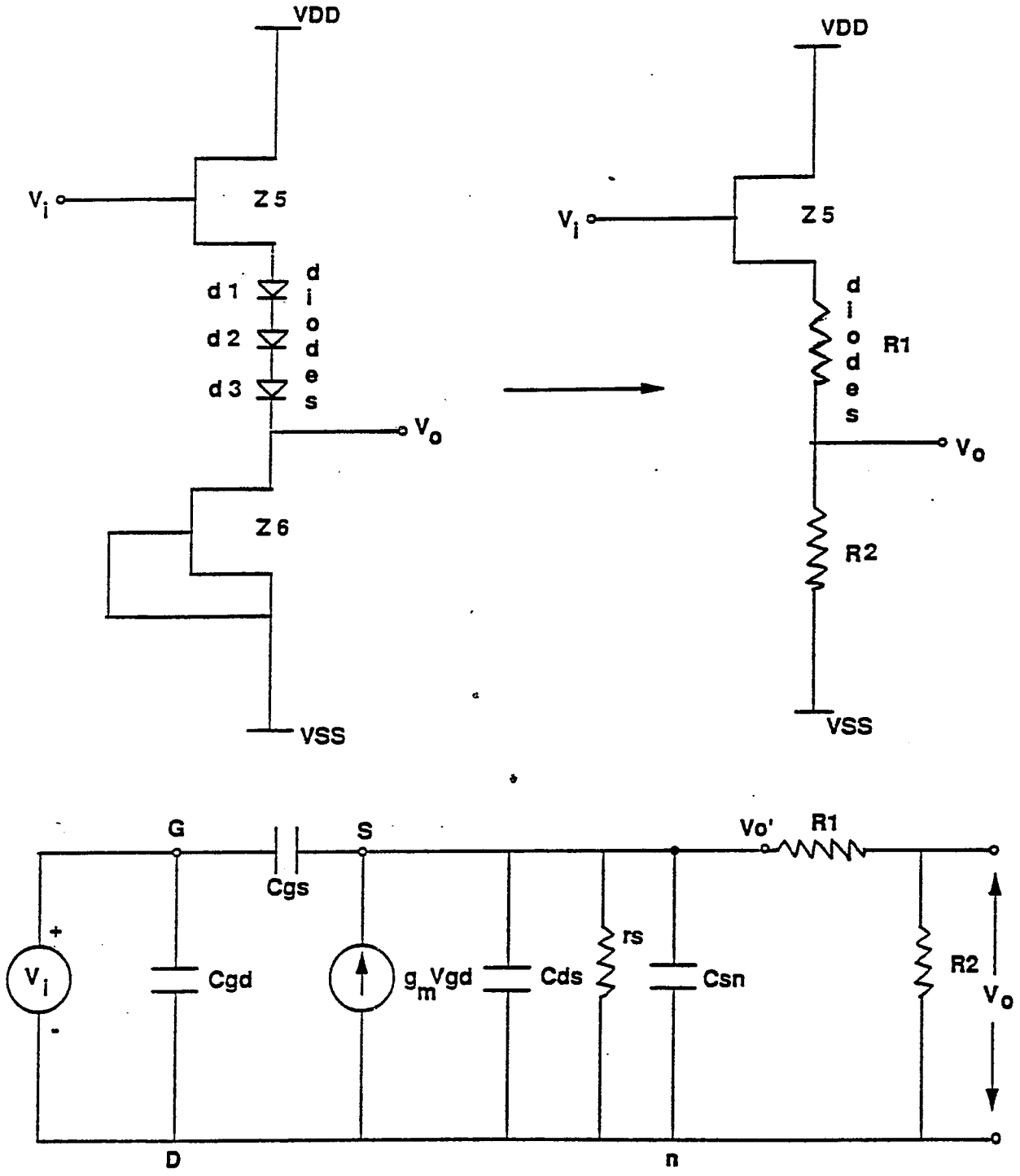


Figure 5.4: Stage 3 of OEIC & its small signal equivalent circuit

$$g_m + j\omega C_{gs} = 0 \tag{5.10}$$

$$S_{03} = -g_m/C_{gs} \tag{5.11}$$

pole calculation: From eq. 5.9, we get

$$S_{p3} = j\omega = -\left[(r_d)^{-1} + (R_1 + R_2)^{-1}\right]/ C_T \tag{5.12}$$

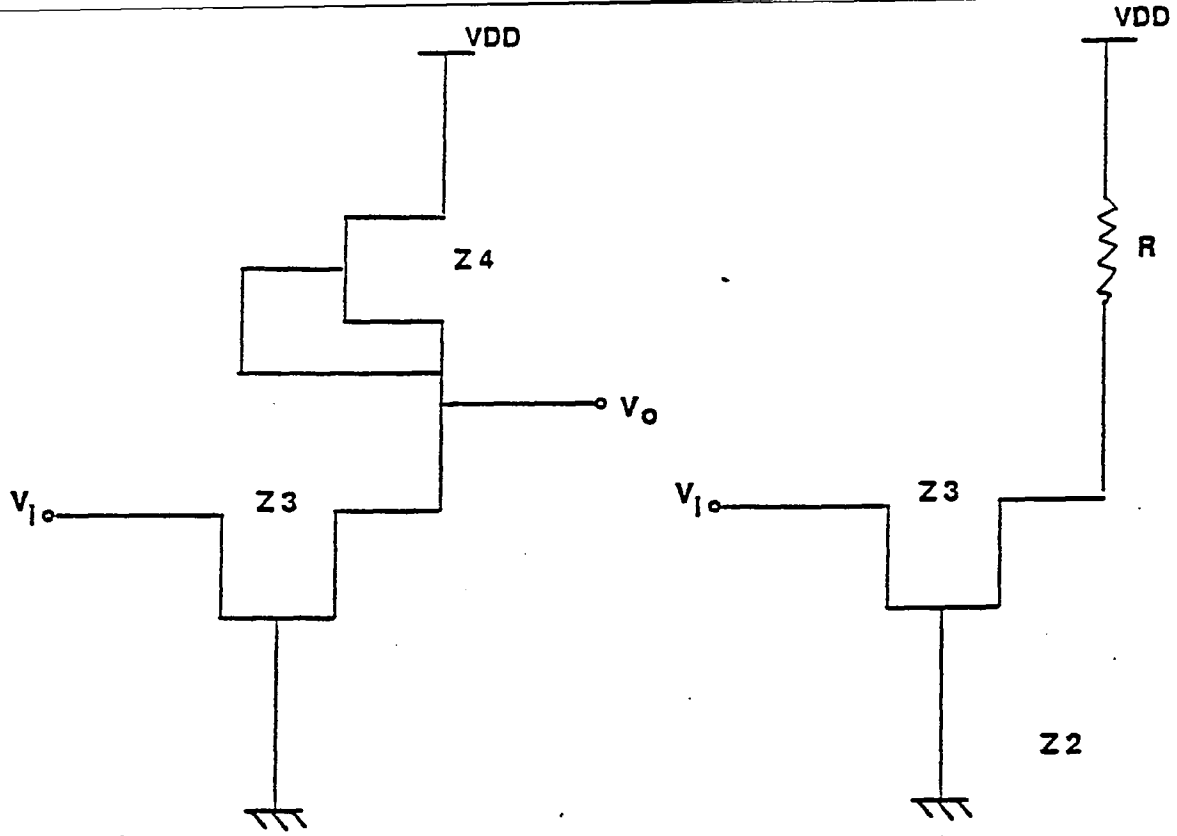
5.2.4 Common gate configuration (stage 2 of OEIC):

From fig.5.5, the nodal equation for the equivalent circuit is written as,

$$g_m V_{gs} = -j\omega V_{gs} + (1/r_d + 1/R + j\omega C_T)\, V_o \tag{5.13}$$

where $C_T = C_{ds} + C_{gd} + C_{sn}$. Now solving the above equation for $A_{v2} = V_o/V_i$, we get

$$A_{v2} = g_m + j\omega C_{ds}/ (1/r_d + 1/R + j\omega C_T) \tag{5.14}$$



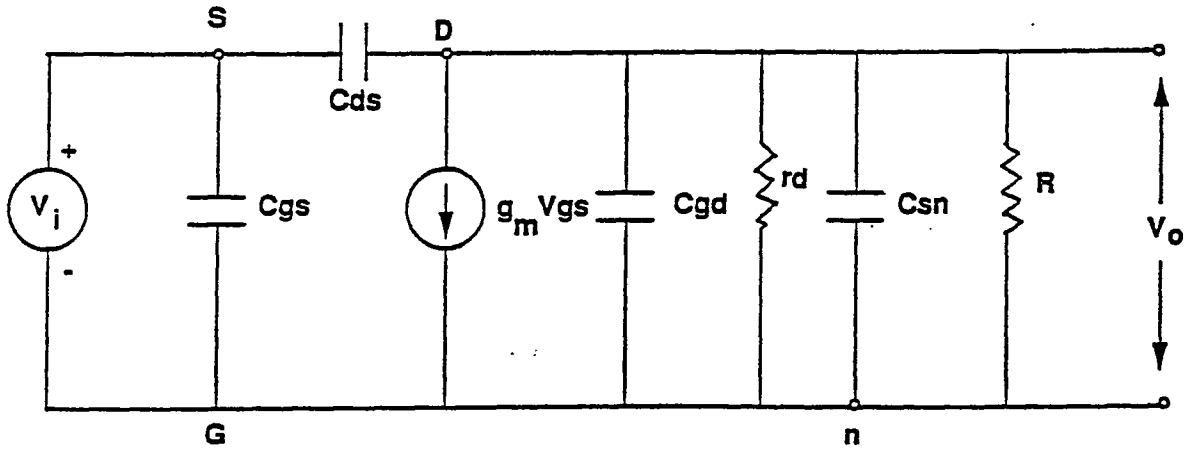


Figure 5.5: Stage 2 of OEIC & its small signal equivalent circuit

zero calculations: From eqn. 5.13 we get,

$$g_m + j\omega C_{ds} = 0 \tag{5.15}$$

$$S_{02} = j\omega = -g_m/C_{ds} \tag{5.16}$$

pole calculations: From eqn.5.13 we get,

$$1/r_d + 1/R + j\omega C_T = 0 \tag{5.17}$$

Hence pole of the stage 2 is given by,

$S_{p2} = j\omega = -(\ r_d + R)/\ r_d R(\ C_{ds} + C_{dg} + C_{sn}\ )$

input capacitance (C_i): $C_i = C_{gs} + C_{ds}(\ 1 - A_{v2}\ )$

output capacitance (C_o): It is obtained by looking into the drain of the MESFET when input voltage is zero. $C_o = C_{ds} + C_{gd} + C_T$

5.2.5 Common source configuration (stage 1 of OEIC):

From fig.5.6, a nodal eq. can be written as

$$-g_m V_{gs} = -j\omega C_{gd} V_{gs} + (\ 1/r_d + j\omega C_T + 1/R)\ V_o \tag{5.18}$$

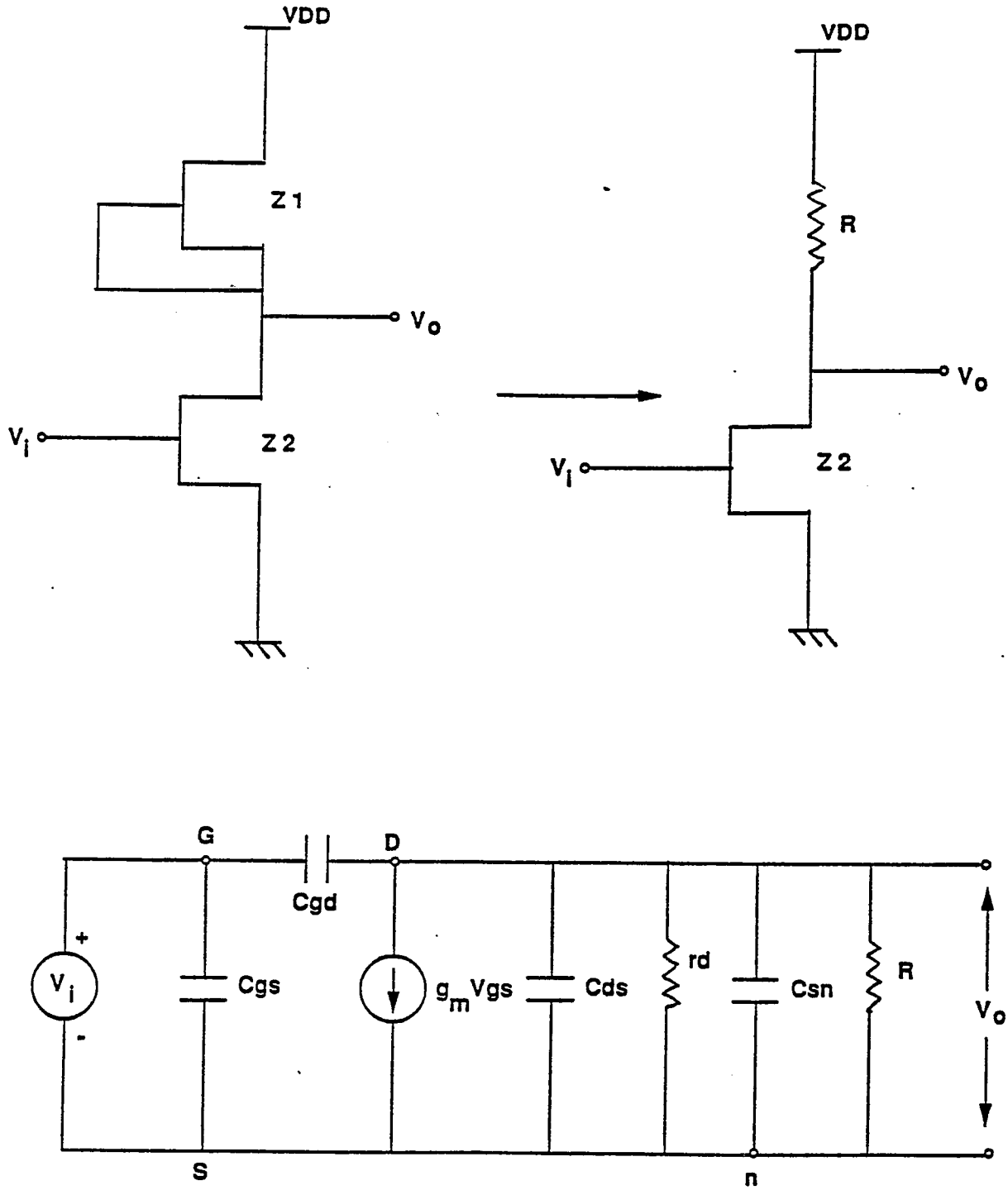


Figure 5.6: Stage 1 of OEIC & its small signal equivalent circuit

Now, solving the above equation for $A_{v1}=V_0/V_i$, we get

$$A_{v1} = -g_m + j\omega C_{gd}/\ [1/r_d + 1/R + j\omega C_T] \tag{5.19}$$

where $C_T = C_{ds} + C_{gd} + C_{sn}$

Input capacitance : $C_i = C_{gs} + (1-A_{v1})C_{gd}$

output capacitance : $C_o = C_{ds} + C_{gd} + C_{sn}$

zero calculation:

From eq.5.19

$$-g_m + j\omega C_{gd} = 0 \tag{5.20}$$

$$S_{(01)} = j\omega = g_m/C_{gd} \tag{5.21}$$

pole calculation: From eq.5.19

$$1/r_d + 1/R + j\omega C_T = 0 \tag{5.22}$$

$$S_{p1} = j\omega = -\ (\ R + r_d)/r_d Z_L[C_T] \tag{5.23}$$

Hence the overall gain of OEIC is given by the product of the gains of individual stages i.e. $A_v = A_{v1}.A_{v2}.A_{v3}.A_{v4}$

Gain-bandwidth product (GBW):

Gain-bandwidth product (GBW) is given by the following equation,

$$\text{GBW} = g_m/\ 2\pi(C_{in} + C_{out}) \tag{5.24}$$

where $C_{in} = C_{gs} + (1 - A_{v1})C_{gd}$ and $C_{out} = C_{gd} + (1 - A_{v4})C_{ds}$. Now, making required approximations and substituting the values we get the GBW as 71.65GHz. The amplifier gain is 31.5 (30.00 dbs, from SPICE output). We get the bandwidth of OEIC as 2.27GHz. This means that gain drops to its 3db value of about 22.38 at 22.38GHz which corrosponds to 27.00 dbs. The upper 3db frequency is calculated by using $f_H = 1/2\pi C_{in}$ and its value is 3.18 GHz. The cutoff frequency of OEIC being 12GHz, it stops amplifying after 12GHz. This is shown in fig.5.7.

Figure of merit (FM):

The figure of merit is used to compare the high frequency performance of the amplifier. The figure of merit of OEIC is calculated as given below.

$$\text{FM} = g_m/2\pi C_{in} \tag{5.25}$$

Substituting the values, we get FM of OEIC as 143.31GHz.

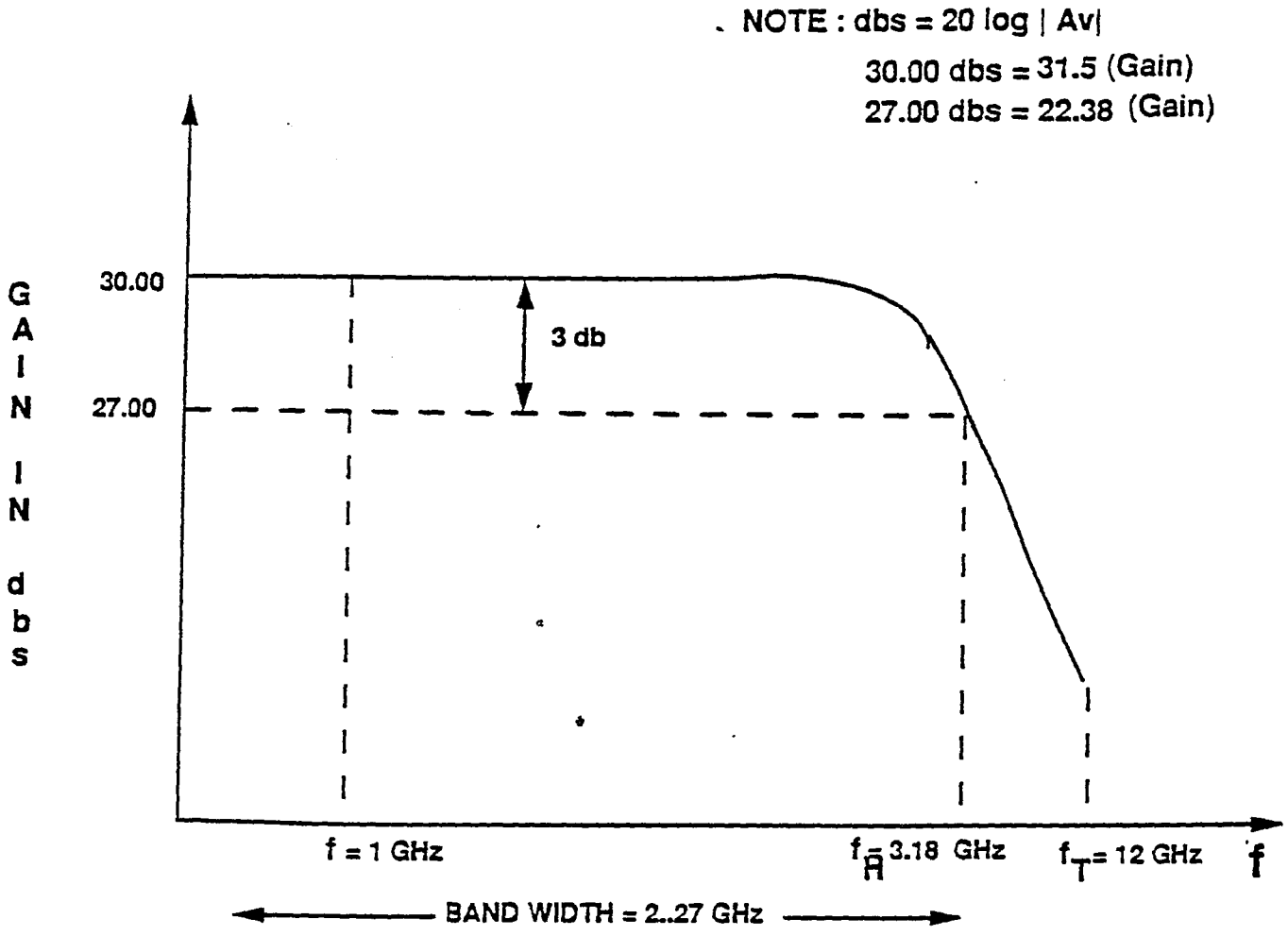


Figure 5.7: Frequency response of OEIC

Chapter 6

CONCLUSIONS

In chapter 3, the fabrication procedures for the respective devices involved in OEIC are discussed. From the fabrication procedure of p-i-n diode, it is seen that InGaAs is the optimum choice for the intrinsic material used for absorption. It absorbs light only in the range from 1.3μ to 1.55μ which is the region of minimum loss for fiber optic communication channel. From the fabrication procedure of GaAs MESFET involving the heteroepitaxial lift off, it is seen that the Van der Waal forces are good substitute for adhesives. A close contact can be obtained between the film and the substrate for good thermal conduction. These forces also reduce the interface thickness to allow the minimum ohmic resistance.

In chapter 4, the SPICE simulation of OEIC has been discussed and the results are shown in figures 4.2 and 4.3. Since the device is operated at the Q-point to get the optimum output signal, this Q-point is obtained from I-V characteristics.

From figure 3.6, it is seen that it is good to operate MESFET Z-7 at -0.52v to get sufficiently large saturation current. Figure 4.3 gives the variation in the output signal with respect to the position of the body capacitance. Since there is not any significant change in the output of OEIC, a conclusion is made on the output of OEIC as being independent of the position of the body capacitance and depends only on the values of gate to source (C_{gs}) and gate to drain (C_{gd}) capacitance. These capacitances can be reduced by metallization.

From the values of body capacitances, which are very much less than (about 10 times) $C_{gs}\&C_{gd}$, it is seen that, in small signal high frequency analysis, these capacitances become the dominant poles. The body capacitances do not influence the frequency response.

In chapter 5, the small signal high frequency analysis and the frequency response of OEIC are discussed. The following conclusions are made from figure 5.7;

[1] The bandwidth of OEIC is 2.27GHz. This is calculated from the gain-bandwidth product of 71.65GHz and the amplifier gain, which is 31.5 (30.0 dbs from SPICE output).

[2] The gain of the OEIC drops to 27.0dbs (from 30.0dbs), which corresponds to the gain of 22.38. This shows that, at the upper 3db frequency of 3.18GHz, a gain of 22.38 can be achieved.

[3] The operating frequency of OEIC is 1GHz and the cut off frequency is 12GHz.

[4] The poles of the OEIC will lie in the frequency range of 3.18GHz to 12GHz, corresponding to each stage of the amplifier.

Within experimental errors, these SPICE simulation and frequency response results are expected to be compatible with the actual chip after fabrication.

Chapter 7

APPENDIX

7.1 Definitions:

Activation energy : Energy required for the reaction.

Conduction band : Energy band of conduction electrons.

Covalent bond : Interatomic bond created when two adjacent atoms share a pair of electrons.

Dielectric : An insulator. A material that can be placed between two electrodes without conduction.

Electron charge : The charge of 0.16 $\times 10^{-18}$ coul. carried by each electron.

Electron-hole pair : A conduction electron in the conduction band and an accompanying hole in the valence band, which result when an electron jumps the gap in an intrinsic semiconductor.

Energy gap : Unoccupied energy levels between the valance band and conduction band.

Insulator : Non conductor of electrical or thermal energy. The material with filled valance band and a large energy gap.

Ionic bond : Atomic bonding by coulombic attraction of unlike ions.

Lattice constant : Dimensions of the unit cell.

Mobility (μ) : The drift velocity of an electric charge per unit electric field.

N-type semiconductor : Semiconductor having negative charge carriers, electrons.

P-type semiconductor : Semiconductor having positive charge carriers, holes.

Photoconduction : Conduction arising from activation of electrons across the energy gap by means of light.

Photon : A quantum of light.

Semiconductor : A material with controllable conductivities. Intermediate between conductor and insulator.

Valance band : Filled energy band below the energy gap. Conduction in this band requires holes.

Van der Waal forces : Secondary bands arising from structural polarization.

7.2 Gallium, Arsenic & GaAs

1. Ga is a rare element and is produced as a by product in Al or Zn production. The physical properties of this metal are described in the table. Standard purification process make it possible to obtain 99.99% pure Ga. Liquid Ga reacts with quartz at high temperature leading to impurities in GaAs growth in quartz container. Ga is considered to be toxic.

2. Arsenic is mainly produced from Sulfur ores (Native mineral which yields metal), such as As_2S_4 or As_2S_3. Oxidation is used to obtain As_2O_3 which is then reduced to get As. This reduction process is done in the presence of Carbon. Arsenic is more diffcult to purify than Ga. The most pure As can be obtained by thermal decomposition of Arsine. Arsenic is very much toxic. The physical properties of this metal are described in the table.

3. To form GaAs following processes are used:

A. Liquid Epitaxy.

B. Vapor Epitaxy.

C. Molecular Beam Epitaxy.

D. Metal Organic Chemical Vapor Deposition.

4.**Constants:**

1. Planck's constant = h = 0.662 $\times 10^{-33}$ J-s.
2. Velocity of light in vacuum = c = 3 $\times 10^{8}$ m/s.
3. 1μm = 10^{-6} m.
4. 1eV = 0.160 $\times 10^{-18}$ J.
5. 1$\mathring{A}$ = 10^{-8} cm = 0.1nm.
6. Giga = G = 10^{9}

7.3 Indium Gallium Arsenide InGaAs:

Parameters	Symbol	Value
Energy gap at 300K	E_g	0.732eV
Electron mobility	μ_n	1.1 $\times 10^4 cm^2/Vsec$
Minority carrier lifetime	τ_d	182psec
Effective lifetime	τ_{eff}	81μsec
Carrier density of an epitaxial layer	N_D	4.3 $\times 10^{15}$
lattice parameter	a	

Table of InGaAs properties.

Chapter 8

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