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Graded buried channel charge coupled device design

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ABSTRACT

Title of Thesis: GRADED CHANNEL CHARGE COUPLE DEVICE DESIGN

Author: ZENGJING WU, Master of Science in Electrical Engineering, 1991

Thesis directed by: DR. WALTER F. KOSONOCKY

A process and device simulation study has been made to optimize a new type of buried channel CCD (BCCD) structure to be referred to as Graded BCCD (GBCCD) whose buried channel is formed by multiple implantations for achieving higher charge transfer efficiency. The 2-D process simulation tool SUPREM4 and 2-D device simulation tool PISCES2 were used in this research. The simulation results of the GBCCD with double channel implants are compared with the previously obtained experimental results.

Triple channel implants under the conditions of various process parameters were also simulated and the optimized case was chosen on the base of results. The device characteristics of the GBCCDs such as charge distribution, potential profile, pinning voltage and electric field have been fully investigated and studied.

Also in order to enhance the performance of PISCES2 a Fortran program that can calculate the number of electrons in the GBCCD channel and estimate their distribution area was successfully developed.

GRADED BURIED CHANNEL CHARGE COUPLED DEVICE DESIGN

by

Zengjing Wu

Thesis submitted to the Faculty of the Graduate School of
the New Jersey Institute of Technology in partial fulfillment of
the requirements for the degree of
Master of Science in Electrical Engineering
1991

Approval Sheet

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Dedicated to
My Parents

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Many people have assisted me during my thesis work. I am very grateful to my graduate advisor Professor Walter F. Kosonocky, holder of the NJIT Foundation Chair for Optoelectronics and Solid-State Circuits. whose inspiration and guidance benefited me significantly; without his support this work could not have been finished. I would like to thank Dr. D. Misra for his suggestions and Dr. K. Sohn for being in my committee.

I would also like to express my appreciation to my friends at NJIT, who gave me their assistance in many ways. I feel particularly grateful to Elie I. Mourad and A. V. Subramanyam for their assistances specifically with the reference to understanding the concept of quasi fermi potentials for carrying out Poisson solution in using PISCES 2B.

Contents

List of Figures

Chapter 1

Introduction

The research described in this thesis was performed at the NJIT Image Sensor Laboratory under the direction of Professor Walter F. Kosonocky, holder of the NJIT Foundation Chair for Optoelectronics and Solid-State Circuits.

Process and device Simulation is considered very essential in industrial applications. Progressive industries are using SUPREM3, SUPREM4, PISCES etc.. in their task of finding an optimized process and developing new devices. Figure 1.1 shows the relationship between fabrication and the simulation process.

In this thesis both SUPREM4 and PISCES were used to find the optimized process for the new device which is called Graded BCCD where buried channel is formed by multiple implants.

The concept of Graded Buried Channel Device was proposed by Prof. Kosonocky to improve charge transfer efficiency in buried-channel CCD operating at a temperature of 77K and below[1][2]. The experimental results[3][4] showed that an additional trench implant in the buried-channel, i.e. double channel implants, improves the charge transfer efficiency especially for small signals.

So in this thesis both process and device simulations were done for the Graded BCCD with double channel implants in order to verify the experimental re-

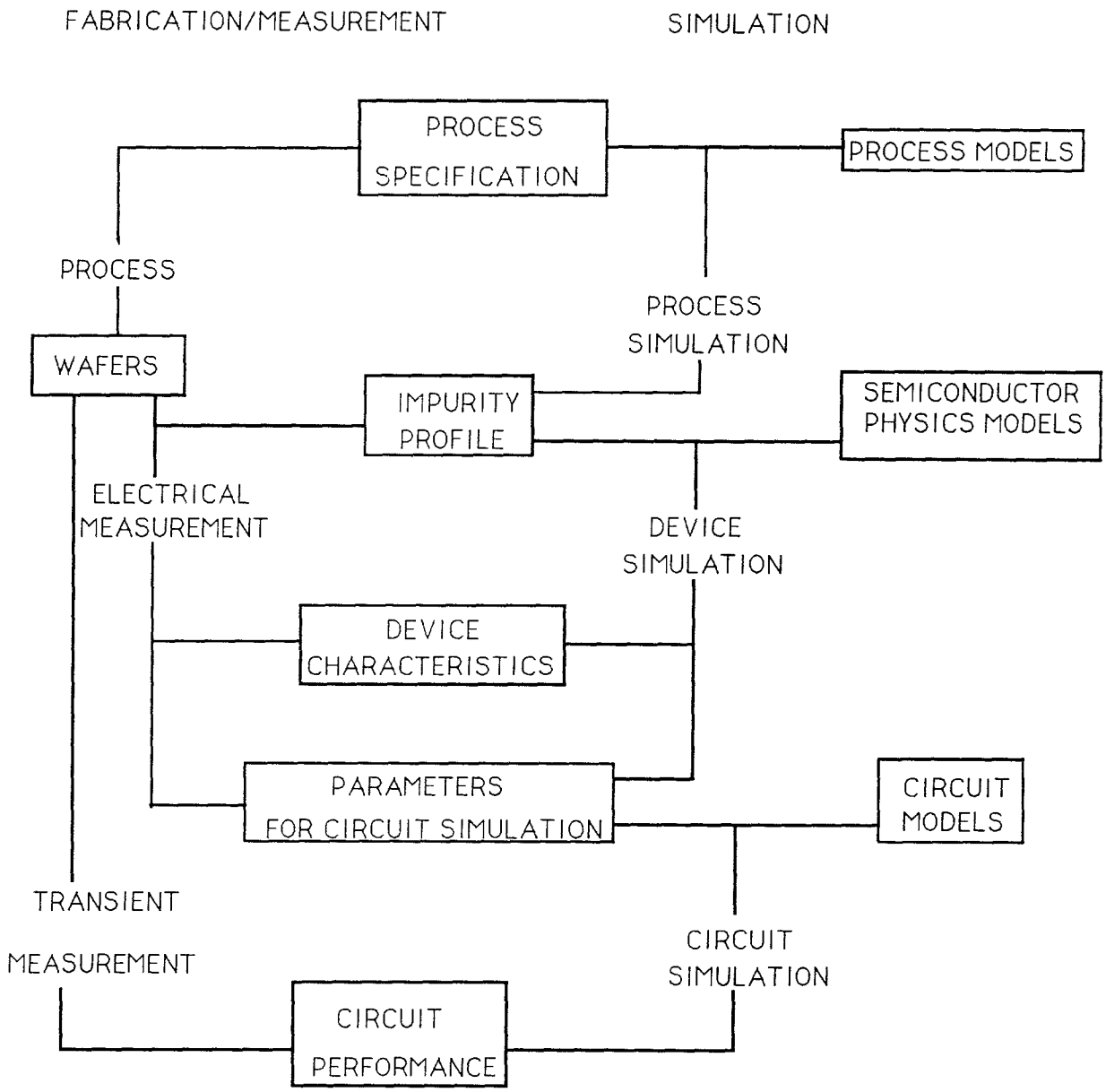

Figure 1.1: Block diagram of the process development

sults.

Then, the Graded BCCD with triple channel implants was investigated and the simulation results were compared to the double implants and the single implant cases.

The main goal of this research has been to investigate the performance of graded buried-channel charge coupled devices under different process conditions and to suggest methods to improve the charge transfer efficiency of these devices.

Chapter 2 describes basic principles of charge storage and charge transfer in BCCD and the advantages of the GBCCD structure which can reduce the bulk trapping and improve the charge transfer efficiency.

Chapter 3 reviews the experimental results of transfer inefficiency for GBCCD with double channel implants.

In Chapter 4, SUPREM4 process simulations were described for the BCCD with single, double and triple channel implants under different process conditions which were based on the process data provided by David Sarnoff Research Center.

In Chapter 5, a parameter extract program was developed to enhance the performance of PISCES2. PISCES2 device simulations were done for each different structures of GBCCD. The results of SUPREM4 were used as the input doping profiles for PISCES2. The device characteristics of each case were investigated. These simulation results were compared to determine the optimum channel doping schedule.

Finally, the summary and conclusion are reported in Chapter 6.

Chapter 2

The Graded BCCD, a New CCD Concept

2.1 Introduction of BCCD

The introduction of CCD's in 1970 generated an enormous world-wide interest and activity in virtually every major semiconductor laboratory and a very large output of papers, reports, and books. And the first product, a CCD imager, was demonstrated only three years after the charge-coupled concept was introduced[5]. Basically CCD is a shift register formed by a string of closely spaced MOS capacitors. A CCD can store and transfer analog-charge signals, either electrons or holes , that may be introduced electrically or optically. Unlike all other integrated circuits, which are merely the fabrication on one silicon chip of circuits that could as easily be made in discrete form, the CCD has no discrete equivalent circuit, *i.e.*, it cannot be made up of discrete devices. It is, in fact, the first truly integrated silicon circuit[9]!

There are two basic types of charge-coupled structures: surface and buried CCDs as shown in Fig. 2.1. SCCD has its charge packets stored very close to the interface between the semiconductor and the overlying insulator. BCCD has its charge packets stored some distance away from the interface between

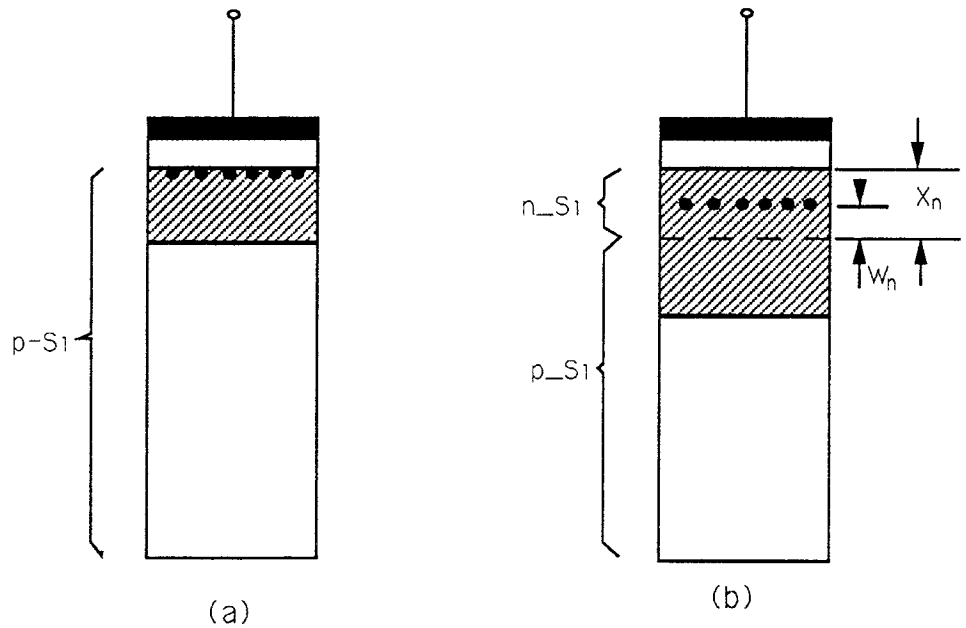

Figure 2.1: Cross sections through (a) an SCCD and (b) a BCCD showing the charge location.

the semiconductor and the insulator.

The transfer of charge in SCCDs is limited by *fast surface states*, these are states found near the semiconductor/insulator interface which rapidly acquire charge as a potential well fills, but which are reluctant to release their charge when the well subsequently empties, resulting in a net loss of signal.

The buried channel is created by an additional implant of opposite type dopant to that of the bulk. This is illustrated in Fig. 2.2 [6]. Also in Fig. 2.2 the energy band diagrams for empty and partially filled configurations are plotted. We see that the bulk channel CCD eliminates the deleterious effect of surface states by causing the potential wells to form, not at the semiconductor-insulator interface. but some distance into the bulk semiconductor. The surface states and trapping effects associated with the interface are avoided, thereby improving the charge transfer efficiency.

2.2 Operation of BCCD

The signal charge in Buried Channel CCD is stored in the bulk of the semiconductor where there is a energy minimum(n-channel BCCD). In a BCCD, the charges present initially are clocked out. Thus the BCCD array gets completely depleted or in other words the p-n junction get reverse biased. Hence while using BCCDs first few clock cycles essentially empty the wells. As shown in Fig. 2.2 the energy minimum lies in the n-region which is away from the Si-SiO_2 interface. Thus, in a manner analogous to the surface channel CCD, BCCD is capable of storing charge in the semiconductor. However the charge storage mechanism in BCCD is very different from that in a surface channel device. In the BCCD, however, the information- carrying electrons are majority carriers which replace some of the electrons that were previously removed.

2.3 Charge Trapping and the Proposal of GBCCD

It is well known that in surface-channel devices, trapping and subsequent loss of carriers from the charge packets occurs due to fast interface states[6]. Fabrication processes cause unavoidable interface traps and oxide charges to exist at this interface which effect device performance[11]. These traps are interface-trapped charge Q_{it}, fixed-oxide charge Q_f, oxide -trapped charge Q_{ot} and mobile ionic charge Q_m[10]. Of these four, the interface -trapped charge effects SCCD performance the most. These interface trapped charges have energy levels distributed throughout the bandgap of Si and are known as fast interface states in CCD terminology because they can be occupied by electrons in approximately 10^{-11} seconds. However, they empty at various rates ranging from 10^{-4} to 10^{-11} seconds depending upon the energy (in electron volts)

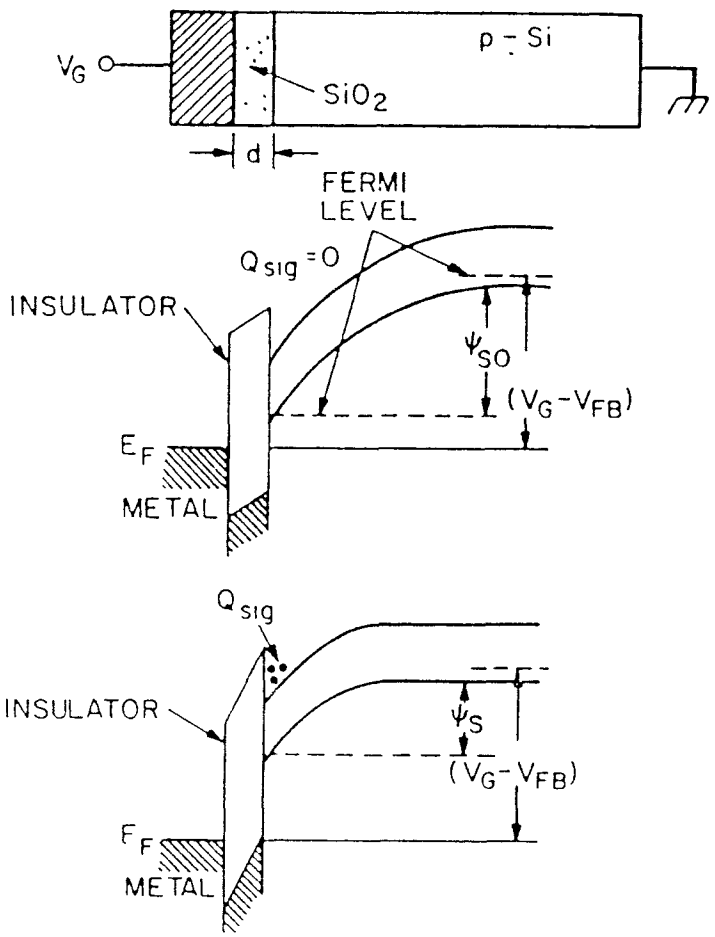

Figure 2.2: Illustration of buried channel CCD:device construction, potential well diagram for no signal present, and potential well diagram for signal present

between the trap site and conduction band of silicon. Thus many states can fill faster than they can empty, resulting in a net loss of signal into trap states. This loss mechanism can be minimized by continuously circulating a small amount of charge[7]. This background charge is generally called 'fat zero', and tends to keep the fast states continuously filled so that no states are empty to trap charge when a full well signal arrives. The number of trapping sites is proportional to crystal orientation and is approximately 10^{10} cm^{-2} for $< 100 >$ Si and 10^{11} cm^{-2} for $< 111 >$ Si. For this reason most devices fabricated today use $< 100 >$ Si to decrease the density of the fast interface states.

The problem of surface state trapping does not , of course, occur with buried channel CCD (because the signal charge is held away from the Si/SiO_2 interface) and this is one of their major advantages over surface channel devices. Unfortunately there are still some transfer losses in BCCDs associated with charge trapping effects[7]. These losses are attributed to traps in the bulk of the buried channel that have discrete energy levels located in the forbidden bandgap of Si [8]. This situation is quite different from the SCCD case where the trap sites are distributed throughout the bandgap. Four different generation and recombination processes utilize the bulk trap levels within the bandgap as transition states for bulk trapping. They are illustrated in Fig. 2.3. Figures 2.3(a) to 2.3(d) represent, respectively, electron capture from the conduction band, emission of electrons to the conduction band, hole capture from the valance band, and emission of holes to the valance band. The rate of change in trap occupancy is described by the Shockley-Read -Hall theory

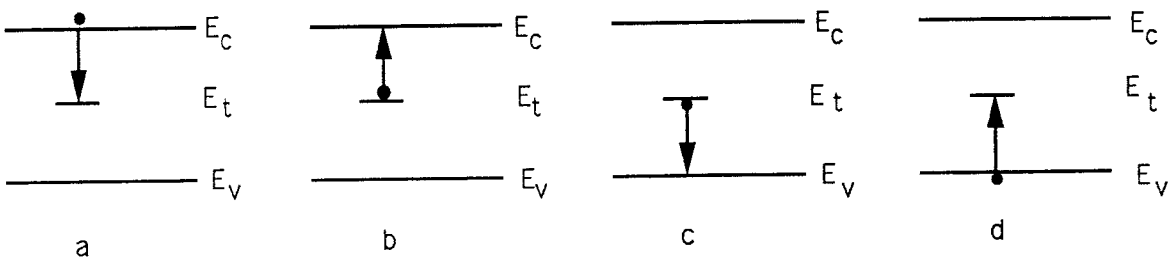

Figure 2.3: Utilization of traps sites for generation and recombination processes–(a) electron capture, (b) emission of electrons, (c) hole capture, and (d) emission of holes.

to be [8].

$$\frac{dn_t}{d_t} = \frac{N_t - n_t}{T_{ne}} - \frac{n_t}{T_{nc}} - \frac{n_t - n_t}{T_{pc}} - \frac{N_t - n_t}{T_{pe}} \tag{2.1}$$

where

n_t = density of captured electrons

N_t = total trap density

T_{ne} = electron emission time constant

T_{nc} = electron capture time constant

T_{pe} = hole emission time constant

T_{nc} = hole capture time constant.

The four items in Eq. 2.1 represent the processes described in Fig. 2.3 (a) through (d), respectively. Since the buried channel is n-type and electrons are the carriers stored in the channel region, the capture and emission of holes

can be neglected. Eq. 2.1 can be simplified as

$$\frac{dn_t}{d_t} = \frac{N_t - n_t}{T_{ne}} - \frac{n_t}{T_{nc}} \tag{2.2}$$

where the electron emission and capture time constants are given by

$$T_{ne} = (\delta_n V_{th} N_c \epsilon xp(-\frac{E_c - E_t}{kT}))^{-1} \tag{2.3}$$

$$T_{nc} = (\delta_n V_{th} n)^{-1} \tag{2.4}$$

where

δ_n = capture cross section for electrons

V_{th} = average thermal velocity of electrons

N_c = effective density of states in the conduction band

E_c = bottom of conduction band

E_t = trap energy level

k = Boltzmann's constant

T = absolute temperature

n = free electron concentration

If charge is present in a potential well there exists a large concentration of free electrons, n, equal to approximately 1/3 the dopant level at full well capacity[3]. This large concentration causes $T_{nc} \ll T_{ne}$ and therefore the trap sites can be assumed to be filled almost immediately as the charge packet arrives in the potential well due to Eq.2.4. Once the charge signal is transferred to an adjacent potential well, n becomes very small. As a result $T_{ne} \ll T_{nc}$ and electrons will be emitted at a rate dictated by Eq.2.3.

It was shown by Mohsen and Tompsett that the charge trapped in bulk traps from a signal charge is proportional to the spatial volume of bulk silicon (in

which the bulk states can be filled by charge signal). Eq.2.5 gives the relationship between the charge trapped in bulk traps and the spatial volume of bulk silicon[7].

$$\Delta Q_s \approx eN_t V_0 exp(-T_0/\tau_e) \tag{2.5}$$

where V_0 is the volume occupied by the signal charge under the storage gate. Moreover, for small signal packets the volume of bulk silicon per electron is greatest, (i.e. greatest proportional loss due to traps.)

From Eq.2.3 it is clear that as temperature decreases, the emission time constant increases. In addition, at a temperature below 100K the charge signal begins to be subjected to carrier freeze-out [10]. Carrier freeze-out refers to the condition in which the donor level in the BCCD channel start acting as traps for charge signal [18]. As temperature is decreased further, the density of traps increases due to increased carrier freeze-out. As a result, the probability of trapping the charge at these donor traps increases with decreasing temperature.

In order to decrease the effects of bulk traps and increase the transfer efficiency especially operating at 77K and below, a Graded doping profile BCCD was proposed by Dr. Kosonocky[1]. The experimental results[3] showed that this kind of GBCCD is very effective when handling the small charge packet.

In this research both process and device simulations are done for the Graded BCCD with double channel implants in order to verify the experimental results.

Then the Graded BCCD with triple channel implants is proposed and the simulation results are compared with the double implants case as well as the single implant case.

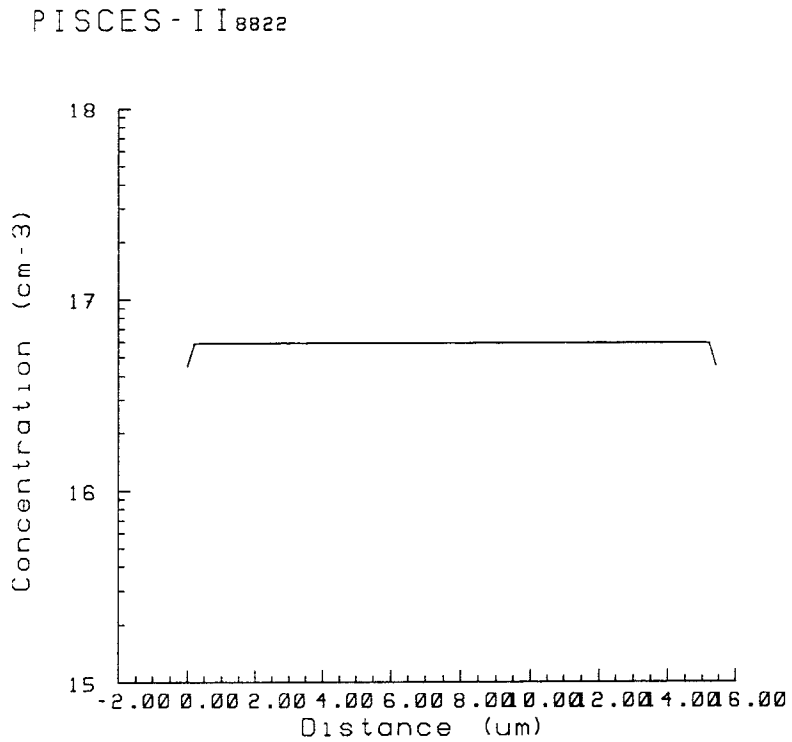

Figure 2.4: The doping profile across the buried channel of normal BCCD

The performances of various GBCCDs with triple implants fabricated under different process procedures are investigated in order to find out the optimized case.

Before discussing the various simulation results in detail we'd like to choose two typical simulation results as an example to show the differences between the normal BCCD and the Graded BCCD

For normal BCCD the doping profile along the buried channel is uniform as shown in Fig. 2.4.

When a small amount of signal electrons is introduced, the potential profile is shown in Fig 2.5. A two dimensional charge distribution for this case is shown in Fig. 2.6. The contour lines in this figure represent the distribution boundaries of the concentration of charge carriers in electrons per cm^3.

In inspection of this figure shows that most electrons are spread over the

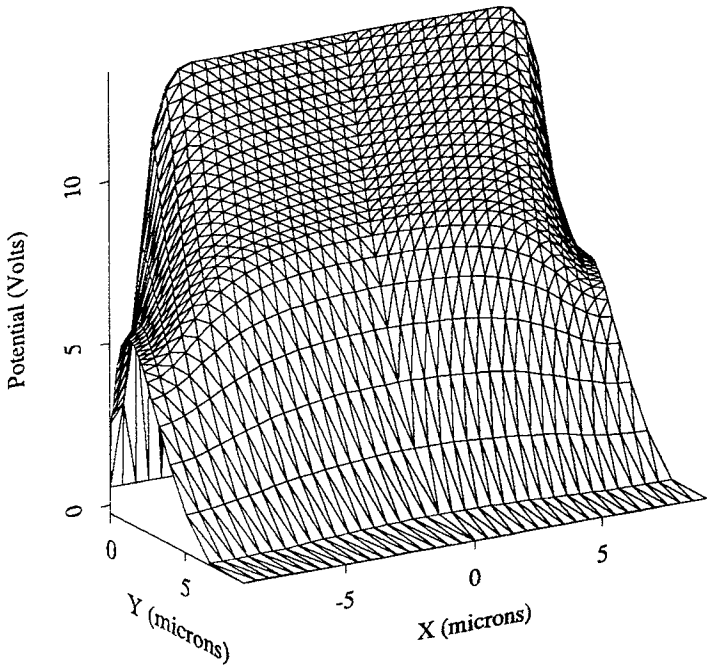

Figure 2.5: The potential profile of normal BCCD without signal charges

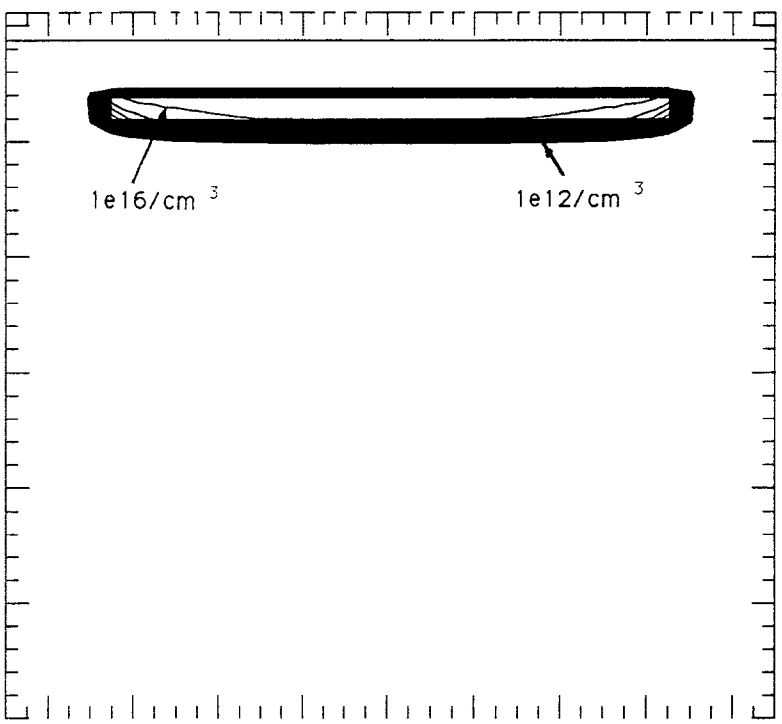

Figure 2.6: Two dimensional distribution of electrons for a small packet of signal charge in normal BCCD

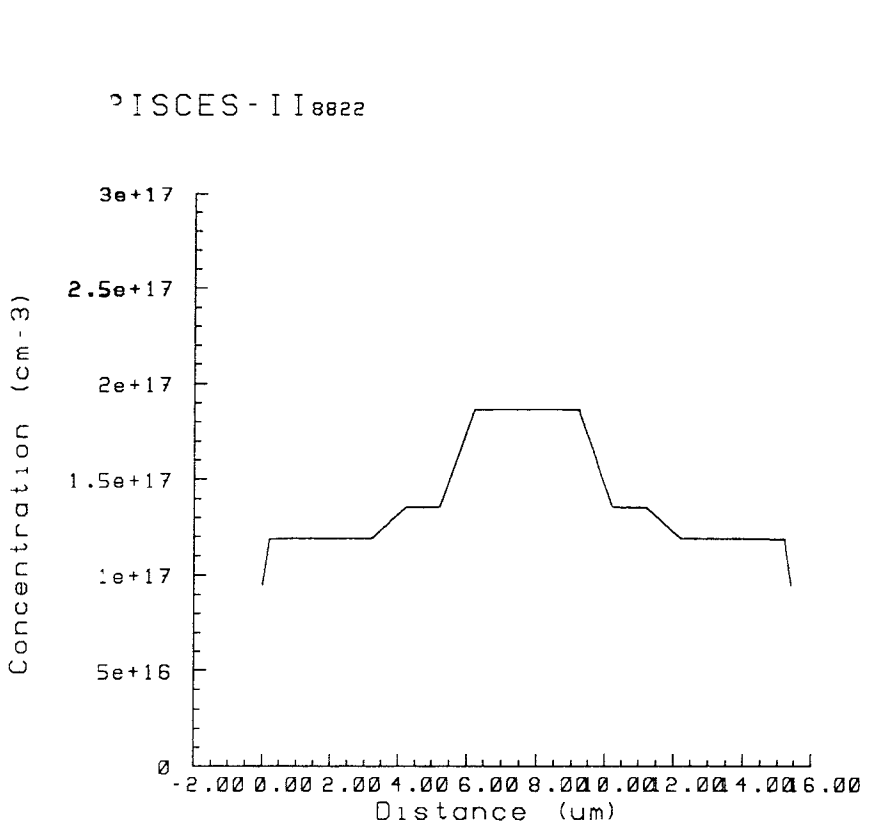

Figure 2.7: The doping profile across the buried channel of Graded BCCD

whole channel width. This results in large charge transfer loss because of bulk trapping.

For graded BCCD the doping profile along the buried channel is made to be not uniform as shown in Fig. 2.7. The doping concentration is selected to be highest around the central area in the channel. This kind of graded doping profile has been achieved by superposition of three BCCD channel implants covering different channel width.

When a small packet of signal electrons is injected into the Graded BCCD, the potential profile takes the shape as shown in Fig. 2.8 and the signal electrons will distribute as shown in Fig. 2.9. In this case the volume of bulk silicon per electron is much smaller than the previous case. Therefore, the signal loss caused by bulk trapping will also be smaller and the transfer efficiency can be improved.

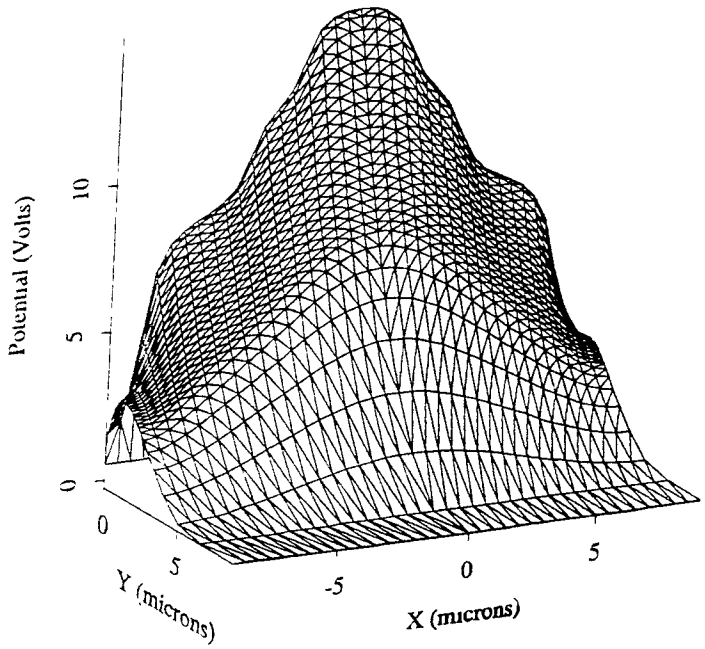

Figure 2.8: The potential profile of GBCCD without signal charges

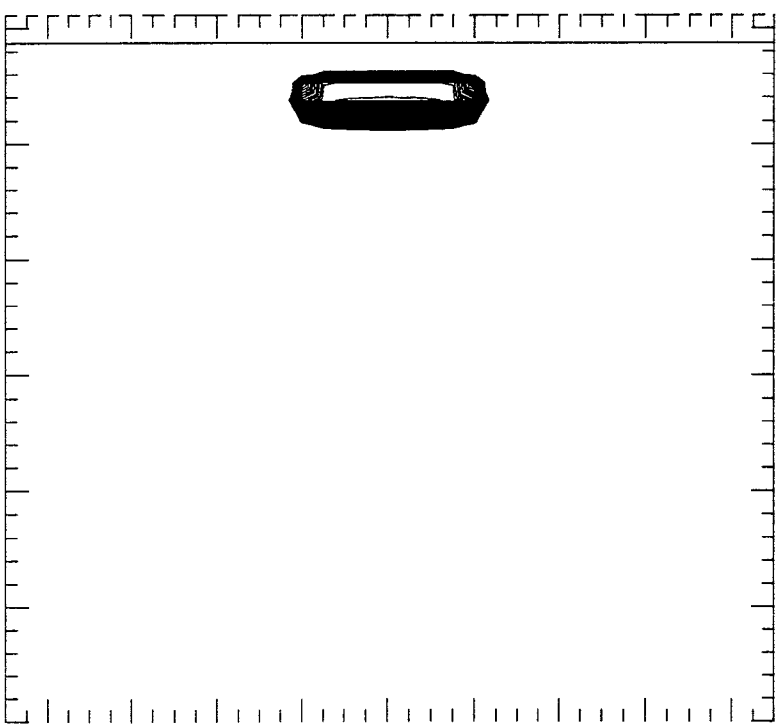

Figure 2.9: Two dimensional distribution of electrons for a small packet of signal charge in GBCCD

The following chapters will explore the GBCCD from processing procedures to device characteristics in great detail.

Chapter 3

Review of Experimental results

3.1 Introduction

This chapter will review the experimental results done by Benjamin J. Esposito[3]. The goal of his research was to investigate the charge transfer inefficiencies of buried- channel charge coupled devices for operation in the temperature range of 77K-45K and to suggest models for the charge trapping losses. The buried-channel charge coupled device studied by Esposito has been used as the readout multiplexer for infrared image sensors with PtSi Schottky- barrier detectors (SBDs).

3.2 Methods of testing charge transfer inefficiency

A IR-CCD image sensors of an interline transfer 160x244-element studied by Esposito is shown in Fig. 3.1. A simplified description of the operation of these devices is as follows. Optical signal detected by the SBDs is transferred into the buried channel B-register (vertical register). The B register then transfers the information one line at a time into the buried channel C-register (horizontal register). The data is then clocked out at video rates to an on chip

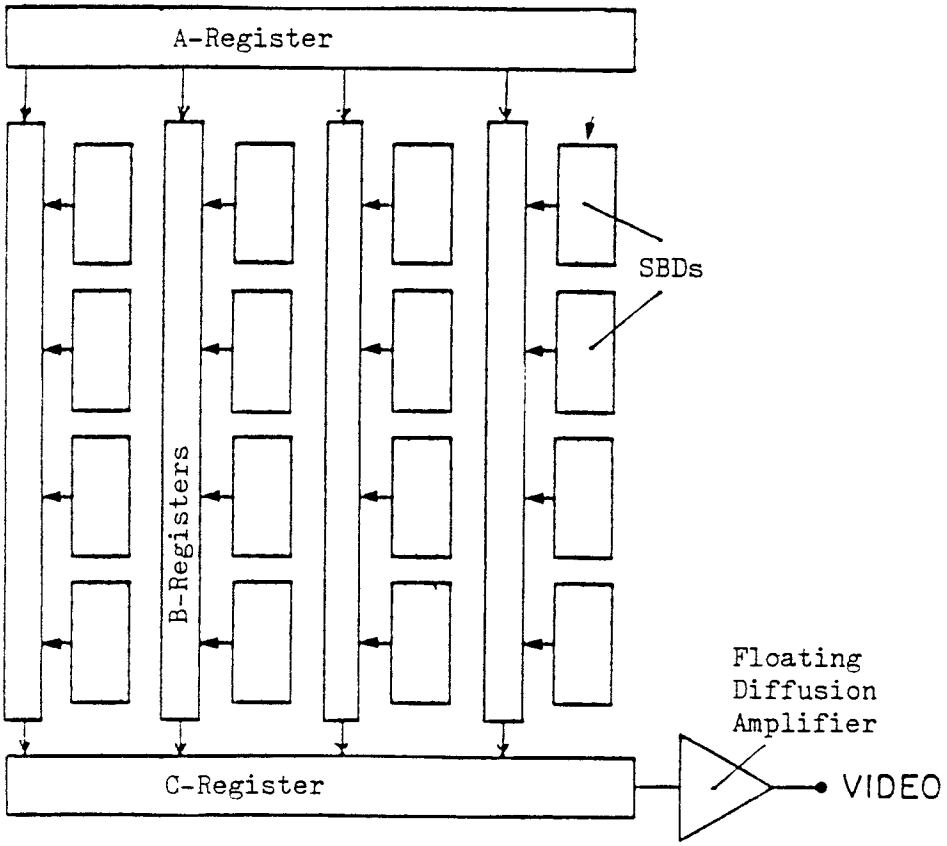

Figure 3.1: Block diagram of chip layout

floating diffusion amplifier. The A-register shown in the diagram is used to introduce signal into the vertical B-register for testing purposes only and is biased off during imaging. There are two methods of testing the charge transfer inefficiency (or charge transfer loss) of the buried channel C-register – one using an electrical input and the other one using an optical input. The optical method relies on transferring information from the detectors to the horizontal register (C-register) where the charge transfer inefficiency is measured. The electric input method requires some form of electric charge signal injected directly into the horizontal register where the charge transfer inefficiency is measured. These two methods are described in greater detail in Chapter V-B of Esposito's thesis [3].

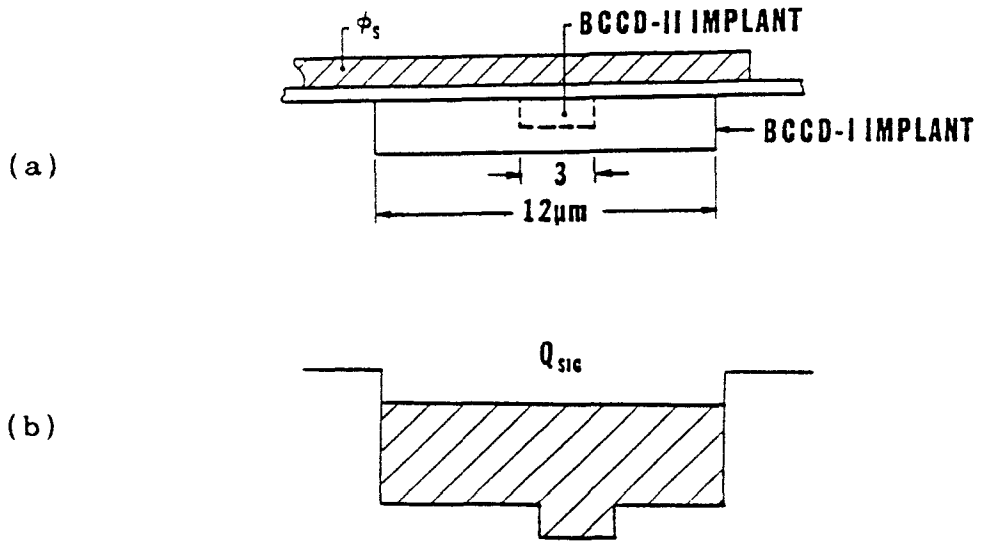

Figure 3.2: Improved BCCD channel structure with trench implant: (a) cross sectional view (b) Corresponding potential well profile.

3.3 Experimental results

3.3.1 Device Structure

The device structure of the 160x244-element IR-CCD imager shown in Fig. 3.2(a) illustrates a cross sectional view of a 12-μm-wide channel with an additional 3μm implant. The corresponding potential well diagram is shown in Fig. 3.2(b). Arsenic was used as the BCCD-2 implant dopant to keep carrier diffusion to a minimum during anneal cycles[2][4]. Note that the implant creates a trench in the potential well profile along the direction of charge flow. For small signals the charge is confined to the small trench while larger signals can occupy both the trench and the larger well.

3.3.2 Measurements of charge transfer inefficiency as a function of applied gate voltage

The transfer inefficiencies of buried-channel charge coupled devices under different test conditions have been measured [3]. Here we consider two typical experimental results of Esposito (Figures 3.3 and 3.4) which will be compared with the simulation results in Chapter 5.

The curves in Fig. 3.3 illustrate the total transfer loss versus signal level for three different clock voltages at zero background signal [3]. Note that, as the gate voltage is increased, the measured total transfer loss decreases. Also note that all three curves have the same profile shape.

The transfer inefficiency curves representing the total charge transfer loss divided by the number of transfer charges shown in Fig. 3.4 correspond to the data in Fig. 3.3.

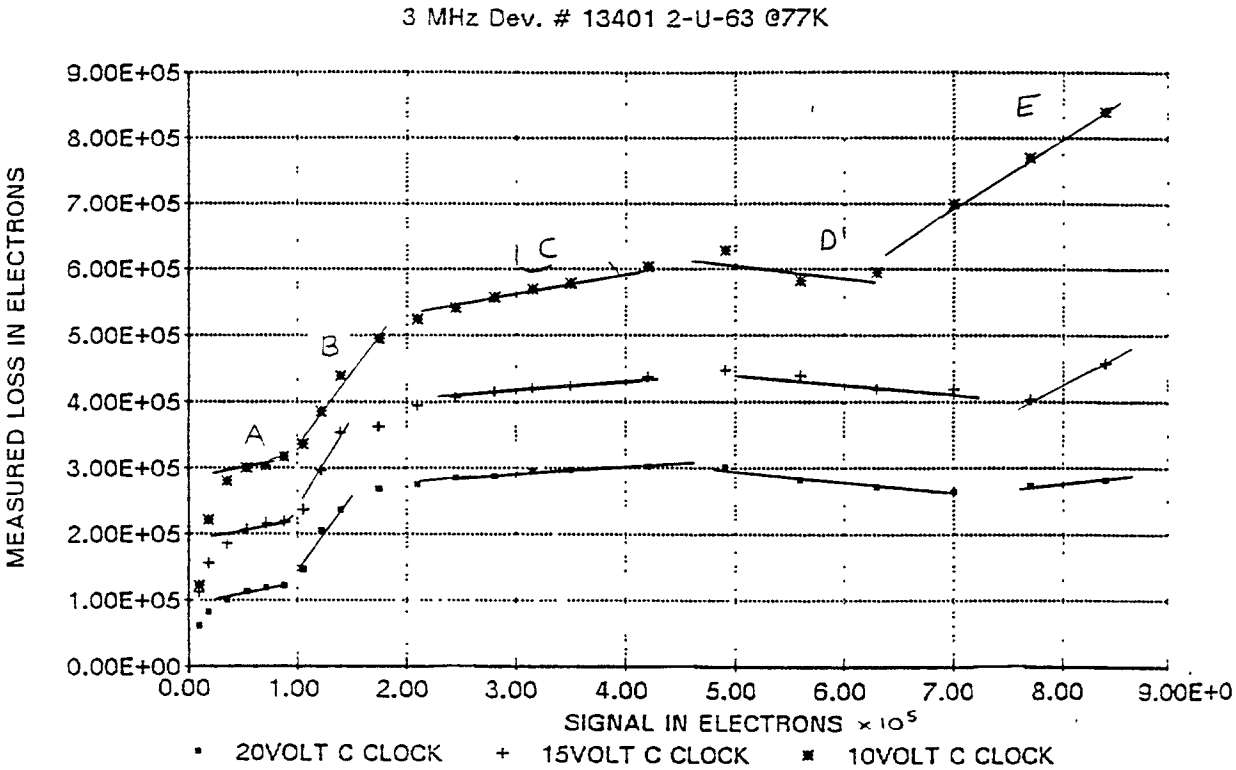

Figure 3.3: Charge transfer inefficiency as a function of applied gate voltage and signal level at zero background charge for a 160x244-element array with 20-μm gates.

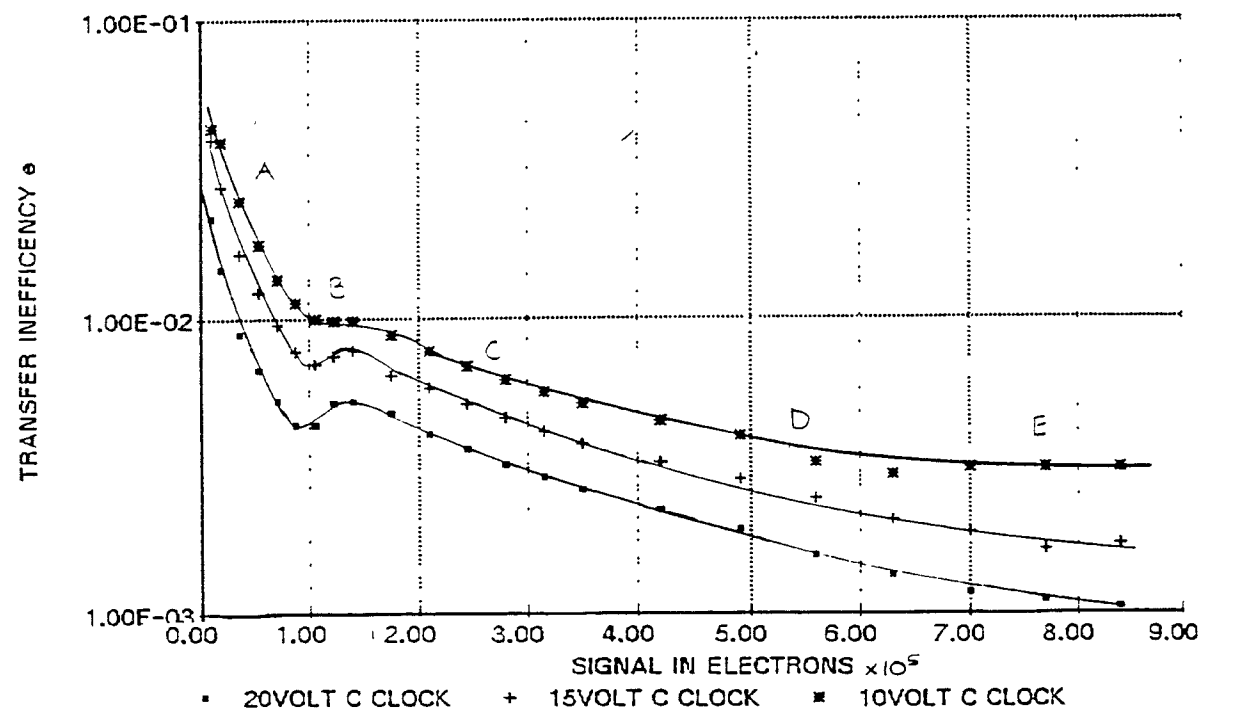

Figure 3.4: Charge transfer inefficiency as a function of applied gate voltage for the given in fig.3.3

Chapter 4

Results of 2-D Processing Simulation

The complete processing simulation programs are shown in Appendix A. Here we only discuss some main processing steps and results.

The first lines in the input deck set some basic SUPREM4 options.

#graded bccd process simulation

set echo

option quiet

The '#' character is the comment character for SUPREM4. The entire line after the '#' is ignored. The echo flag is turned on. This instructs SUPREM4 to echo input lines after they are typed. This is useful when the output from the simulator is being redirected into a file, so the commands are in the output listing. The second command instructs the simulator to be quiet about what it is doing. The default option is verbose, but this prints far more information than is needed by the novice user.

The next section begins the definition of the mesh to be used for the simulation.

line x loc=0.0 tag=left spacing=0.5

line x loc=9.0 tag=right spacing=0.5

This section describes the locations of the x lines in the mesh. SUPREM4 defines x to be the direction across the top of the wafer, and y to be the vertical dimension into the wafer. The first command line instructs SUPREM4 to locate a mesh line at x equals 0.0 μm. This line is 'tagged' to be the name of 'left'. The tag name is used later in defining regions and boundaries. The second mesh line is placed at 9.0 μm and is tagged by the name 'right'.
The line statement fixes line locations in the mesh as well as the average spacing between lines.

The next section of input describes the location and spacings of

line y loc=0.0 tag=top spacing=0.05

line y loc=0.5 spacing=0.1

line y loc=0.5 spacing=0.1

line y loc=9.0 tag=bot

the vertical mesh lines. The first statement places a mesh line at the top of wafer, y coordinate 0.0μm and tags the line as "top". The spacing is set to 0.05μm. Two lines are placed at 0.5μm and 2.0μm respectively The spacing is set to 0.1μm. Finally a line is placed at 9.0μm, which is greater than the depth of the profile after the anneal. In the case where spacings are different in neighbor lines, the spacing is graded between them.

The next two sections describe the device starting material and the surfaces which are exposed to gas.

region silicon xlo=left xhi=right ylo=top yhi=bot

bound exposed xlo=left xhi=right ylo=top yhi=top

bound backside xlo=left xhi=right ylo=bot yhi=bot

The region statement is used to define the starting materials. In this case the wafer is silicon with no initial masking layers. The silicon area is defined to extend between the lines tagged left and right in the horizontal direction, and top and bottom in the vertical direction. Looking back at the mesh line definition section, this corresponds to the entire area that had been defined. The initial simulation area is completely silicon.

The bound statement allows the definition of the front and backsides of the wafer. Any gases on the diffusion statement, depositions, and etchings are applied to the surface marked exposed. It is important to define the top of the wafer for SUPREM4 to correctly simulate these actions.

The next line informs SUPREM4 that the mesh has been defined and should be computed.

init boron conc=3.0e14 ori=100

This statement computes the locations of lines given the spacings, triangulate the rectangular mesh, and computes geometry information. The initial doping is boron with a concentration of $3x10^{14}cm^{-3}$.

The next line adds a pad oxide to the wafer.

#growing if the gate oxide

oxide hcl.pc=2

diffuse time=38 temp=800 wet

The thickness of oxide growth is about 250Å.

Following the oxide growth, a mask is deposited and etched.

#do the phosphorus implant

deposit photores thick=2.0

etch photores left p1.x=4.0 p2.x=4.0

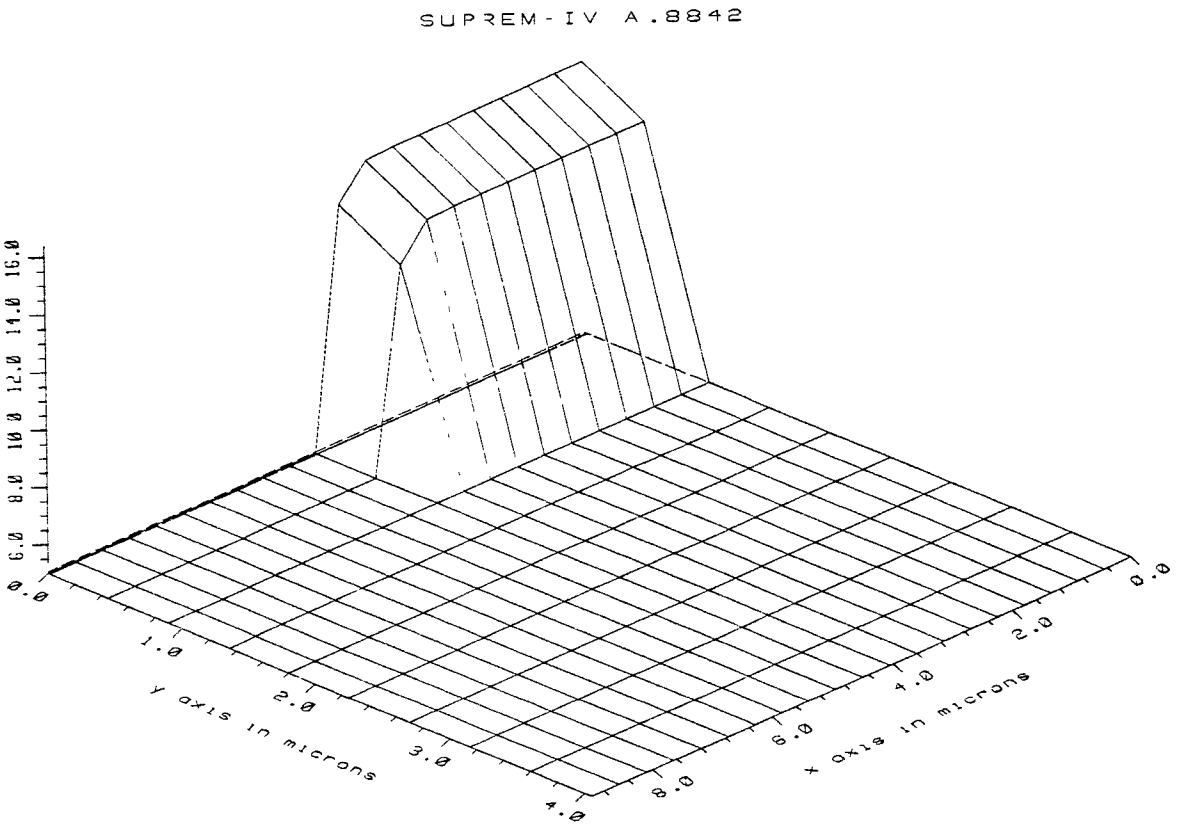

Figure 4.1: Doping profile after the 8μm wide channel implant

The mask material is specified to be 2.0μm thick of photoresist

The next statement performs the implant of phosphorus.

implant phos dose=5.0e11 energy=150.0 pearson

the implant is modeled with a Pearson-IV distribution. The energy and dose are 150Kev and $5*10^{11}cm^{-2}$. respectively. This produces an abrupt phosphorus profile as show in Fig. 4.1.

Then the second mask of phosphorus is defined and the implant of

etch photores left p1.x=8.0 p2.x=8.0

implant phos dose=1.3e12 energy=150.0 pearson

phosphorus is performed. This time the energy and dose are 150Kev and $1.3*10^{12}cm^{-2}$ respectively. the phosphorus profile is show in Fig. 4.2.

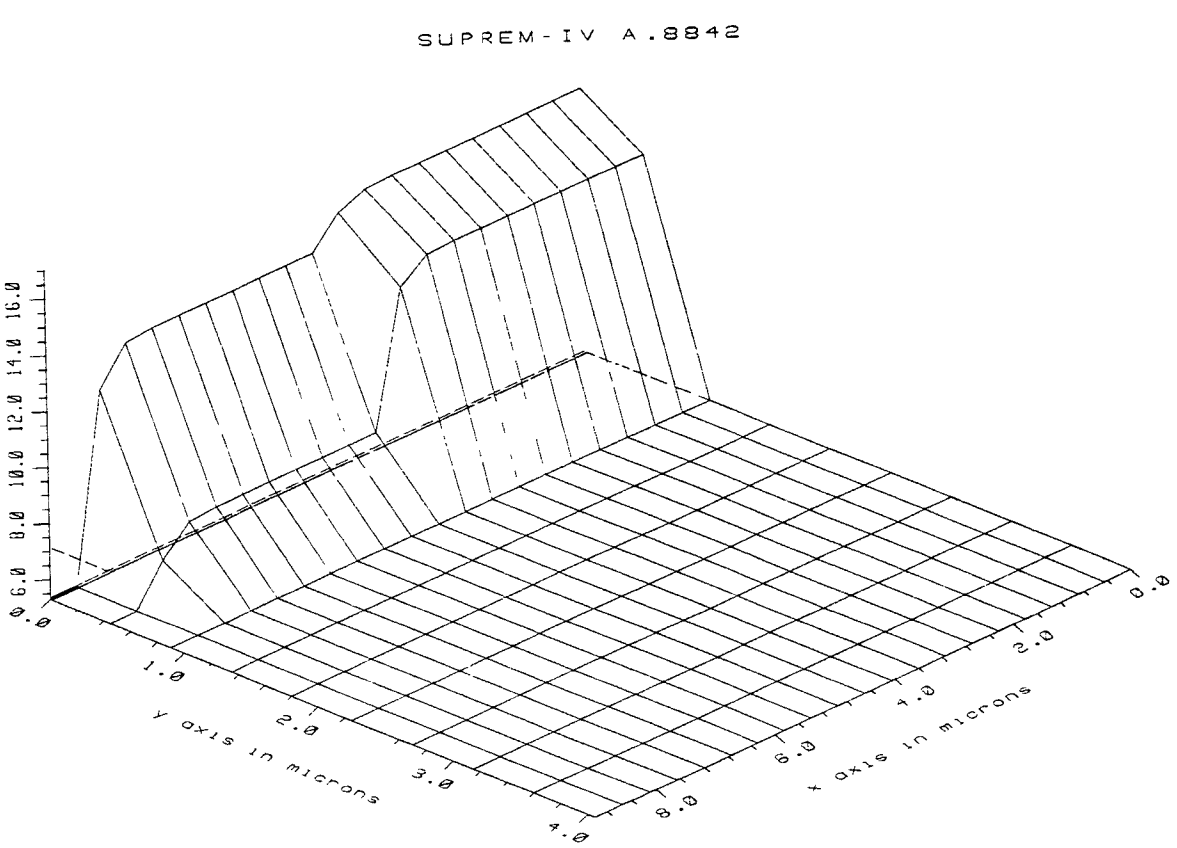

Figure 4.2: Doping profile after the 16μm wide channel implant

Following above step. the third mask of phosphorus is defined and the

deposit photores thick=2.0

etch photores left p1.x=2.0 p2.x=2.0

implant phos dose=5e11 energy=150.0 pearson

etch photores all

implant of phosphorus is performed. This time the energy and dose are 150kev and $5*10^{11}cm^{-2}$ respectively. the phosphorus profile is show in Fig. 4.3.

The next diffusion card contains the directive to simulate the 15 minutes 1100°C drive in and anneal.

diffuse time=15 temp=1000 nit

The following steps continue the diffusion process and the doping profile is shown in Fig. 4.4.

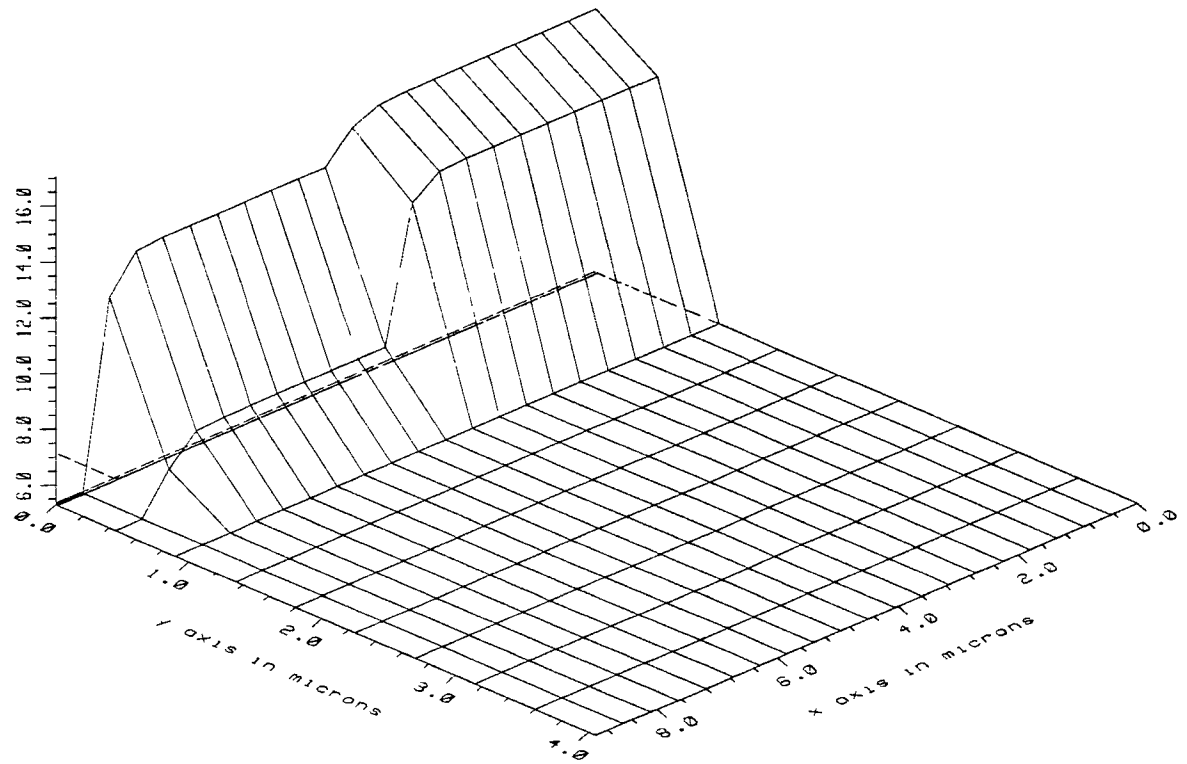

Figure 4.3: Doping profile after the 4μm wide channel implant

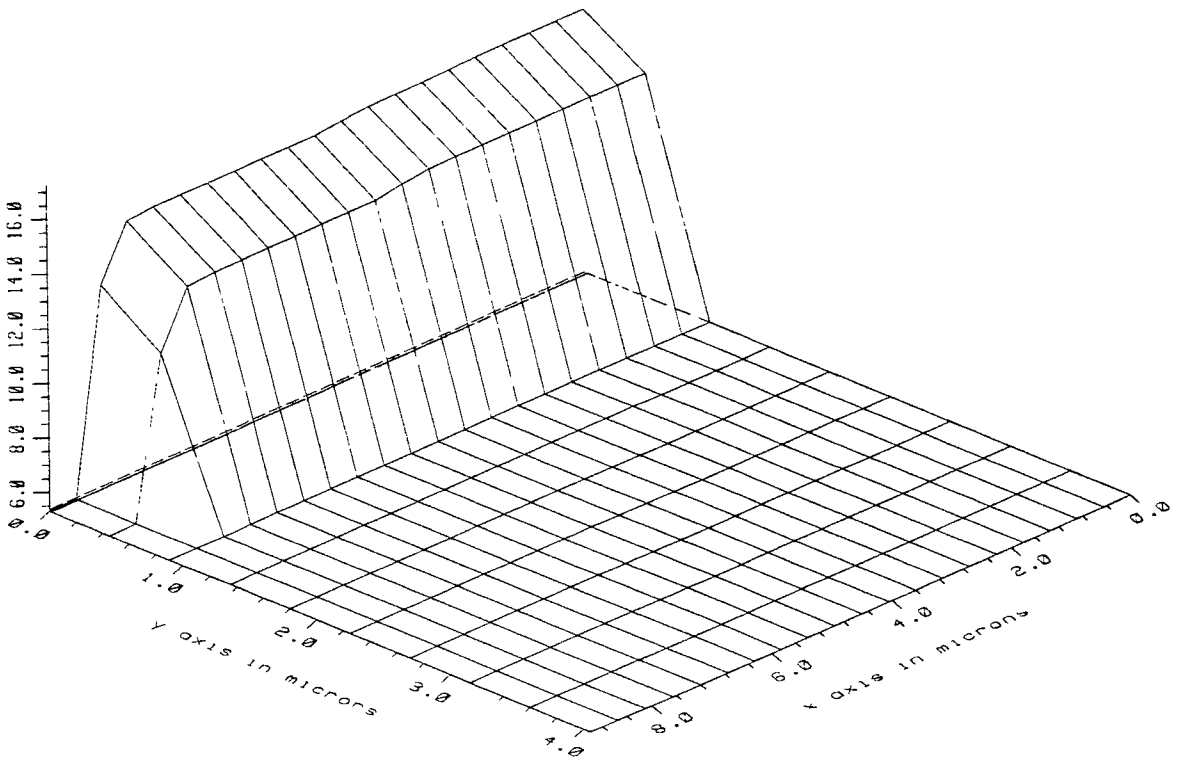

Figure 4.4: Doping profile after 15 minutes anneal

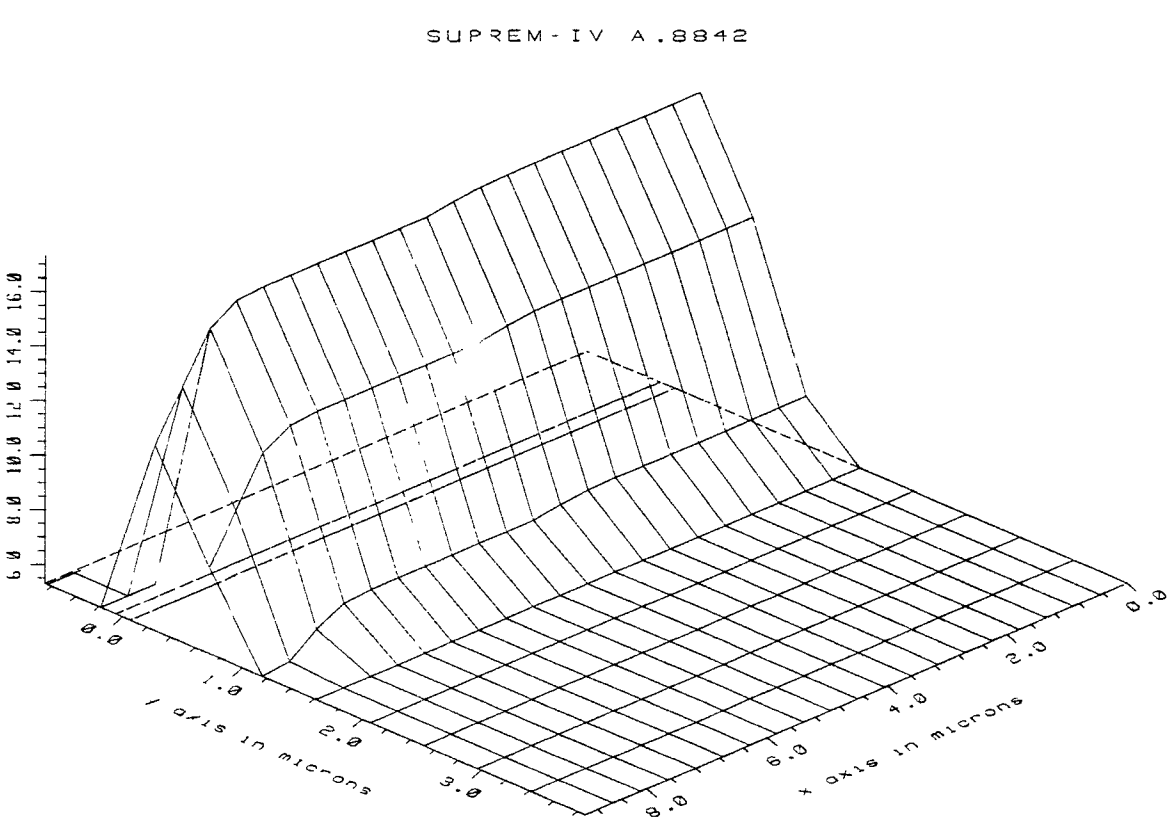

Figure 4.5: Doping profile after poly deposition and further annealing

The next cards define the poly deposition and anneal. The doping profile is shown in Fig. 4.5.

```
deposit poly thick=0.600 div=10
foreach val(0 to 29 step 1)
diffuse time=1 temp=800+val*5 nit
end
```

diffuse time=15 temp=950 phos gas.con=3.1585e20

In this card the solid solubility sets the concentration of the phosphorus in the ambient gas at the surface of the structure to the solid solubility of the impurity in polysilicon. The doping profile after this diffusion step is shown in Fig. 4.6.

The remaining diffusion cards contain the directives to simulate the drive in and anneal.

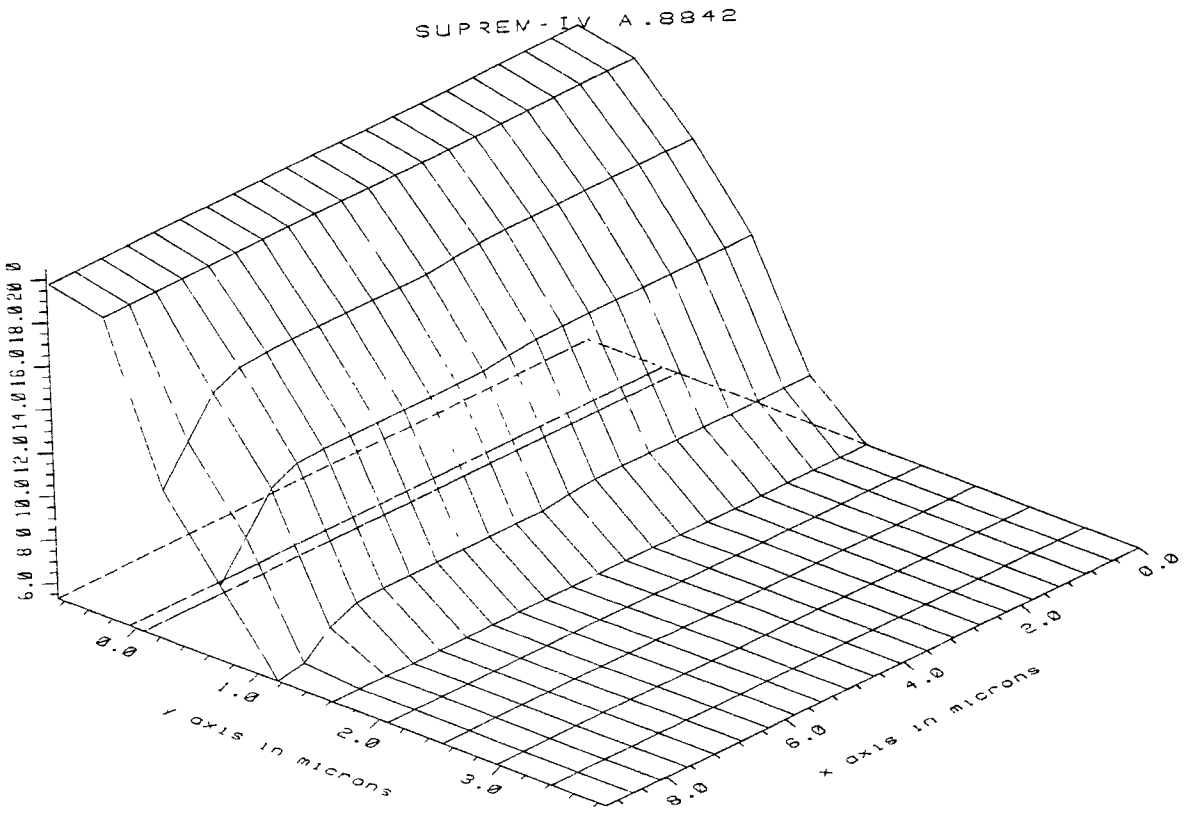

Figure 4.6: Doping profile after the diffusion step where solubility of phosphorus was set to $3.1585*10^{20}cm^{-3}$

.....

diffuse time=15 temp=1000 nit

foreach val(0 to 49 step 1)

diffuse time=1 temp=950-val*3 nit

end

Fig. 4.7 shows the final doping profile of the GBCCD structure.

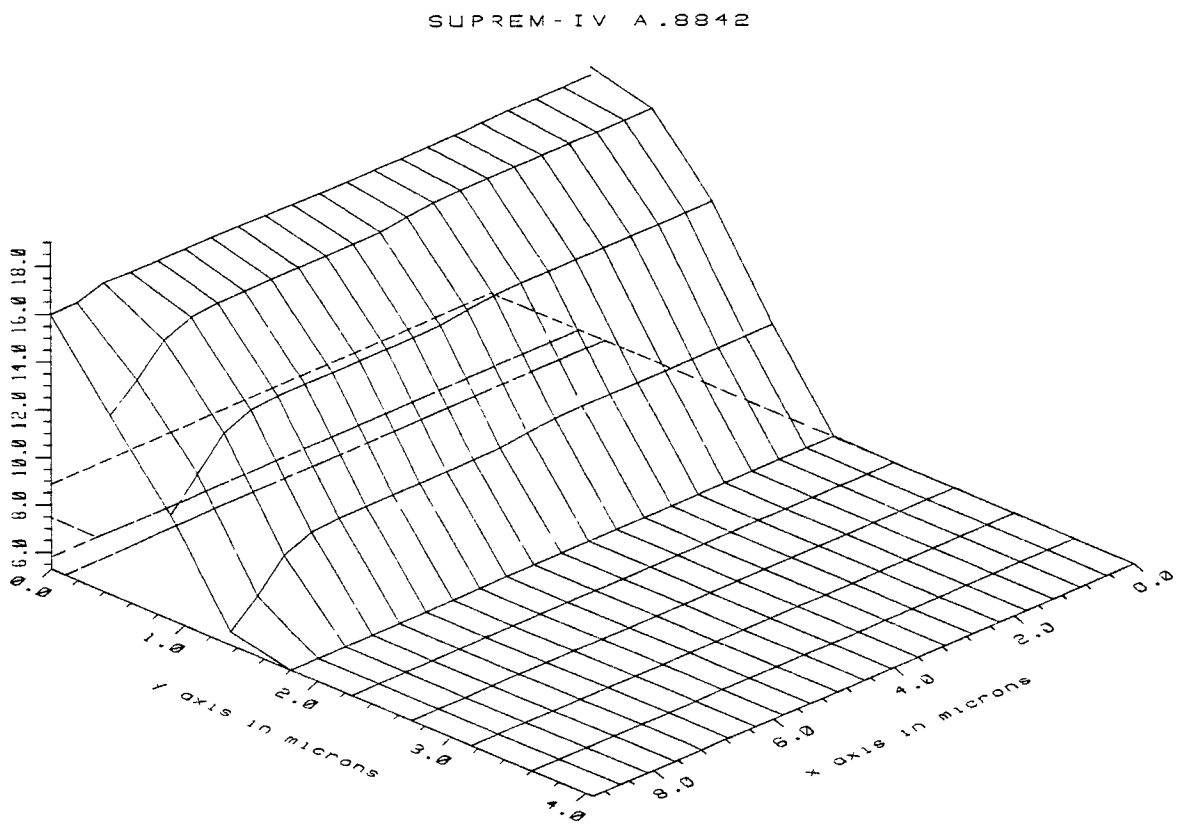

Figure 4.7: Doping profile after the final diffusion

Chapter 5

Results of 2-D Device Simulation

5.1 Enhancements of PISCES-2B

PISCES-2B contains a number of enhancements over version 2-A. The major additions are as follow :

1) lumped resistive

2) distributed contact resistance.

3) small-signal analysis.

4) a new grid generation program.

But PISCES-2B version 8822 had a bug in the extract card which integrates the electron concentration. It also cannot estimate the distribution area of electrons which is critical in this GBCCD simulation. Fortunately PISCES-2B has the print card which can print specific quantities at points within a defined area of the device.

PRINT POINTS can print the physical coordinate information for points along X grid lines as well as Y grid lines. Its output data file takes the format as shown in Fig. 5.1.

PRINT SOLUTION can print the electron concentration at each point. Its output data file takes the format as shown in Fig. 5.2.

These two data files offer us valuable information. A parameter-extract program written in Fortran77 has been coded and executed. This program can read the two data files generated by PISCES2, extract the useful data, then do necessary data processing and finally give the number of electrons and the area they occupy. Refer to Appendix C for the source program. Figures 5.3 and 5.4 give the flow charts for calculating the number of electrons and estimating the distribution area.

5.2 Simulation of normal BCCD with single implant

This section shows PISCES simulation results of normal BCCD with single implant. The buried channel was obtained by implanting phosphorous ions (dose=2.0e12cm^{-2}, energy=180Kev) in a boron substrate of doping 3e14cm^{-3}. The polysilicon electrode length is 16 μm. The whole processing steps including ion implantation, oxide growth, anneal cycles and polysilicon deposition are simulated by SUPREM4. The output of SUPREM4 is used as input to the PISCES.

In PISCESIIb N.BIAS and P.BIAS specify fixed quasi-Fermi potentials for carriers (electrons and holes, respectively)[17]. The N-type buried channel in BCCD can be depleted by slowly increasing the N.BIAS voltage. Combined with the our parameter extract program we can check how many signal charges

1 Node information :

Node (#)	x coord (um)	y coord (um)	Doping (cm-3)	Qf (cm-2)	Material (#)	Electrode (#)
1	0.000E+00	6.452E-02	2.075E+17	1.000E+10	1	0
2	0.000E+00	1.044E-01	1.841E+17	1.000E+10	1	0
3	0.000E+00	1.664E-01	7.830E+16	1.000E+10	1	0
4	0.000E+00	2.359E-01	3.905E+16	1.000E+10	1	0
5	0.000E+00	3.140E-01	2.130E+16	1.000E+10	1	0
6	0.000E+00	4.016E-01	6.897E+15	1.000E+10	1	0
7	0.000E+00	5.000E-01	1.088E+15	1.000E+10	1	0
8	0.000E+00	6.000E-01	-1.104E+14	1.000E+10	1	-2
9	0.000E+00	7.000E-01	-2.799E+14	1.000E+10	1	-2
10	0.000E+00	8.000E-01	-2.983E+14	1.000E+10	1	-2
11	0.000E+00	9.000E-01	-2.999E+14	1.000E+10	1	-2
12	0.000E+00	1.000E+00	-3.000E+14	1.000E+10	1	-2
13	0.000E+00	1.100E+00	-3.000E+14	1.000E+10	1	-2
14	0.000E+00	1.200E+00	-3.000E+14	1.000E+10	1	-2
15	0.000E+00	1.300E+00	-3.000E+14	1.000E+10	1	-2
16	0.000E+00	1.400E+00	-3.000E+14	1.000E+10	1	-2
17	0.000E+00	1.500E+00	-3.000E+14	1.000E+10	1	-2
18	0.000E+00	1.600E+00	-3.000E+14	1.000E+10	1	-2
19	0.000E+00	1.700E+00	-3.000E+14	1.000E+10	1	-2
20	0.000E+00	1.800E+00	-3.000E+14	1.000E+10	1	-2
21	0.000E+00	1.900E+00	-3.000E+14	1.000E+10	1	-2
22	0.000E+00	2.000E+00	-3.000E+14	1.000E+10	1	-2
23	0.000E+00	2.098E+00	-3.000E+14	1.000E+10	1	-2
24	0.000E+00	2.245E+00	-3.000E+14	1.000E+10	1	-2
25	0.000E+00	2.462E+00	-3.000E+14	1.000E+10	1	-2
26	0.000E+00	2.786E+00	-3.000E+14	1.000E+10	1	-2
27	0.000E+00	3.268E+00	-3.000E+14	1.000E+10	1	-2
28	0.000E+00	3.985E+00	-3.000E+14	1.000E+10	1	-2
29	0.000E+00	5.052E+00	-3.000E+14	1.000E+10	1	-2
30	0.000E+00	6.639E+00	-3.000E+14	1.000E+10	1	-2
31	0.000E+00	9.000E+00	-2.564E+14	1.000E+10	1	2
32	5.000E-01	6.452E-02	2.075E+17	1.000E+10	1	0
33	5.000E-01	1.044E-01	1.841E+17	1.000E+10	1	0
34	5.000E-01	1.664E-01	7.830E+16	1.000E+10	1	0
35	5.000E-01	2.359E-01	3.905E+16	1.000E+10	1	0
36	5.000E-01	3.140E-01	2.130E+16	1.000E+10	1	0
37	5.000E-01	4.016E-01	6.897E+15	1.000E+10	1	0
38	5.000E-01	5.000E-01	1.088E+15	1.000E+10	1	0
39	5.000E-01	6.000E-01	-1.104E+14	1.000E+10	1	-2
40	5.000E-01	7.000E-01	-2.799E+14	1.000E+10	1	-2
41	5.000E-01	8.000E-01	-2.983E+14	1.000E+10	1	-2
42	5.000E-01	9.000E-01	-2.999E+14	1.000E+10	1	-2
43	5.000E-01	1.000E+00	-3.000E+14	1.000E+10	1	-2
44	5.000E-01	1.100E+00	-3.000E+14	1.000E+10	1	-2
45	5.000E-01	1.200E+00	-3.000E+14	1.000E+10	1	-2
46	5.000E-01	1.300E+00	-3.000E+14	1.000E+10	1	-2
47	5.000E-01	1.400E+00	-3.000E+14	1.000E+10	1	-2
..	.....	.....	.....	.....	...	...
1158	-9.000E+00	2.098E+00	-3.000E+14	1.000E+10	1	-2
1159	-9.000E+00	2.245E+00	-3.000E+14	1.000E+10	1	-2
1160	-9.000E+00	2.462E+00	-3.000E+14	1.000E+10	1	-2
1161	-9.000E+00	2.786E+00	-3.000E+14	1.000E+10	1	-2
1162	-9.000E+00	3.268E+00	-3.000E+14	1.000E+10	1	-2
1163	-9.000E+00	3.985E+00	-3.000E+14	1.000E+10	1	-2
1164	-9.000E+00	5.052E+00	-3.000E+14	1.000E+10	1	-2
1165	-9.000E+00	6.639E+00	-3.000E+14	1.000E+10	1	-2
1166	-9.000E+00	9.000E+00	-2.564E+14	1.000E+10	1	2

Figure 5.1: Data file created by the PRINT POINTS command

Node	v	n	p	qfn	qfp
1	1.41503	1.3573E+17	2.4417E-14	1.0000E+00	0.0000E+00
2	1.42198	1.7754E+17	1.8667E-14	1.0000E+00	0.0000E+00
3	1.40106	7.9065E+16	4.1917E-14	1.0000E+00	0.0000E+00
4	1.38297	3.9270E+16	8.4394E-14	1.0000E+00	0.0000E+00
5	1.36459	1.9285E+16	1.7185E-13	1.0000E+00	0.0000E+00
6	1.32149	3.6405E+15	9.1037E-13	1.0000E+00	0.0000E+00
7	1.22743	9.5693E+13	3.4633E-11	1.0000E+00	0.0000E+00
8	1.11670	1.3206E+12	2.5096E-09	1.0000E+00	0.0000E+00
9	1.00770	1.9475E+10	1.7018E-07	1.0000E+00	0.0000E+00
10	0.90298	3.3908E+08	9.7742E-06	1.0000E+00	0.0000E+00
11	0.80285	7.0469E+06	4.7031E-04	1.0000E+00	0.0000E+00
12	0.70731	1.7498E+05	1.8940E-02	1.0000E+00	0.0000E+00
13	0.61638	5.1918E+03	6.3836E-01	1.0000E+00	0.0000E+00
14	0.53005	1.8407E+02	1.8005E+01	1.0000E+00	0.0000E+00
15	0.44832	7.7982E+00	4.2500E+02	1.0000E+00	0.0000E+00
16	0.37120	3.9478E-01	8.3950E+03	1.0000E+00	0.0000E+00
17	0.29868	2.3882E-02	1.3877E+05	1.0000E+00	0.0000E+00
18	0.23077	1.7264E-03	1.9197E+06	1.0000E+00	0.0000E+00
19	0.16746	1.4913E-04	2.2223E+07	1.0000E+00	0.0000E+00
20	0.10876	1.5394E-05	2.1529E+08	1.0000E+00	0.0000E+00
21	0.05466	1.8989E-06	1.7453E+09	1.0000E+00	0.0000E+00
22	0.00516	2.7990E-07	1.1841E+10	1.0000E+00	0.0000E+00
23	-0.03903	5.0642E-08	6.5443E+10	1.0000E+00	0.0000E+00
24	-0.09654	5.4739E-09	6.0545E+11	1.0000E+00	0.0000E+00
25	-0.16389	4.0440E-10	8.1952E+12	1.0000E+00	0.0000E+00
26	-0.22481	3.8315E-11	8.6499E+13	1.0000E+00	0.0000E+00
27	-0.25185	1.3464E-11	2.4615E+14	1.0000E+00	0.0000E+00
28	-0.25657	1.1218E-11	2.9545E+14	1.0000E+00	0.0000E+00
29	-0.25695	1.1054E-11	2.9981E+14	1.0000E+00	0.0000E+00
30	-0.25691	1.1069E-11	2.9942E+14	1.0000E+00	0.0000E+00
31	-0.25290	1.2927E-11	2.5637E+14	1.0000E+00	0.0000E+00
32	1.41503	1.3573E+17	2.4417E-14	1.0000E+00	0.0000E+00
33	1.42198	1.7754E+17	1.8667E-14	1.0000E+00	0.0000E+00
34	1.40106	7.9065E+16	4.1917E-14	1.0000E+00	0.0000E+00
35	1.38297	3.9270E+16	8.4394E-14	1.0000E+00	0.0000E+00
36	1.36459	1.9285E+16	1.7185E-13	1.0000E+00	0.0000E+00
37	1.32149	3.6402E+15	9.1045E-13	1.0000E+00	0.0000E+00
38	1.22742	9.5661E+13	3.4645E-11	1.0000E+00	0.0000E+00
39	1.11669	1.3198E+12	2.5111E-09	1.0000E+00	0.0000E+00
40	1.00768	1.9458E+10	1.7033E-07	1.0000E+00	0.0000E+00
41	0.90296	3.3870E+08	9.7851E-06	1.0000E+00	0.0000E+00
42	0.80281	7.0374E+06	4.7094E-04	1.0000E+00	0.0000E+00
43	0.70727	1.7471E+05	1.8970E-02	1.0000E+00	0.0000E+00
44	0.61633	5.1828E+03	6.3946E-01	1.0000E+00	0.0000E+00
45	0.53000	1.8372E+02	1.8039E+01	1.0000E+00	0.0000E+00
46	0.44827	7.7825E+00	4.2585E+02	1.0000E+00	0.0000E+00
47	0.37115	3.9395E-01	8.4127E+03	1.0000E+00	0.0000E+00
..	.....	.....	.....	.....	.....
1158	-0.17031	3.1556E-10	1.0503E+13	1.0000E+00	0.0000E+00
1159	-0.19962	1.0153E-10	3.2643E+13	1.0000E+00	0.0000E+00
1160	-0.22911	3.2453E-11	1.0212E+14	1.0000E+00	0.0000E+00
1161	-0.24883	1.5132E-11	2.1902E+14	1.0000E+00	0.0000E+00
1162	-0.25568	1.1608E-11	2.8551E+14	1.0000E+00	0.0000E+00
1163	-0.25686	1.1091E-11	2.9881E+14	1.0000E+00	0.0000E+00
1164	-0.25696	1.1050E-11	2.9994E+14	1.0000E+00	0.0000E+00
1165	-0.25691	1.1068E-11	2.9943E+14	1.0000E+00	0.0000E+00
1166	-0.25290	1.2927E-11	2.5637E+14	1.0000E+00	0.0000E+00

Figure 5.2: Data file created by the PRINT SOLUTION command

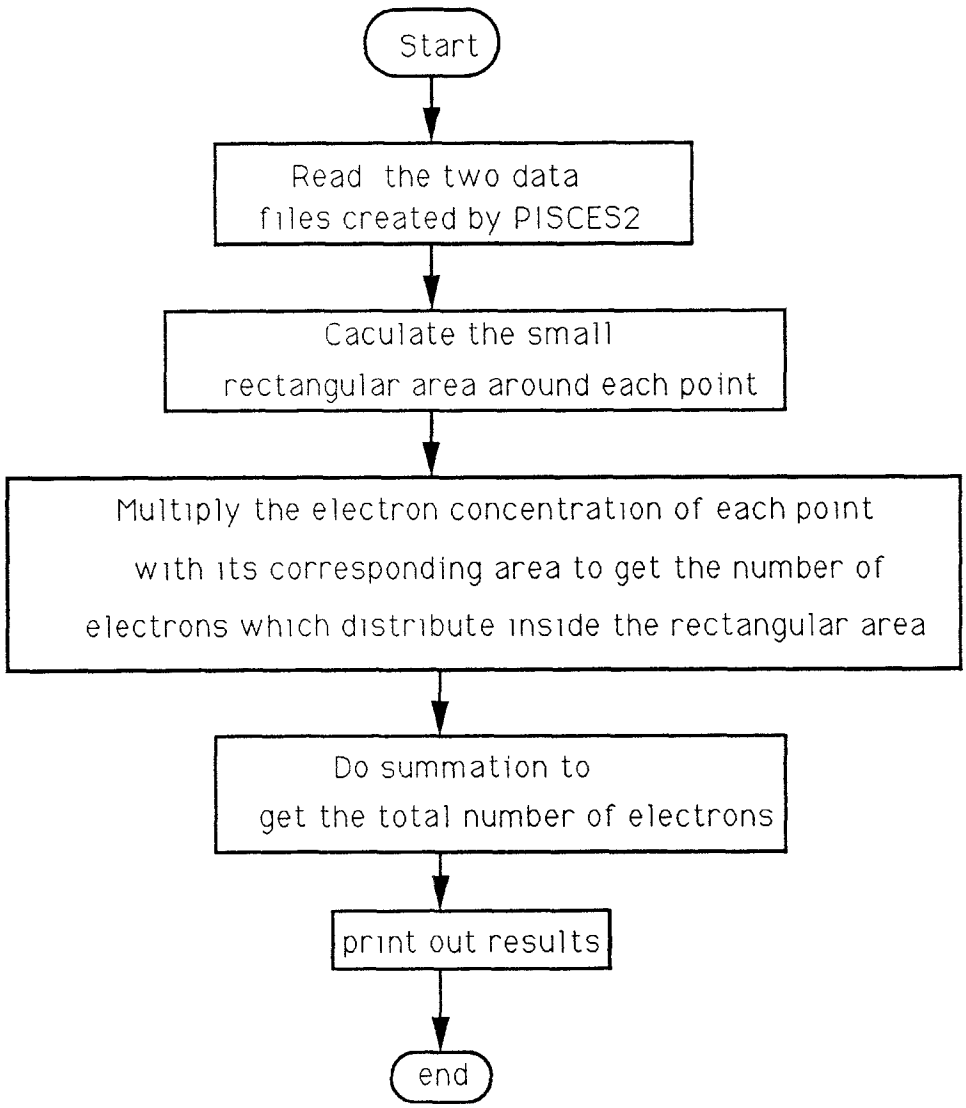

Figure 5.3: Flow chart for calculating the number of electrons

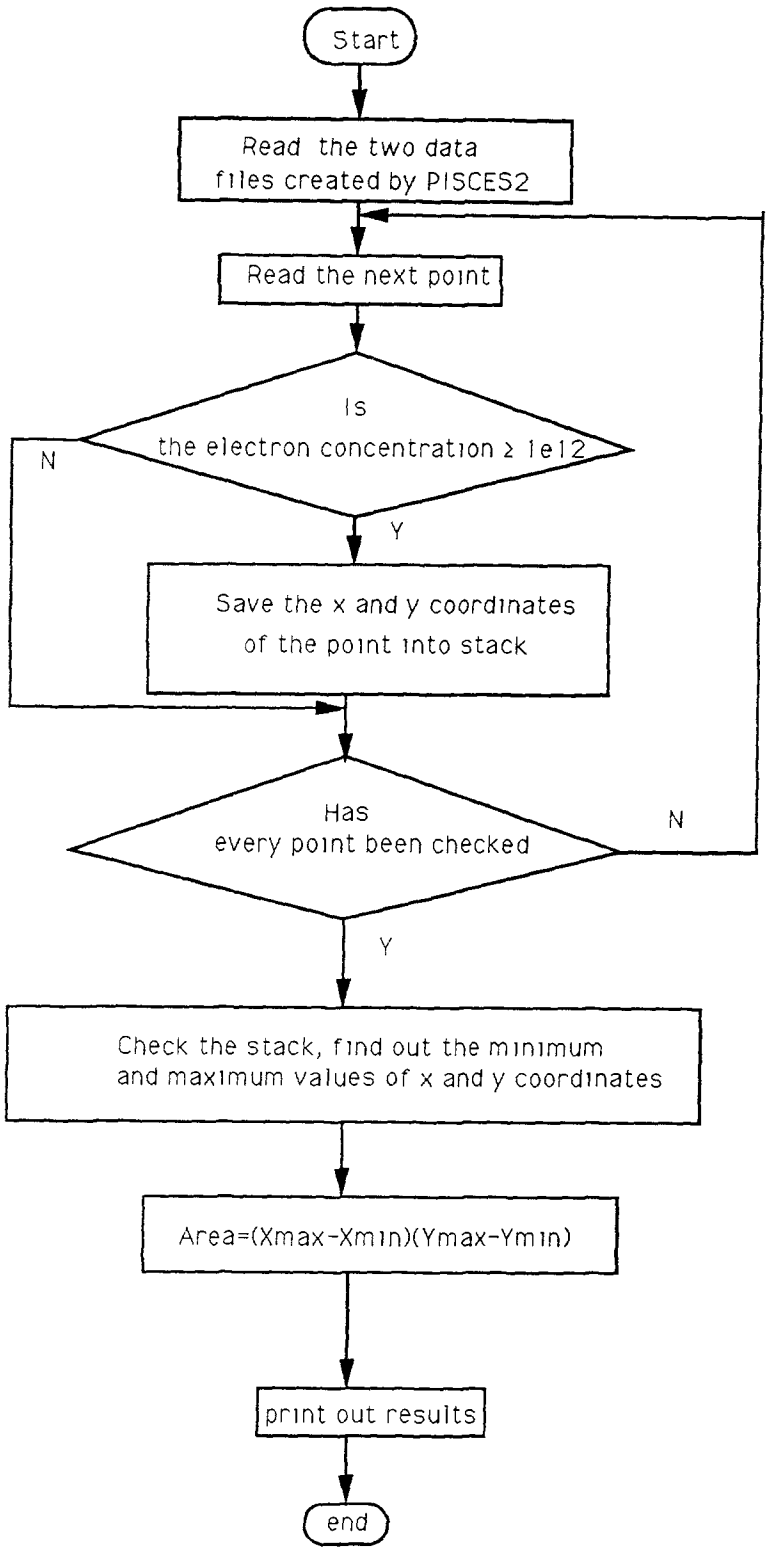

Figure 5.4: Flow chart for estimating the electron distribution area

are left in channel and how they are distributed. Table 5.1 shows the relationship between the number of signal charges per micron of channel length and the area they occupy in the normal BCCD. The boundary of the charge packet area has been defined here by the perimeter at which the charge concentration is reduced to $\leq 10^{12}\text{cm}^{-3}$, i.e. one electron per μm^3. Figure 5.5 shows the curve of distribution area versus the number of signal charges based on the data of Table 5.1.

We can get the area per electron value by simply dividing the charge packet area by the number of electrons. The curve of area per electron versus the number of electrons is plotted in Fig. 5.25. This curve represents the transfer inefficiency, since the transfer inefficiency is proportional to the area per electron.

Figure 5.7 illustrates the change of the two dimensional charge packet boundaries for increasing the signal level.

Figures 5.8, 5.9 and 5.10 show the 3-D potential profiles with empty well, a small signal packet and a large signal packet, respectively.

5.3 Simulation of Graded BCCD with double implants

As discussed in Chapter 3, the volume of bulk silicon per electron is greatest for small signal packet. Figures 5.5 and 5.6 also verified this conclusion. The slope of the curve in Fig. 5.5 is steepest when the amount of charges is small, i.e. the area of bulk silicon per electron is greatest for small signal packet as shown in Fig. 5.6. The value of area per electron for small signal level is around $3.5 \times 10^{-3}\mu\text{m}^2$/per electron which is almost 1 order of magnitude

Number of electrons	Occupied area (μm^2)
0	0 0
1427	5 0
13147	6 5
28317	7 0
44814	7 3
61798	7 5
79893	7 7
99301	8 0
119280	8 1
139632	8 2
160645	9.6
173533	1 0

Table 5.1: Normal BCCD with single implant (16μm)

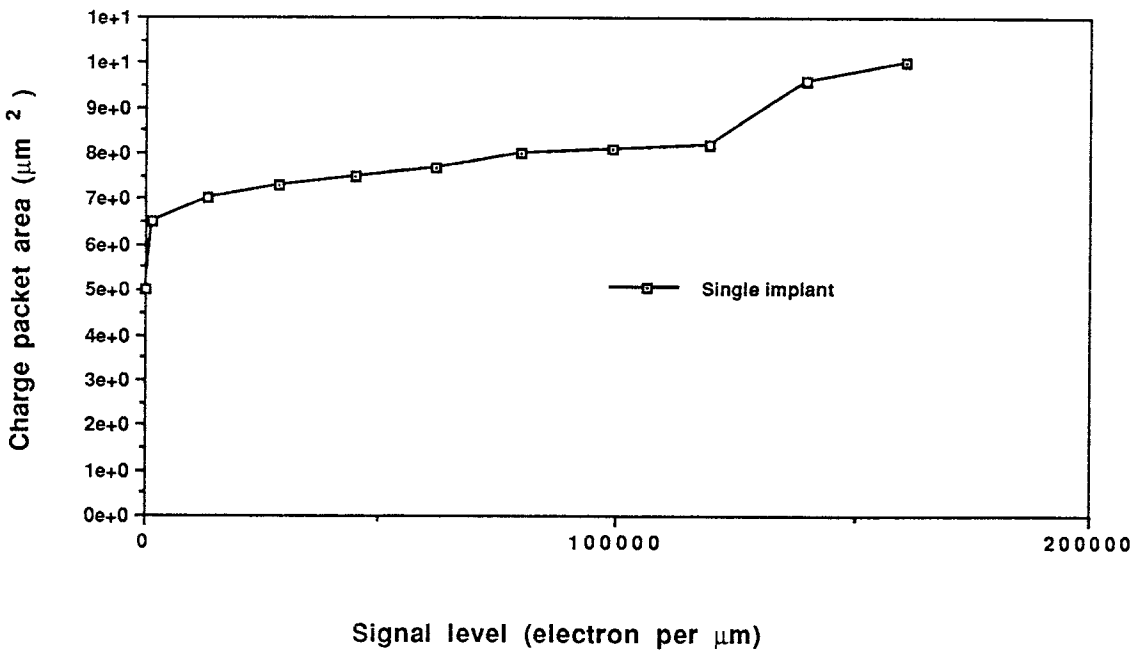

Figure 5.5: Charge distribution area as a function of signal level (single implant)

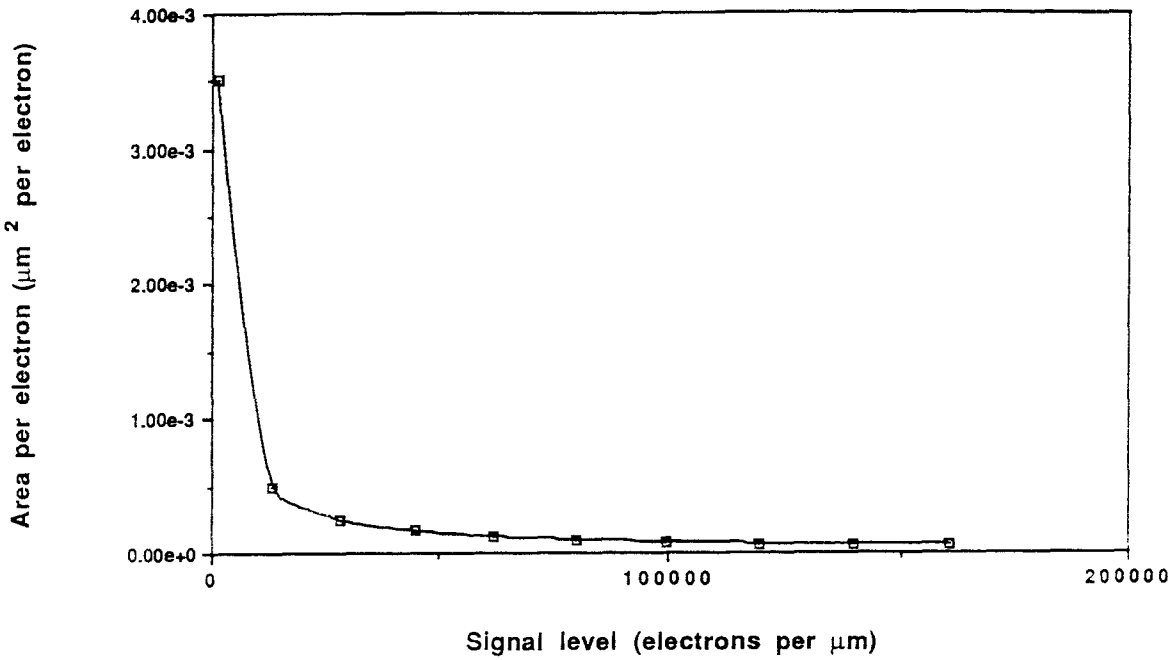

Figure 5.6: Area per electron as a function of of signal level (single implant)

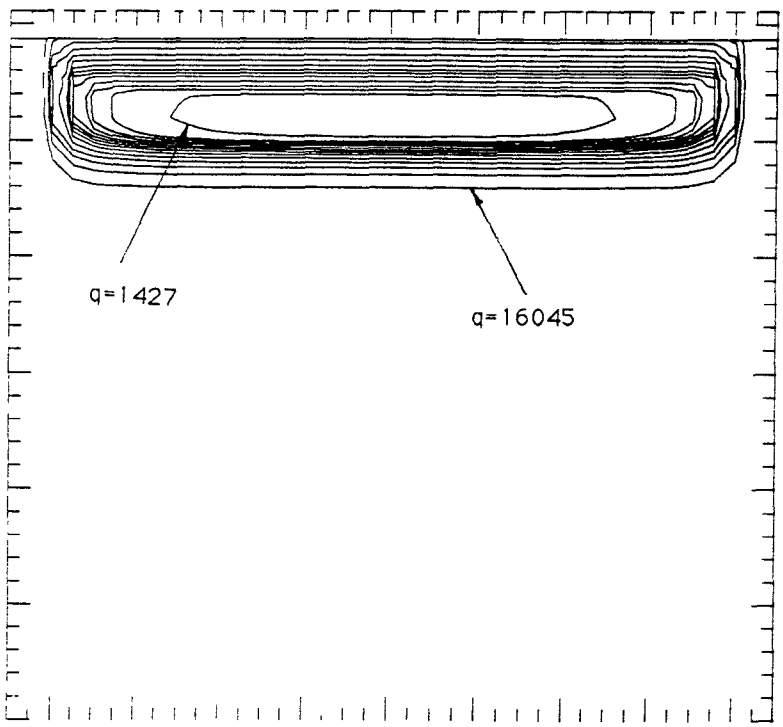

Figure 5.7: Two dimensional boundaries of the charge signal packets for different signal level in electrons per one micron channel length. (single implant)

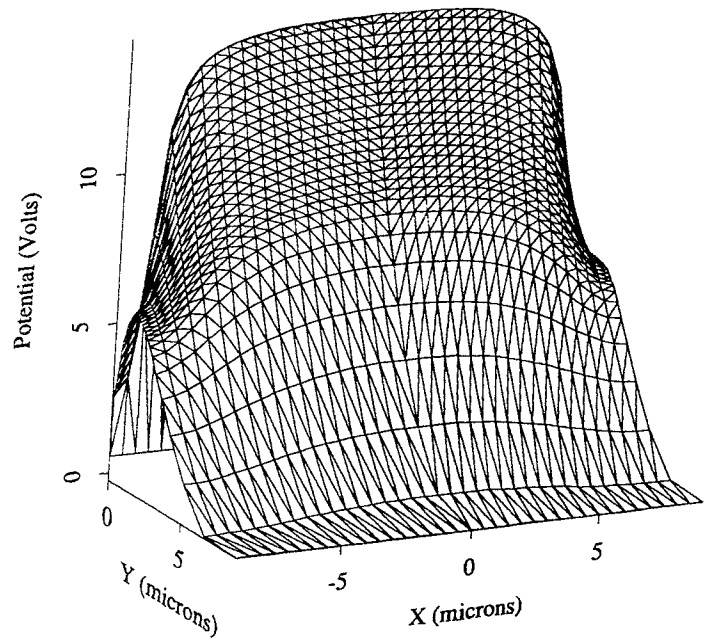

Figure 5.8: Potential profile of the Normal BCCD with empty well

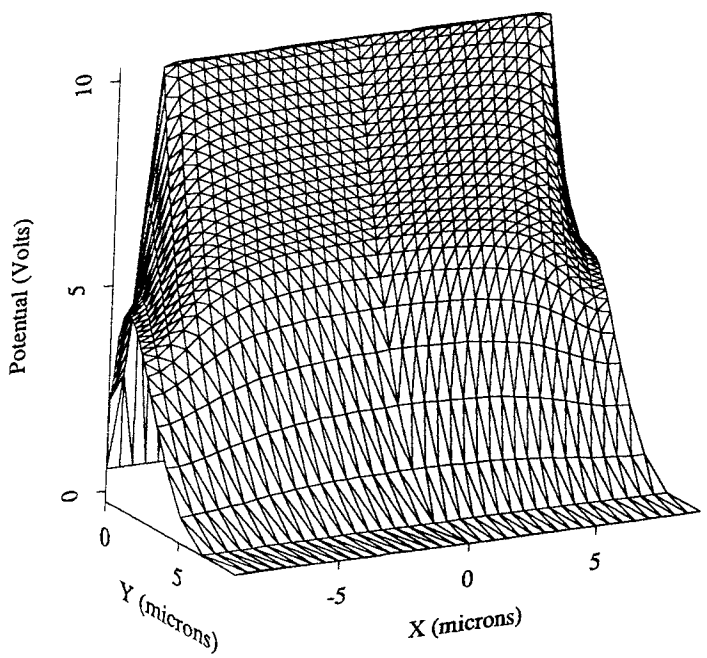

Figure 5.9: Potential profile of the Normal BCCD with small signal packet

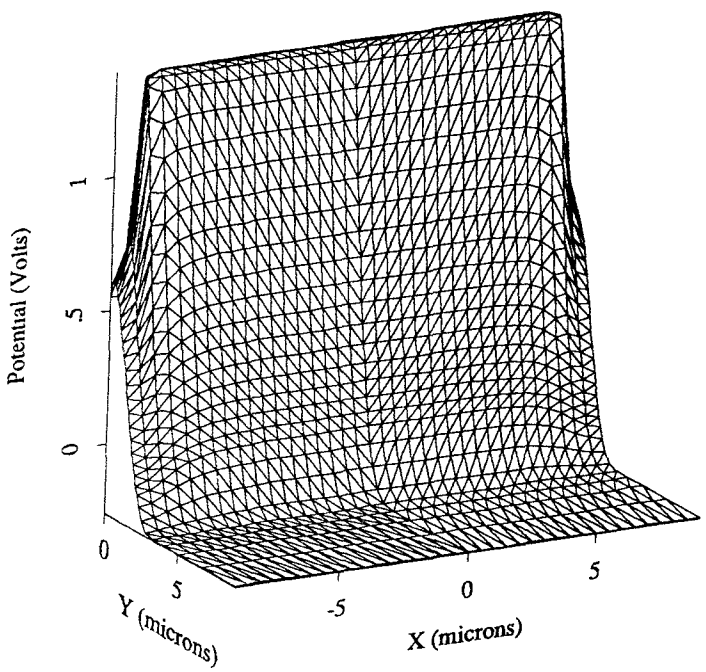

Figure 5.10: Potential profile of the Normal BCCD with large signal packet

higher than the value for high signal level which is about $4 \times 10^{-4}\mu m^2$/per electron. This means the transfer inefficiency for the small signal packet is expected to be much higher than for the large signal packet. In order to solve this problem an additional smaller BCCD implant (4μm) was added to the normal 16-μm-wide BCCD. The implant dopant for the 4μm mask in this study was either phosphorus or arsenic.

5.3.1 Case 1 – 4μm phosphorus implant

In this case the 4μm buried channel was obtained by implanting phosphorous ions (dose=0.5e12cm^{-2}, energy=150Kev) into the substrate. Table 5.2 gives number of electrons and the corresponding area they occupy. Figure 5.11 shows a plot of the area per electron versus the signal level for both single implant and double implant BCCD cases.

A comparison of the two curves in Figure 5.11 indicates that the area per

Number of electrons	Occupied area (μm^2)
0..0	0 0
1034	1.2
5499	1 3
11099	1 6
19358	6 5
35348	7 0
54297	7 5
75150	7 6
97300	7 7
120589	8 0
144940	9 6

Table 5.2: Graded BCCD with double implants (Phosphorus is used for $4\mu m$ buried channel implant, Case 1)

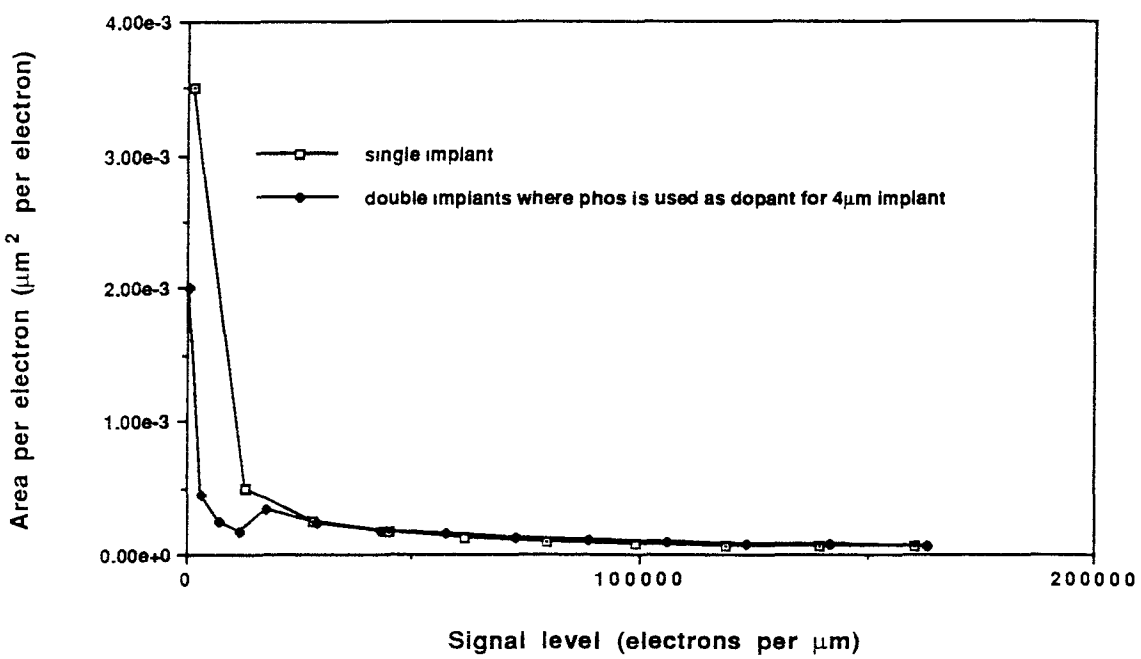

Figure 5.11: Area per electron as a function of signal level for double implant case (Case 1)

Number of electrons	Occupied area (μm^2)
0 0	0 0
2596	1 2
8027	1.6
16174	4 8
32355	5 9
51696	7 3
72716	7 6
94845	7 7
118056	8 0
143086	9 6

Table 5.3: Graded BCCD with double implants (Arsenic is used for 4μm buried channel implant, Case 2)

electron for small signal packet in the case of the double implant BCCD is much smaller than that for a normal BCCD, i.e. the signal loss due to bulk traps is smaller for the double implant case and therefore the transfer efficiency should be improved.

5.3.2 Case 2 – 4μm arsenic implant

In this case the 4μm buried channel was obtained by implanting arsenic ions (dose=0.5e12cm^{-2}, energy=180Kev) into the substrate.

Table 5.3 gives number of electrons and the corresponding area they occupy. Figure 5.12 shows the curve of distribution area versus the signal level based on the data of Table 5.3.

We obtain the verification of the simulation results by comparing of the simulation results with the experimental results[3].

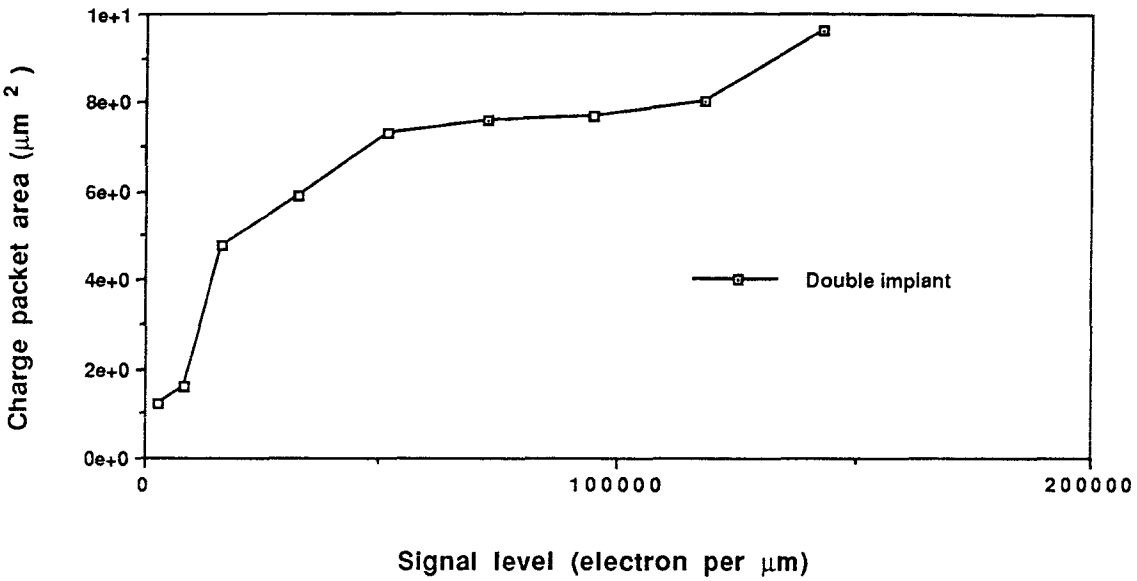

Figure 5.12: Distribution area as a function of the signal level (Case 2)

Figure 5.12 shows the curve of the charge packet areas versus the signal level and Fig. 3.3 shows the curves of total loss in electrons versus the signal level. Since both of the above curve have the same shape we conclude that the simulation results confirm the experimental measurements.

Figure 5.13 shows the curves of area per electron versus the signal level. For easy to compare we convey the curve representing transfer inefficiency versus the signal level in Fig. 3.4 into the curve representing area per electron versus the signal level by aid of Eq.2.5. This experimental curve is also shown in Fig. 5.13. Again, this confirms that simulation results are consistent with the experimental measurements.

The rest of this section will demonstrate the characteristics of this double implant BCCD in great detail. Figure 5.14 plots the change of the boundaries of the signal charge packets for increasing the charge signal levels.

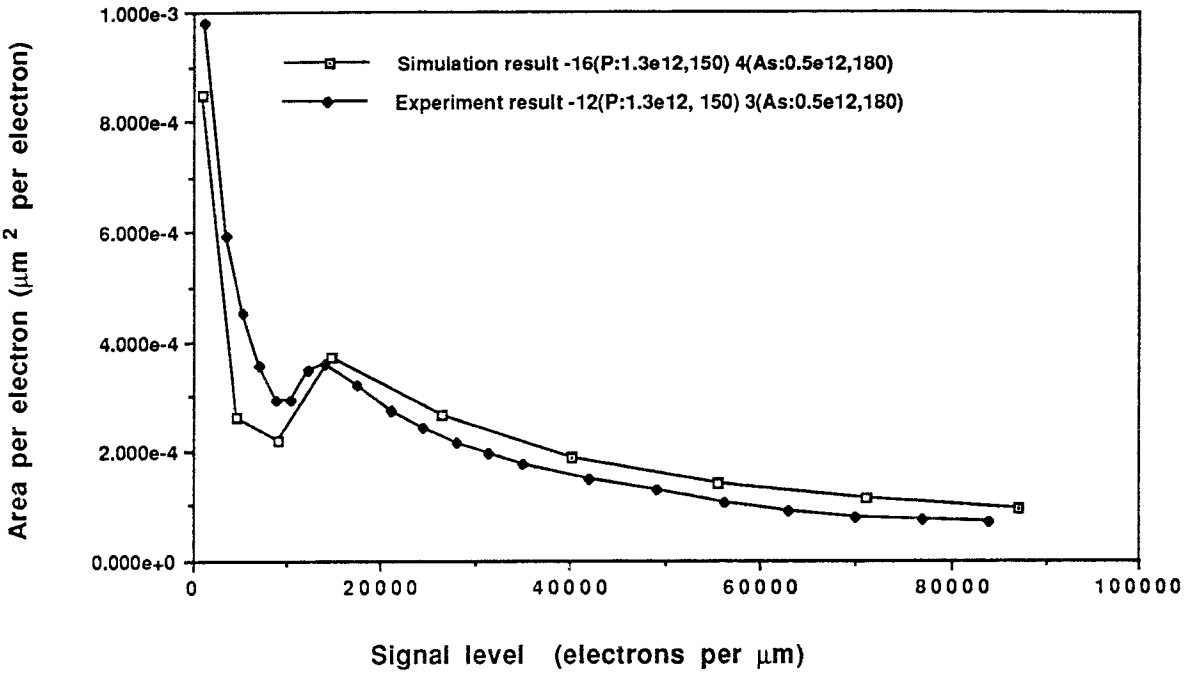

Figure 5.13: Area per electron as a function of the signal level (Case 2)

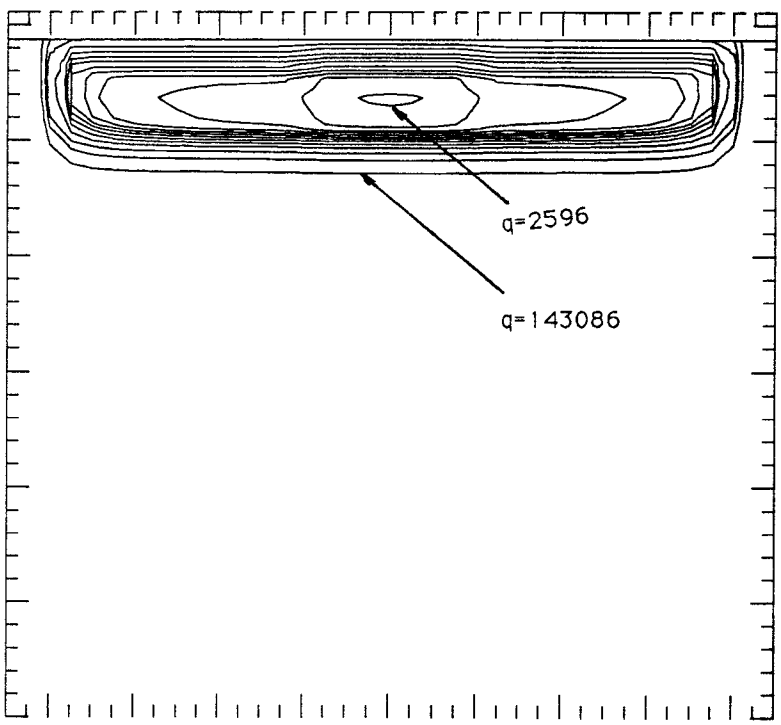

Figure 5.14: Changes of the occupy area for increasing signal level (Case 2)

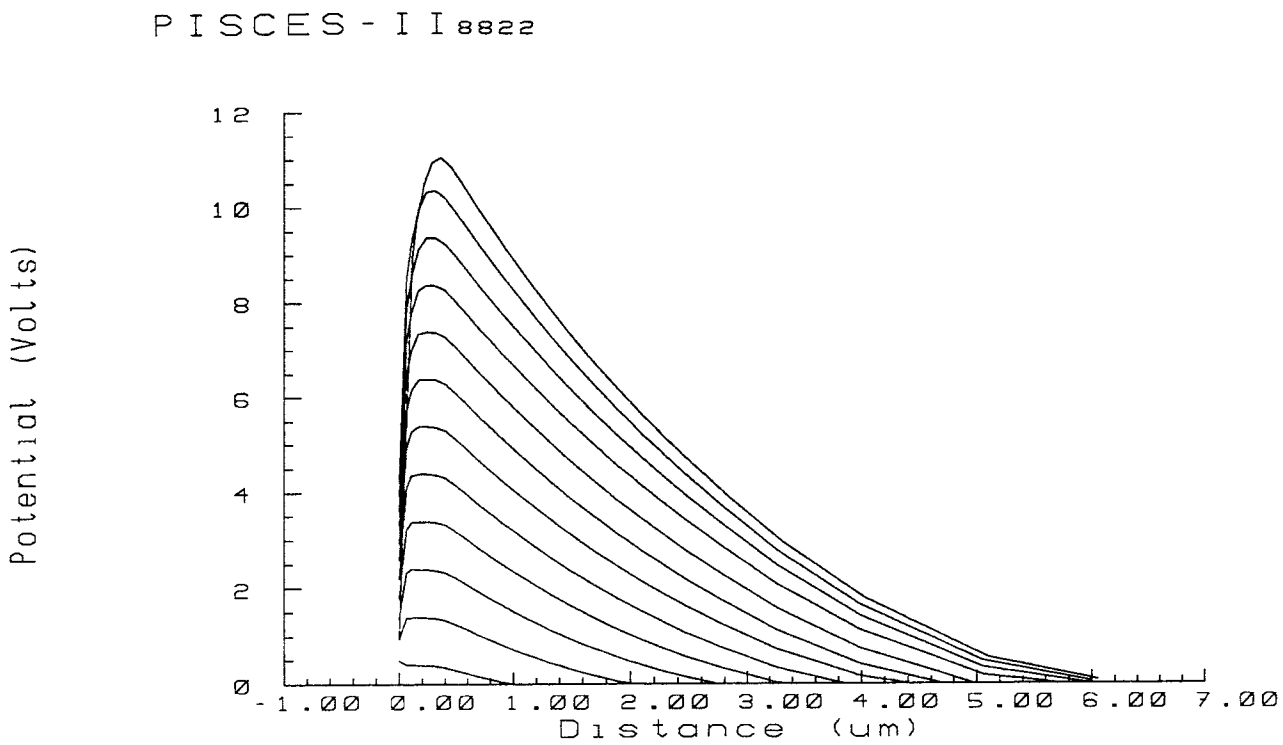

Figure 5.15: Potential profile of the GBCCD vertical to the buried channel corresponding to the empty well, partially filled well and full well (Case2)

The 1-D potential profile across the middle section from the surface to the backside for different bias voltages is shown in Fig. 5.15. The 1-D potential profile along the buried channel (0.3 μm) away from surface for different bias voltages is shown in Fig. 5.16.

Figures 5.17, 5.18 and 5.19 show the 3-D potential profiles with an empty well, a small signal packet and a large signal packet, respectively.

The dynamic range of gate voltage is an important factor in the designing of buried channel device. In order to obtain this characteristics, a gate voltage is applied in steps to the polysilicon gate. A curve of the maximum potential for an empty well as a function of gate voltage is shown in Fig. 5.20. The channel potential decreases as the gate voltage becomes more negative. Finally the pinning voltage is reached. Inspection of the Fig. 5.20 shows that the pinning voltage V_{pin} is about -10V.

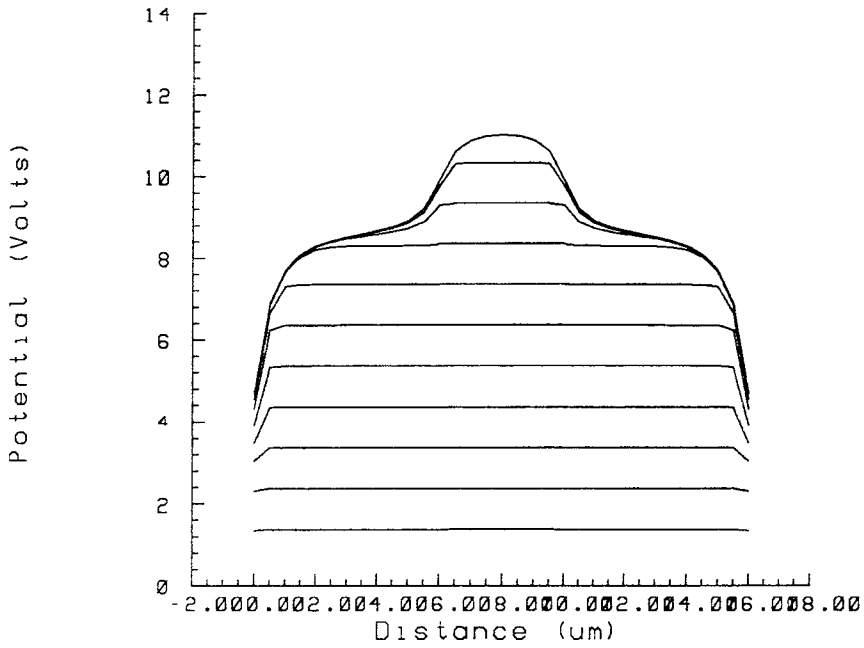

Figure 5.16: Potential profile of the GBCCD along the buried channel corresponding to the empty well, partially filled well and full well (Case2)

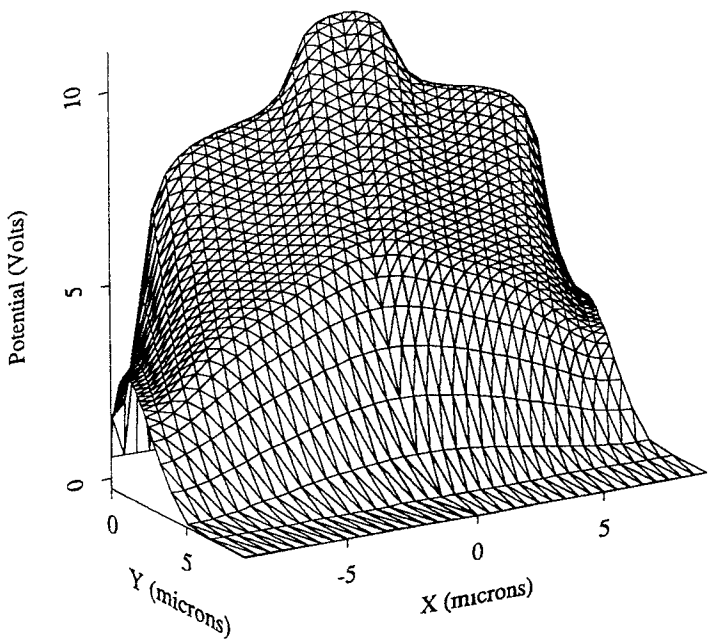

Figure 5.17: Potential profile of the GBCCD with empty well (Case2)

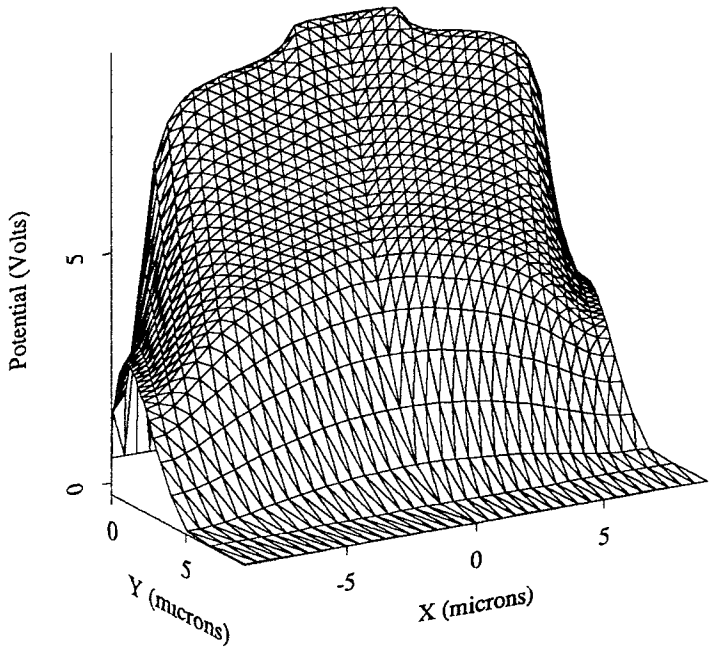

Figure 5.18: Potential profile of the GBCCD with small signal packet (Case2)

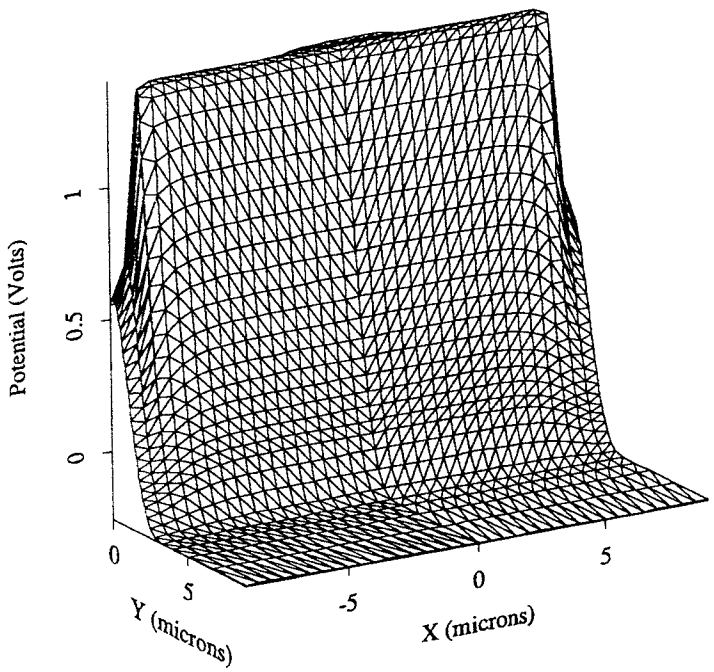

Figure 5.19: Potential profile of the GBCCD with large signal packet (Case2)

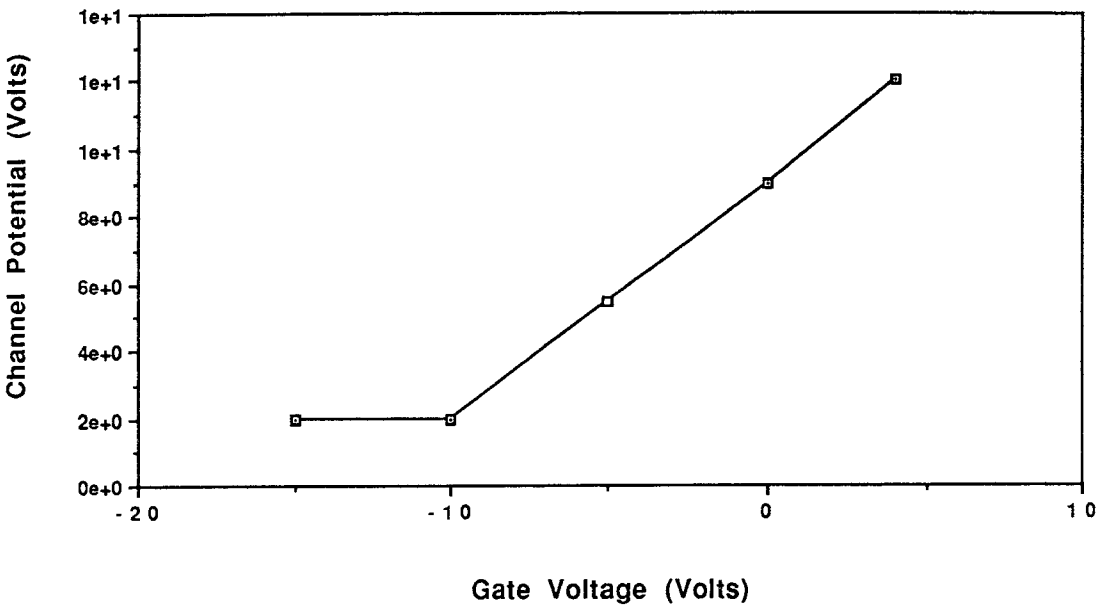

Figure 5.20: Potential profile as a function of gate voltage (Case2)

The electric field is constant in the oxide region since the charge distribution in the oxide is assumed to be zero. And it is a maximum at the interface of Si-SiO_2. Figure 5.21 depicts the electric field with empty well, partially filled and full well conditions. The maximum electric field in Fig. 5.21 is $6.8*10^5$V/cm in oxide and $1.4*10^5$V/cm in silicon.

5.4 Simulation of Graded BCCD with triple implants

Inspection of the curve in Fig. 5.13 shows a peak at the signal level that fills the 4-μm trench. In order to eliminate the peak a third middle size channel implant (8μm) was added to the GBCCD. This study was made with a constraint that anneal times for the 16-μm and 4-μm implant were kept the same as in the standard process of the David Sarnoff Research Center for

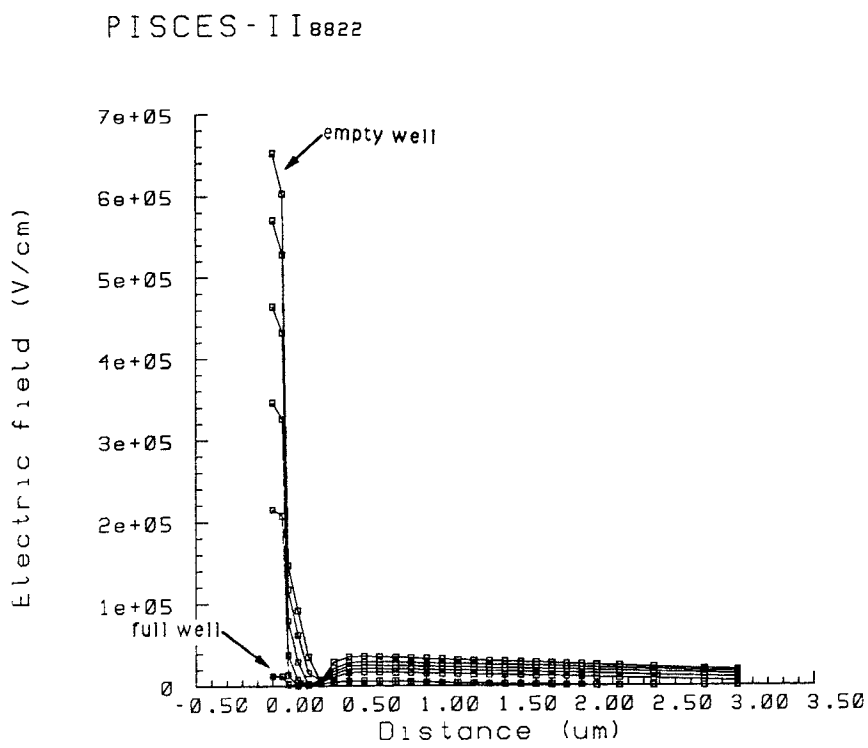

Figure 5.21: Electric Field distribution as function of channel depth and signal level (Case2)

IR-CCDs with PtSi Schottky-barrier detectors. However, the mask level of the additional implant with 8-μm-wide channel in the serial output register could be made at the beginning of the process and would allow an unlimited drive-in (anneal) and the dopant can be either arsenic or phosphorus. More than 20 different cases have been simulated to determine the optimum choice of implants. But only 5 case are reported in the following sections.

5.4.1 Case 1 – 8(P:0.5e12,150) 16(P:1.3e12,150) 4(P:0.5e12,150)

The parameters of the implant dose and energy for the three channel implants for this case are shown in Table 5.4. In this case all three channel implants use phosphorus as dopant. Table 5.5 gives number of electrons and the corresponding area they occupy.

The curve of area per electron versus the number of electrons for this case is

Mask level	Implant width μm	Implant dosage $x10^{12} cm^{-2}$	Implant energy Kev	Dopant
1	8	0.5	150	Phos
2	16	1.3	150	Phos
3	4	0.5	150	Phos

Table 5.4: The process parameters of triple implants (Case1)

plotted in Fig. 5.22. The curve for the double implant (Using As for the 4μm implant) is plotted again in Fig. 5.22 for comparison. Inspection of the two curves in Fig. 5.22 shows that the peak which appeared in double implants case did not appear in this triple implant case. i.e. the transfer efficiency is further improved.

5.4.2 Case 2 – 8(As:0.5e12,180) 16(P:1.3e12,150) 4(As:0.5e12,180)

The parameters of the implant dose and energy for the three channel implants of this case are shown in Table 5.6. In this case phosphorus is used as dopant for the 16μm channel implant. And arsenic instead of phosphorus is used as dopant for the 8μm and 4μm channel implants. Table 5.7 gives number of signal charges and the corresponding area they occupy for this case. The curve of area per electron versus the number of electrons for this case is plotted

Number of electrons	Occupied area (μm^2)
0 0	0 0
2280	1 2
7010	1 6
12769	2 0
19934	2 8
29372	3 5
29947	4 0
52045	6 5
69006	7.0
88730	7 5
110281	7 6
132792	7 8
156069	8 5

Table 5.5: Graded BCCD with triple implants (Case1)

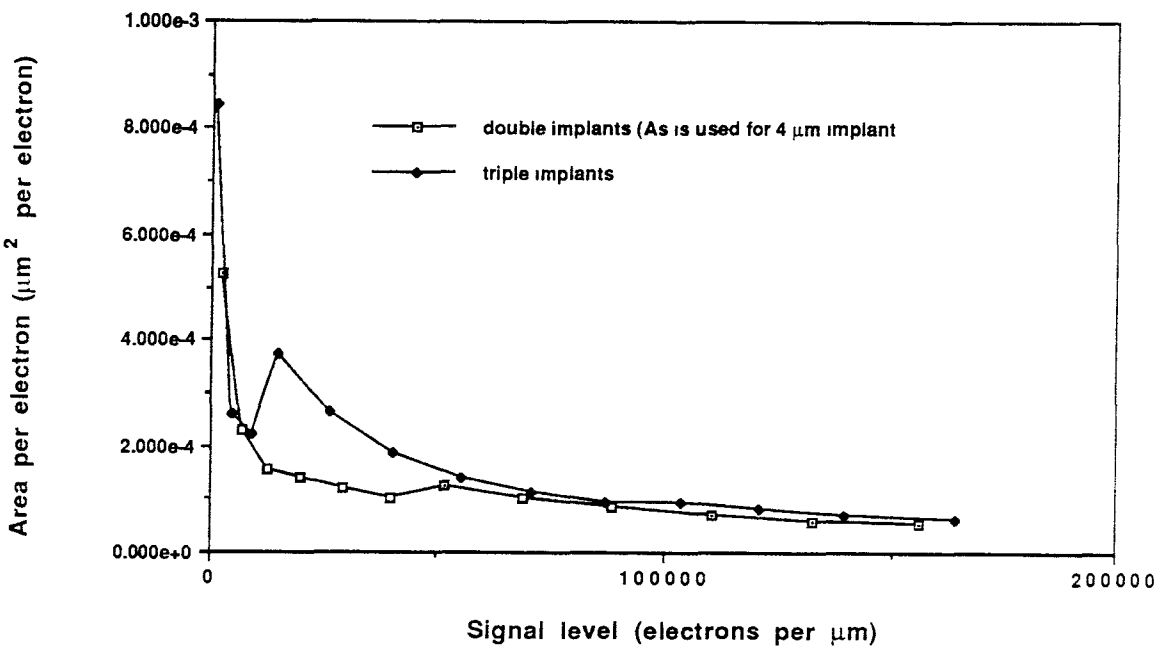

Figure 5.22: Area per electron as a function of the signal level (Case1)

Mask level	Implant width μm	Implant dosage $x10^{12} cm^{-2}$	Implant energy Kev	Dopant
1	8	0.5	180	As
2	16	1.3	150	Phos
3	4	0.5	180	Phos

Table 5.6: The process parameters of triple implants (Case2)

in Fig. 5.23. The curve for the Case 1 (Using Phosphorus for all the three implants) is plotted again in Fig. 5.6 for comparison. Inspection of the two curves in Fig. 5.6 indicates that there is no significant difference between these two cases.

5.4.3 Case 3 – 8(As:0.5e12,180) 16(P:1e12,150 + As:0.5e12,180) 4(As:0.5e12,180)

As shown in Table 5.8, the only difference between this case and the Case2 is that the combination of phosphorus and arsenic is used as dopant impurities for the 16μm channel implant. The 16μm buried channel is obtained by implanting both phosphorous ion(dose=1.0e12, energy=150Kev) and arsenic ion(dose=0.5e12, energy=180Kev). Table 5.9 gives the number of electrons and the corresponding area they occupy. The curve of area per electron versus the signal level in this case is plotted in Fig. 5.24. The curve for the Case

Number of electrons	Occupied area (μm^2)
0.0	0 0
2976	1 6
12154	2 0
20588	2 8
31458	3 2
44120	4 8
61593	5 6
81679	7 5
103259	7 6
125602	7 7
149067	8 0
179730	9 6

Table 5.7: Graded BCCD with triple implants (Case2)

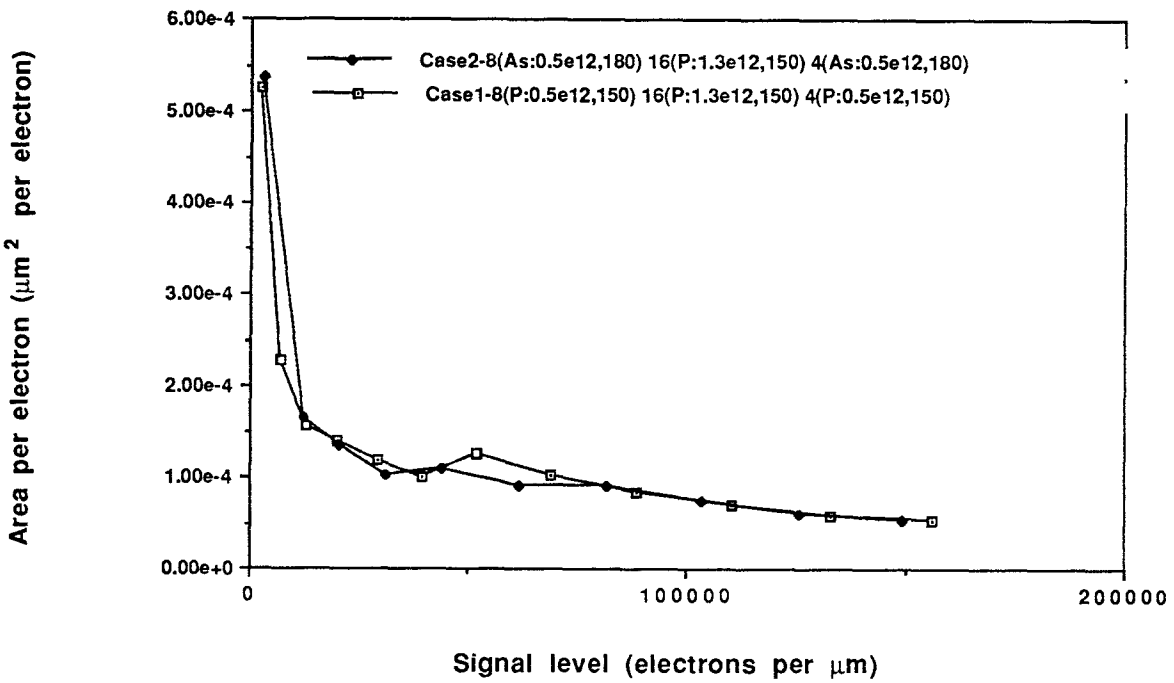

Figure 5.23: Area per electron as a function of the signal level (Case2)

Mask level	Implant width μm	Implant dosage $x10^{12}cm^{-2}$	Implant energy Kev	Dopant
1	8	0.5	180	As
2.1	16	0.5	180	As
2.2	16	1.0	150	Phos
3	4	0.5	180	As

Table 5.8: The process parameters of triple implants (Case3)

2 is plotted again in Fig. 5.6 for comparison. A comparison of the two curves in Fig. 5.24 indicates that Case 3 is better for a low signal level.

5.4.4 Case 4 – 8(P:0.5e12,150) 16(P:0.5e12,150 + As:1e12,180) 4(As:0.5e12,180)

The parameters of the implant dose and energy for the three channel implants for this case are shown in Table 5.10. The difference between this case and Case 3 is that the 8μm buried channel is obtained by implanting phosphorus instead of arsenic. Also the implant doses of phosphorus and arsenic for the 16μm buried channel are different. Table 5.11 gives the number of electrons and the corresponding area they occupy. The curve of area per electron versus the number of electrons is plotted in Fig. 5.25. The curve for Case 3 is also plotted in Fig. 5.6 for comparison. Comparison of the two curves in Fig. 5.25 shows that Case 4 is better than the Case 3.

Number of electrons	Occupied area (μm^2)
0.0	0 0
4515.5	1 2
10519	1 6
18451	2 8
29191	3 2
41382	4 0
57572	5 6
77300	5 8
98722	6 0
121413	7 5
144352	7 7
170003	8 0

Table 5.9: Graded BCCD with triple implants (Case3)

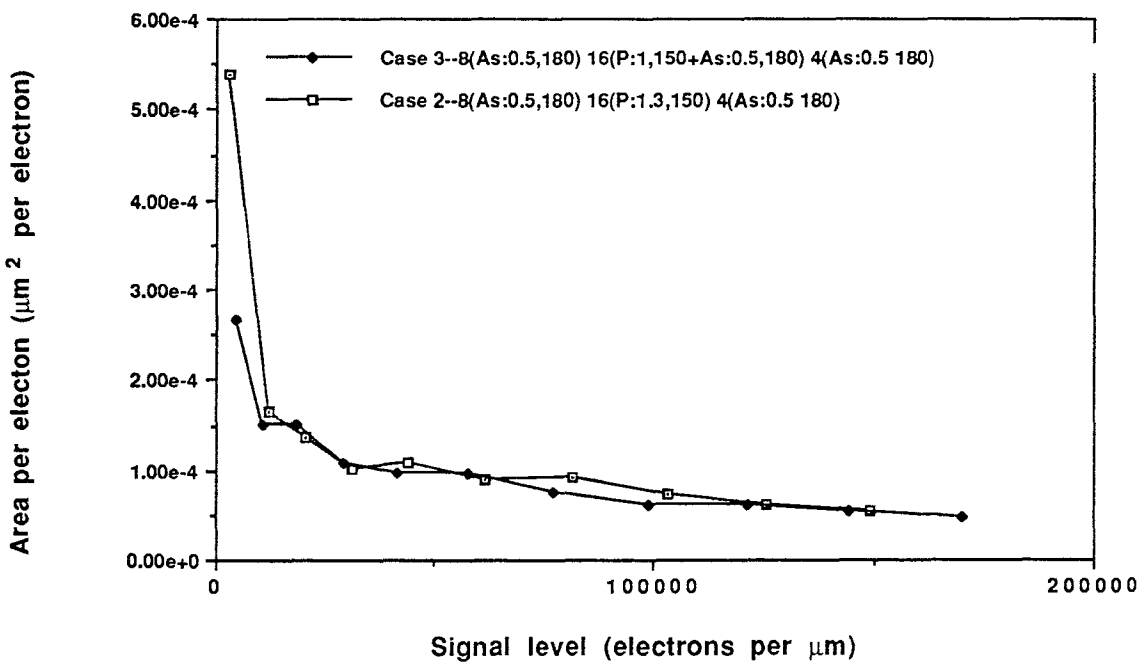

Figure 5.24: Area per electron as a function of the signal level (Case3)

Mask level	Implant width μm	Implant dosage $x10^{12} cm^{-2}$	Implant energy Kev	Dopant
1	8	0.5	150	Phos
2.1	16	1.0	180	As
2.2	16	0.5	150	Phos
3	4	0.5	180	As

Table 5.10: The process parameters of triple implants (Case4)

Number of electrons	Occupied area (μm^2)
0.0	0 0
2788	1 2
7786	1 6
14397	2 4
23347	2 8
34102	3 2
46206	4 4
62132	5 6
81802	7 0
103267	7 5
126069	7 6
149003	7 7
172546	8 0

Table 5.11: Graded BCCD with triple implants (Case4)

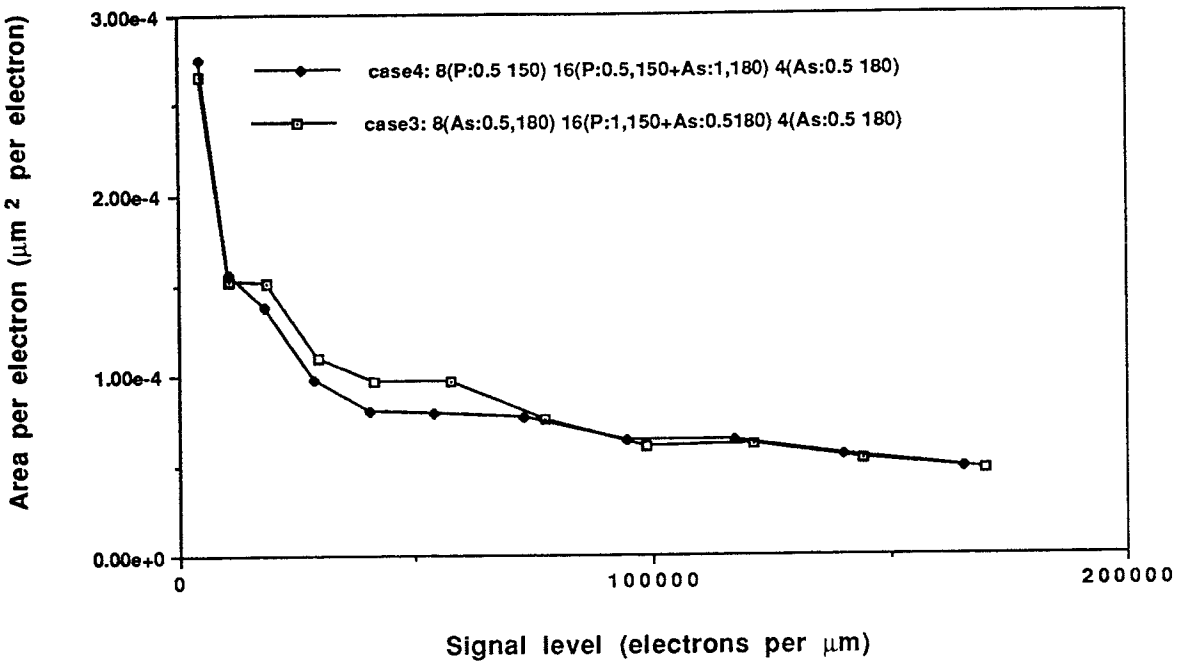

Figure 5.25: Area per electron as a function of the signal level (Case4)

5.4.5 Case 5 – 8(P:0.5e12,180) 16(P:1e12,150 + As:0.5e12,180) 4(As:0.5e12,180)

The parameters of the implant dose and energy for the three channel implants for this case are shown in Table 5.12. This case is the same as Case 4 except that the implant doses of phosphorus and arsenic for the 16μm buried channel are different. Table 5.13 gives the number of electrons and the corresponding area they occupy for this case. The curve of area per electron versus the number of electrons for this case is plotted in Fig. 5.26. The curve for the Case 4 is also plotted in Fig. 5.26 for comparison. Inspection of the two curves in Fig. 5.26 indicates that Case 4 is still better than Case 5.

Mask level	Implant width μm	Implant dosage $x10^{12} cm^{-2}$	Implant energy Kev	Dopant
1	8	0.5	150	Phos
2.1	16	0.5	180	As
2.2	16	1.0	150	Phos
3	4	0.5	180	As

Table 5.12: The process parameters of triple implants (Case5)

Number of electrons	Occupied area (μm^2)
0 0	0 0
4374	1 2
10319	1 6
18044	2 5
28521	2 8
40230	3 2
53735	4 2
72997	5 6
9466	6 0
117316	7 5
140072	7 7
165797	8 0

Table 5.13: Graded BCCD with triple implants (Case5)

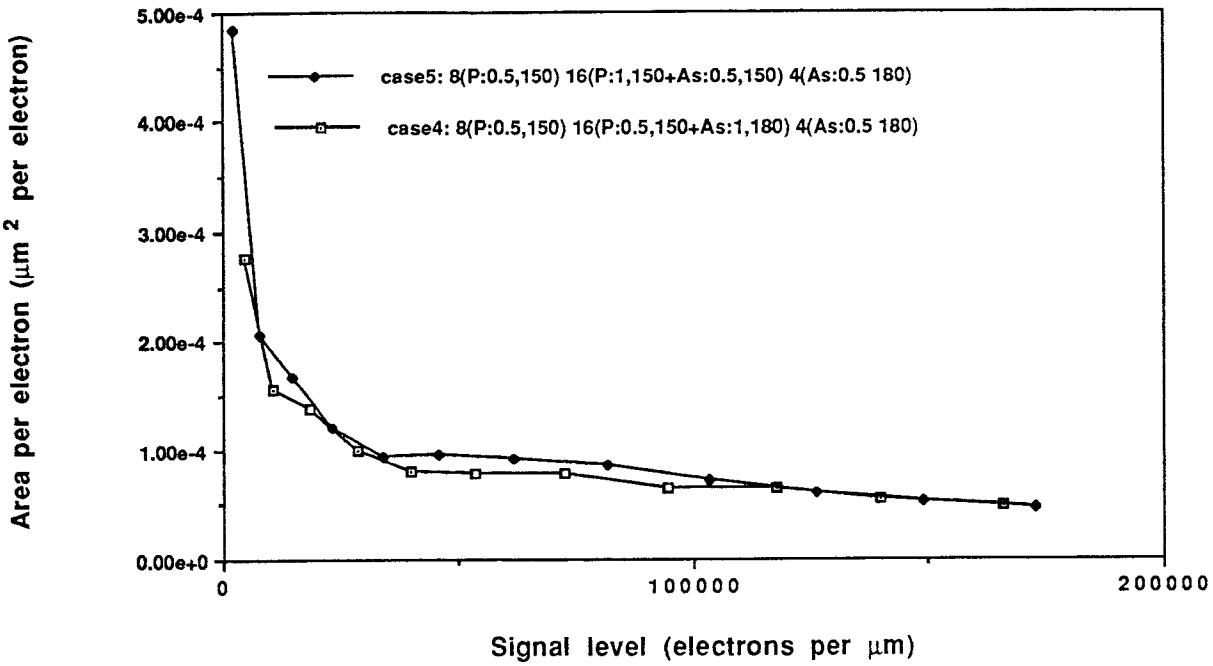

Figure 5.26: Area per electron as a function of the signal level (Case5)

5.4.6 The electrical characteristics of GBCCD with triple implants

Comparing the results of each case discussed above we found the Case 4 is the best. Figure 5.27 shows the plot of charge packet area as function of increasing the signal level for Case4.

Next we will check the electrical characteristics of GBCCD with triple implants of Case 4.

Potential Profile

The 1-D potential profile across the middle section from the surface to the backside for different bias voltages is shown in Fig. 5.28. The 1-D potential profile along the buried channel (0.3 μm) away from surface for different bias voltages is shown in Fig. 5.29.

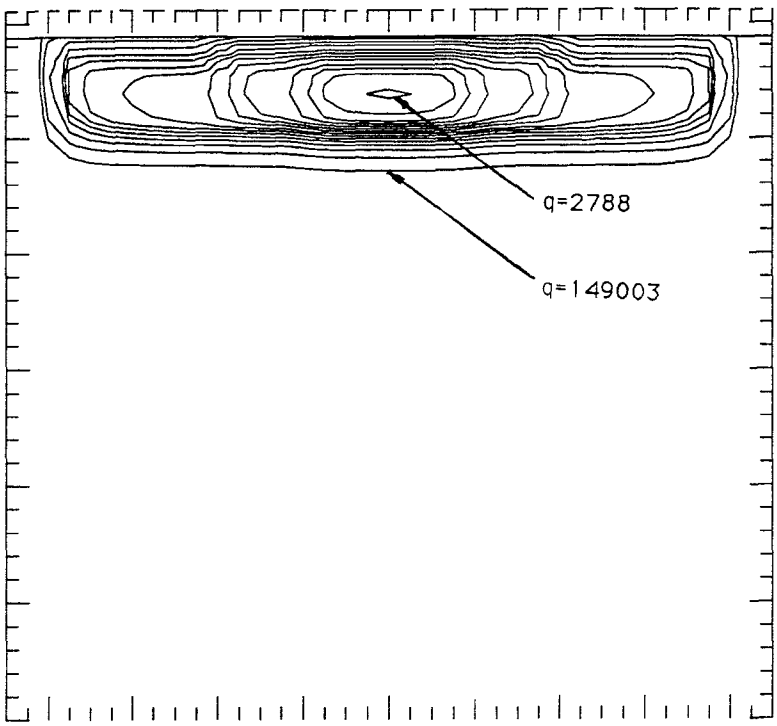

Figure 5.27: Charge pocket area for increasing signal level (Case 4)

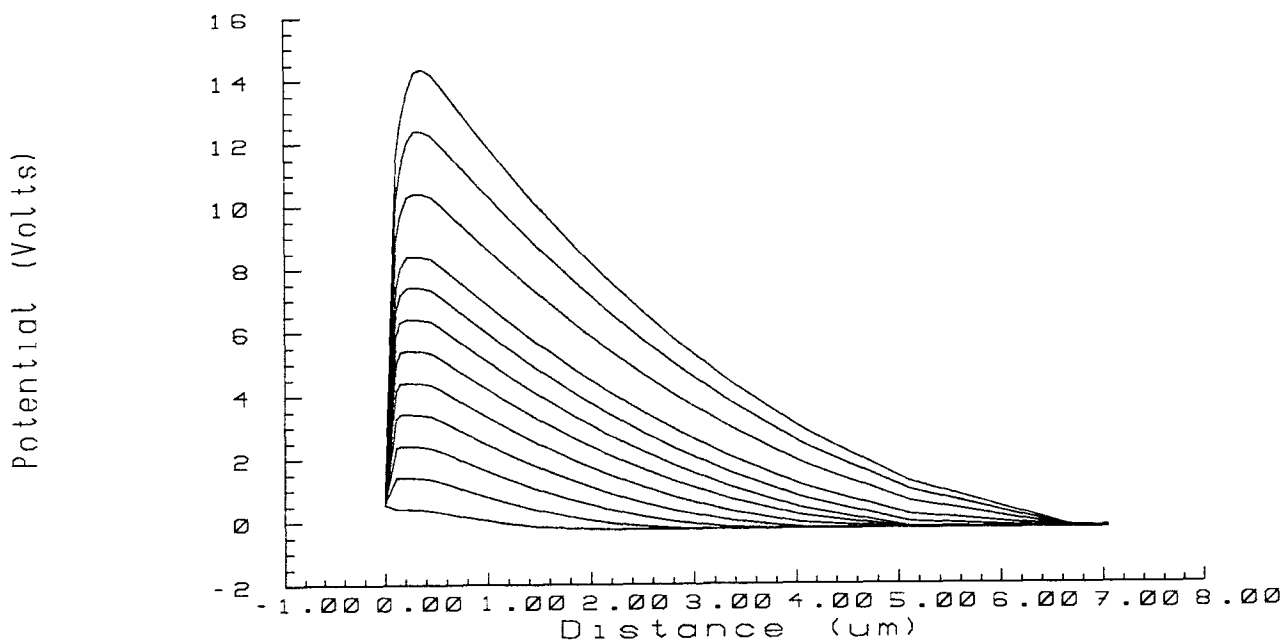

Figure 5.28: Potential profile of the GBCCD vertical to the buried channel corresponding to the empty well, partially filled well and full well (Case4)

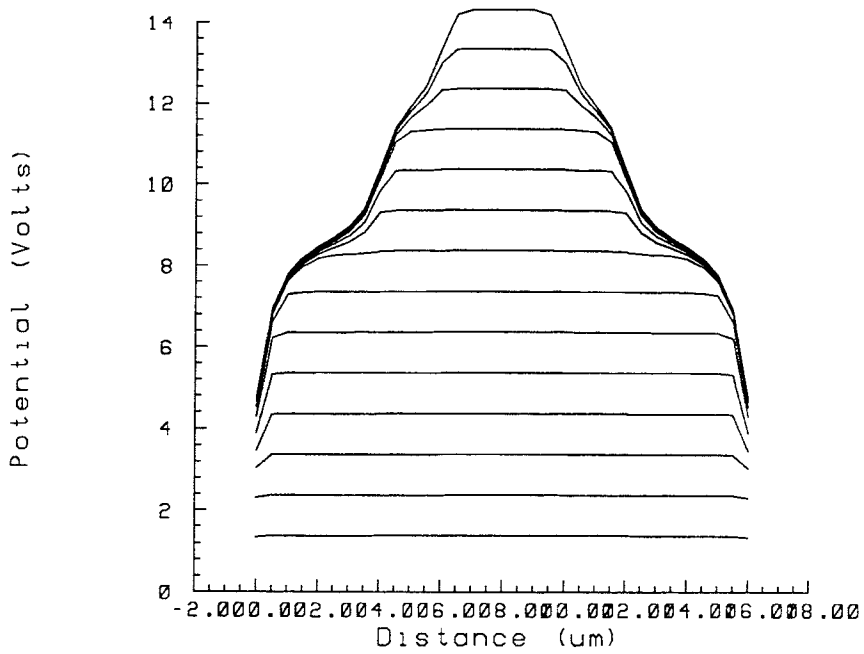

Figure 5.29: Potential profile of the GBCCD along to the buried channel corresponding to the empty well, partially filled well and full well (Case4)

Figures 5.30, 5.31 and 5.32 show the 3-D bird's view of the potential profiles with empty well, a small signal packet and a large signal packet respectively.

A plot of maximum potentials for the empty well as a function of gate voltage is shown in Fig. 5.33. In this case the pinning voltage V_{pin} is found to be about -12V.

Electric Field

Figure 5.34 shows the calculated electric field with empty well, partially filled and full well conditions. The maximum electric field is $8*10^5$V/cm in oxide and $2*10^5$V/cm in silicon.

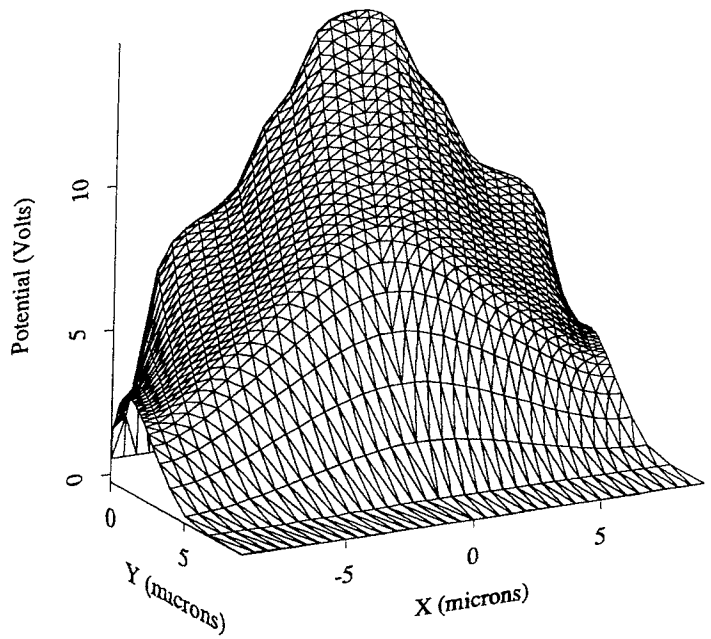

Figure 5.30: Potential profile of the GBCCD with empty well (Case4)

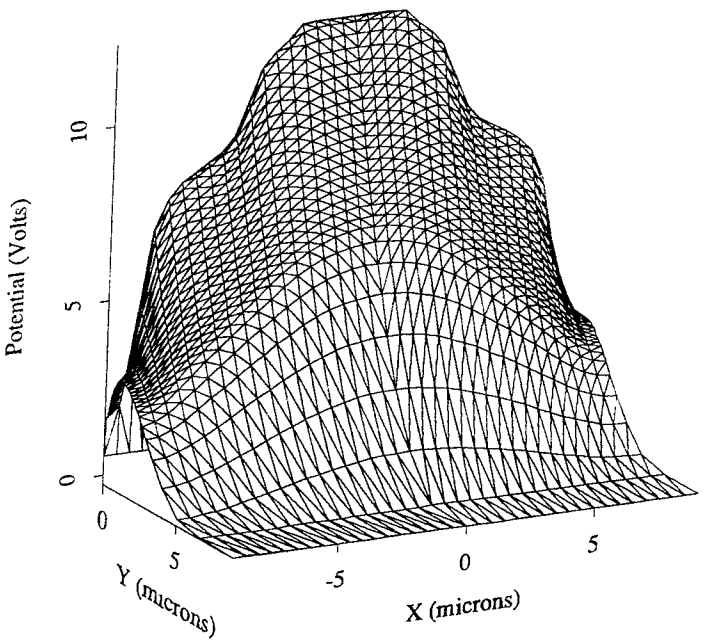

Figure 5.31: Potential profile of the GBCCD with small signal packet (Case4)

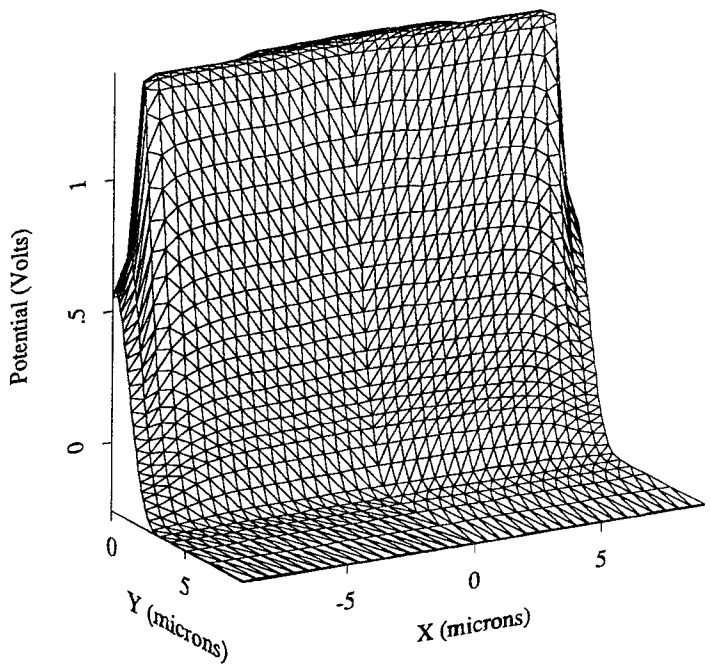

Figure 5.32: Potential profile of the GBCCD with large signal packet (Case4)

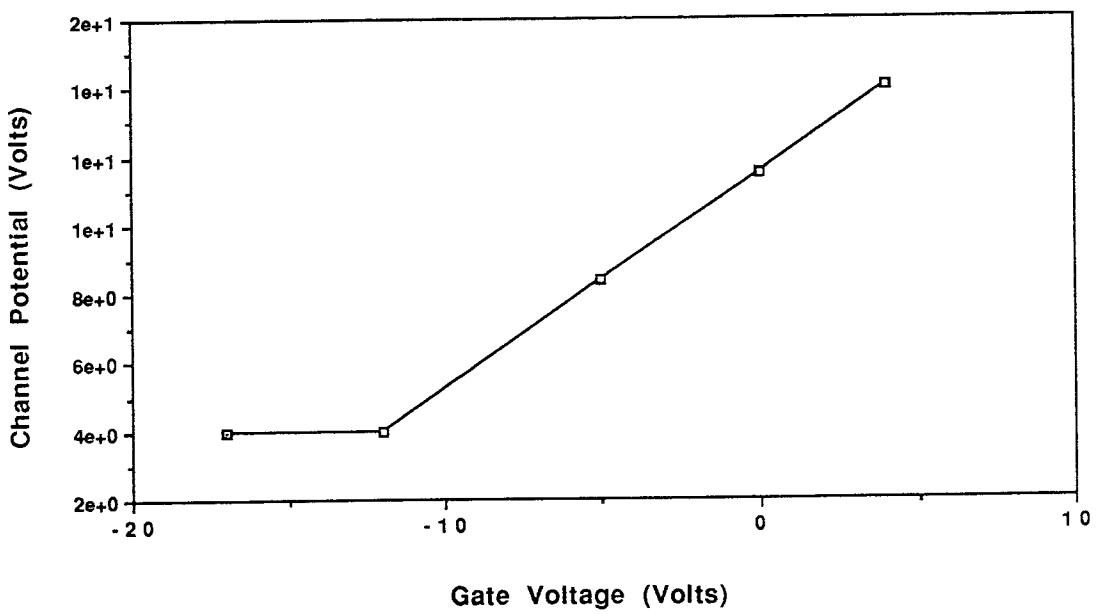

Figure 5.33: Potential profile as a function of gate voltage (Case4)

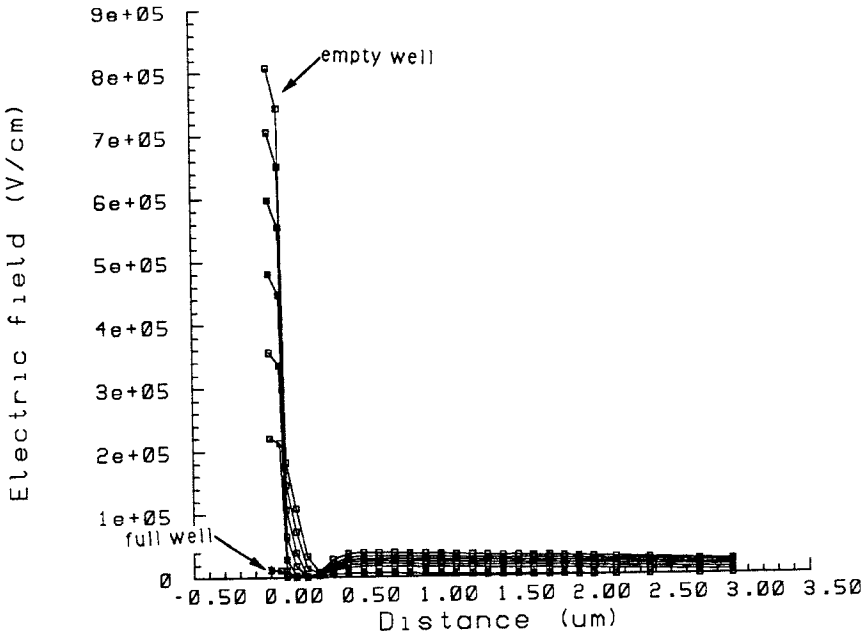

Figure 5.34: Electric Field distribution as function of channel depth and signal level (Case4)

5.4.7 Optimum case for GBCCD with triple implants

In order to achieve the optimum result, other cases have been explored assuming that the implant dose and energy for the buried channel can be adjusted freely. We found that the distribution area of the signal charges has a linear relationship with the number of electrons if the implant parameters shown in Table 5.14. is adopted. The value of the area per electron is very small and almost constant.

Table 5.15 gives the number of electrons and the corresponding area they occupy in this case.

Figure 5.35 shows the curve of charge packet area versus the number of electrons based on the data of Table 5.1 and the corresponding curves for single, double and triple(Case4) implants are also shown in Fig. 5.35. The curve of

Mask level	Implant width μm	Implant dosage $x10^{12} cm^{-2}$	Implant energy Kev	Dopant
1	8	1.0	100	Phos
2	16	1.0	100	Phos
3	4	0.7	30	Phos

Table 5.14: The process parameters of triple implants (optimum case)

the area per electron versus the number of electrons for this case is plotted in Fig. 5.36. The curves for the single and double implants cases are also plotted in Fig. 5.36.

Number of electrons	Occupied area (μm^2)
0 0	0 0
5024	0 94
10899	1 26
18073	1 57
26851	1 88
37600	2 4
49270	2 8
61285	3 2
74388	4 2
89003	5 6
109839	6 0
134011	7 5
167177	8 0

Table 5.15: Graded BCCD with triple implants (optimum case)

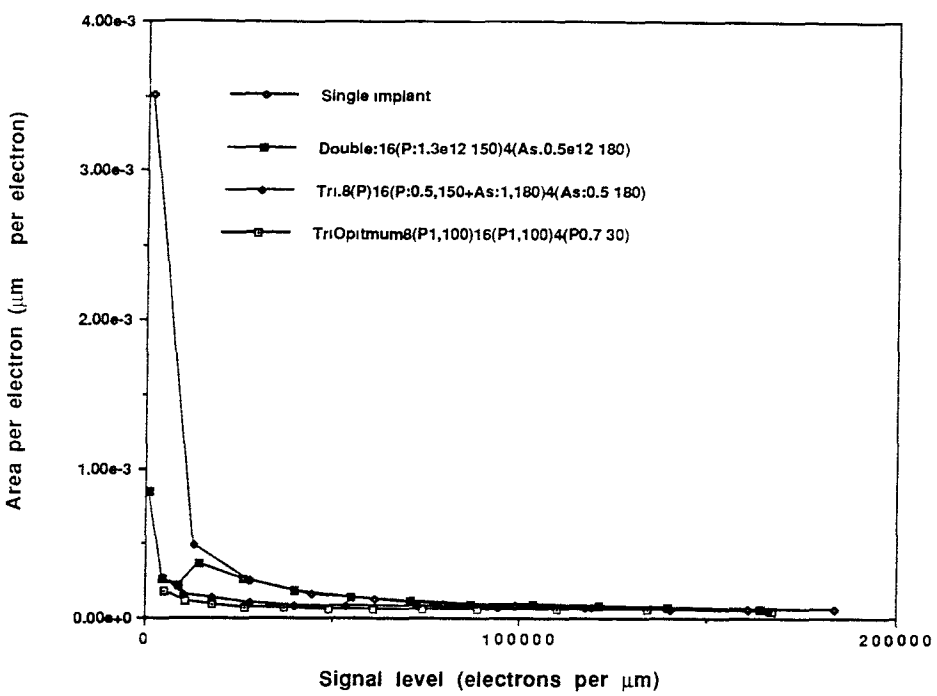

Figure 5.35: Distribution area as a function of the signal level

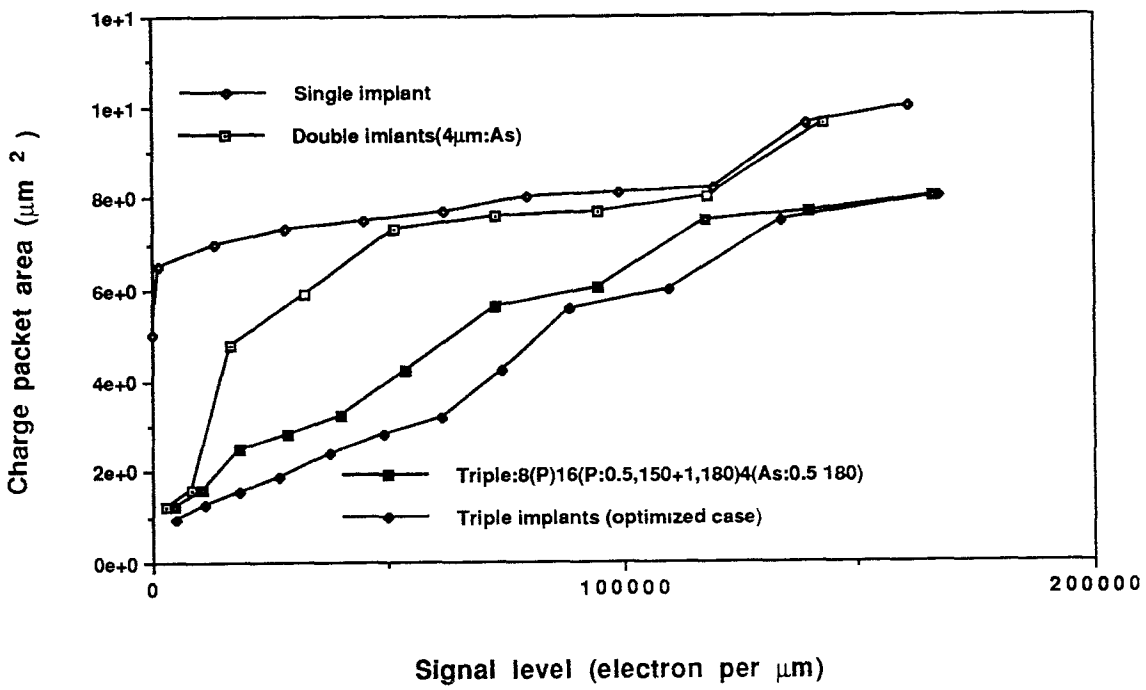

Figure 5.36: Area per electron as a function of the signal level

Chapter 6

Conclusion

A study of GBCCD process and device modeling is performed by using of SUPREM4 and PISCES2. Multiple implantation technique has been used. It was found that additional trench implants in the BCCD improve transfer efficiency of the BCCD.

• The 2-D process and device simulation software, SUPREM4 and PISCES2, were extensively used and debugged on the Sparc 2 Sun workstation. The powerful functions of these CAD tools are demonstrated. And a complete knowledge of these tools also has been obtained.

• A normal BCCD with 16-μm-wide buried channel, by implanting phosphorous ions(dose=2.0e12cm^{-2}, energy=180Kev) in a boron substrate of doping 3e14cm^{-2}, was simulated. The analysis of the results showed that the value of area per electron for small signal level is around $3.5 \times 10^{-3}\mu$m^2/per electron which is almost 1 order of magnitude higher than the value for high signal level of about $4 \times 10^{-4}\mu$m^2/per electron.

• The first simulations for the Graded BCCD (GBCCD) were done with double implants. In this case the graded buried channel was obtained by adding an additional 4-μm-wide implant to the normal 16-μm-wide BCCD. The simulation results show that the area per electron in this case is about 5 times

smaller than the value in the normal BCCD case when signal level is low. This indicates that the transfer efficiency would be improved be a factor of 5.

• Further simulations of the GBCCDs were done with triple implants which were obtained by adding another 8-μm-wide implant to the GBCCDs with double implants. Five cases with different process parameters (but still satisfying the limitation of the processing steps used in Sarnoff Research Center) were studied. The comparison the simulation results indicates that the optimized case (Case 4) is constructed of phosphorous(dose=0.5e12, energy=150) for 8-μm-wide implant, both arsenic(dose=1e12, energy=180) and phosphorous(dose=0.5e12, energy=150) for the 16-μm-wide implant, and arsenic(dose=0.5e12, energy=180) for the 4-μm-wide implant. The simulation results for this case showed that for low signal level the area per electron is about 10 times smaller than the value in the normal BCCD case, i.e. the transfer efficiency is improved be 10 times.

• An optimized channel structure was also found without the restriction imposed on the Sarnoff process. In this case, phosphorus(dose=1.0e12, energy=100) is used for 8-μm-wide implant, phosphorus(dose=1.0e12, energy=100) is used for 16-μm-wide implant, and phosphorus(dose=0.7e12, energy=30) is used for 4-μm-wide implant. The simulation results showed that in this case the area per electron value is almost constant and independent of the signal level.

APPENDIX A

Sarnoff Processing Data

The physical processing steps and procedures are

INITIALIZE < 100 > SILICON BORON Concentration=3E14

DIFFUSION Temperature=800 Time=38 WetO2 HCl

IMPLANT Phosphorus Energy=150 Dose=1.3e12

DIFFUSION Temperature=0900 Time=040

DIFFUSION Temperature=550 Time=120 Nitrogen

DIFFUSION Temperature=550 Time=90 T.Rate=5 Nitrogen

DIFFUSION Temperature=1000 Time=15 Nitrogen

DIFFUSION Temperature=1000 Time=66 T.Rate=-3 Nitrogen

ETCH Oxide all

DIFFUSION Temperature=800 Time=20 T.Rate=5 Nitrogen

DIFFUSION Temperature=900 Time=47 WetO2 HCl

DIFFUSION Temperature=900 Time=10 Nitrogen

DIFFUSION Temperature=900 Time=33 T.Rate=-3 Nitrogen

DEPOSIT Polysilicon Temperature=560 Thickness=0.6

DIFFUSION Temperature=800 Time=30 T.Rate=5 Nitrogen

DIFFUSION Temperature=950 Time=5 Nitrogen

DIFFUSION Temperature=950 Time=15 Nitrogen + Phosphorus Solidsolubility

DIFFUSION Temperature=950 Time=10 Nitrogen

DIFFUSION Temperature=950 Time=30 T.Rate=-5 Nitrogen

ETCH Polysilicon all

DIFFUSION Temperature=800 Time=20 T.Rate=5 Nitrogen

DIFFUSION Temperature=900 Time=31 WetO2 HCl

DIFFUSION Temperature=900 Time=10 Nitrogen

DIFFUSION Temperature=900 Time=33 T.Rate=-3 Nitrogen

DEPOSIT Polysilicon Temperature=560 Thickness=0.6

DIFFUSION Temperature=800 Time=30 T.Rate=5 Nitrogen

DIFFUSION Temperature=950 Time=15 Nitrogen + Phosphorus Solidsolubility

DIFFUSION Temperature=950 Time=10 Nitrogen

DIFFUSION Temperature=950 Time=30 T.Rate=-5 Nitrogen

DIFFUSION Temperature=800 Time=20 T.Rate=5 Nitrogen

DIFFUSION Temperature=900 Time=10 WetO2 HCl

DIFFUSION Temperature=900 Time=10 Nitrogen

DIFFUSION Temperature=900 Time=33 T.Rate=-3 Nitrogen

DIFFUSION Temperature=800 Time=15 Nitrogen

DIFFUSION Temperature=800 Time=10 WetO2 HCl

DIFFUSION Temperature=800 Time=10 Nitrogen

DIFFUSION Temperature=800 Time=40 T.Rate=5 Nitrogen

DIFFUSION Temperature=1000 Time=30 Nitrogen

DIFFUSION Temperature=1000 Time=67 T.Rate=-3 Nitrogen

DIFFUSION Temperature=800 Time=30 T.Rate=5 Nitrogen

DIFFUSION Temperature=950 Time=15 Nitrogen

DIFFUSION Temperature=950 Time=50 T.Rate=-3 Nitrogen

DIFFUSION Temperature=800 Time=30 T.Rate=5 Nitrogen

DIFFUSION Temperature=950 Time=15 Nitrogen

DIFFUSION Temperature=950 Time=50 T.Rate=-3 Nitrogen

APPENDIX B

2-D Process Simulation Programs

The SUPREM4 process simulation program for BCCD with triple implants is shown next:

```
set echo
option quiet
line x loc=0.0 tag=left spacing=0.5
line x loc=9 tag=right spacing=0.5
line y loc=0.0 tag=top spacing=0.05
line y loc=0.5 spacing=0.1
line y loc=2 spacing=0.1
line y loc=9.0 tag=bot
region silicon xlo=left xhi=right ylo=top yhi=bot
bound exposed xlo=left xhi=right ylo=top yhi=top
bound backside xlo=left xhi=right ylo=bot yhi=bot
init boron conc=3.0e14 ori=100
#deposit the gate oxide
oxide hcl.pc=2
diffuse time=38 temp=800 wet
#do the phosphorus implant
deposit photores thick=2.0
```

```
etch photores left p1.x=4.0 p2.x=4.0
implant phos dose=7.0e11 energy=120.0 pearson
etch photores all
implant phos dose=1.0e11 energy=100.0 pearson
deposit photores thick=2.0
etch photores left p1.x=2.0 p2.x=2.0
implant phos dose=1.3e12 energy=150.0 pearson
etch photores all
struct out=1.str
set echo
option quiet
init inf=1.str
diffuse time=15 temp=1000 nit
struct outf=2.str
foreach val(0 to 65 step 1)
diffuse time=1 temp=1000-val*3 nit
end
struct outf=3.str
etch oxide all
struct outf=4.str
foreach val(0 to 19 step 1)
diffuse time=1 temp=800+val*5 nit
end
struct outf=5.str
oxide hcl.pc=2
diffuse temp=900 time=47 wet
```

```
struct outf=6.str
set echo
opt quiet
init inf=6.str
diffuse time=10 temp=1000 nit
struct outf=7.str
foreach val(0 to 32 step 1)
diffuse time=1 temp=900-val*3 nit
end
struct outf=8.str
deposit poly thick=0.600 div=10
struct outf=9.str
foreach val(0 to 29 step 1)
diffuse time=1 temp=800+val*5 nit
end
struct outf=10.str
diffuse time=5 temp=950 nit
struct outf=11.str
diffuse time=15 temp=950 phos gas.con=3.1585e20
struct outf=12.str
diffuse time=10 temp=950 nit
struct outf=13.str
foreach val(0 to 29 step 1)
diffuse time=1 temp=950-val*5 nit
end
struct outf=14.str
```

```
etch poly all
struct outf=15.str
foreach val(0 to 19 step 1)
diffuse time=1 temp=800+val*5 nit
end
struct outf=16.str
oxide hcl.pc=2
diffuse temp=900 time=31 wet
struct outf=17.str
set echo
opt quiet
init inf=17.str
diffuse time=10 temp=900 nit
struct outf=18.str
foreach val(0 to 32 step 1)
diffuse time=1 temp=900-val*3 nit
end
struct outf=19.str
deposit poly thick=0.600 div=10
etch poly right p1.x=7.0 p2.x=7.0
struct outf=20.str
init inf=20.str
foreach val(0 to 29 step 1)
diffuse time=1 temp=800+val*5 nit
end
struct outf=21.str
```

```
diffuse time=15 temp=950 phos gas.con=3.1585e20
struct outf=22.str
diffuse time=10 temp=950 nit
struct outf=23.str
foreach val(0 to 29 step 1)
diffuse time=1 temp=950-val*5 nit
end
struct outf=24.str
foreach val(0 to 19 step 1)
diffuse time=1 temp=800+val*5 nit
end
struct outf=25.str
oxide hcl.pc=2
diffuse temp=900 time=10 wet
struct outf=26.str
set echo
opt quiet
init inf=26.str
diffuse time=10 temp=900 nit
struct outf=27.str
foreach val(0 to 32 step 1)
diffuse time=1 temp=900-val*3 nit
end
struct outf=28.str
diffuse time=15 temp=800 nit
struct outf=29.str
```

```
oxide hcl.pc=2
diffuse temp=800 time=10 wet
struct outf=30.str
set echo
opt quiet
init inf=30.str
diffuse time=10 temp=800 nit
struct outf=31.str
foreach val(0 to 39 step 1)
diffuse time=1 temp=800+val*5 nit
end
struct outf=32.str
diffuse time=30 temp=1000 nit
struct outf=33.str
foreach val(0 to 66 step 1)
diffuse time=1 temp=1000-val*3 nit
end
struct outf=34.str
foreach val(0 to 29 step 1)
diffuse time=1 temp=800+val*5 nit
end
struct outf=35.str
set echo
opt quiet
init inf=35.str
diffuse time=15 temp=950 nit
```

```
struct outf=36.str
foreach val(0 to 49 step 1)
diffuse time=1 temp=950-val*3 nit
end
struct outf=37.str
foreach val(0 to 29 step 1)
diffuse time=1 temp=800+val*5 nit
end
struct outf=38.str
diffuse time=15 temp=950 nit
struct outf=39.str
foreach val(0 to 49 step 1)
diffuse time=1 temp=950-val*3 nit
end
struct outf=40.str
```

The programme to transfer the Suprem4 output into Pisces input formate:

```
init inf=14.str
# remove extra grid nodes to save Pisces compute time
# etch start x=-0.5 y=-0.1
# etch cont x=1.6 y=-0.1
# etch cont x=1.6 y=-1.0
# etch done x=-0.5 y=-1.0
structure mirror left
# save it in Pisces format
struct pisc=ldd.mesh
```

APPENDIX C

2-D Device Simulation Programs

The following PISCES program shows the grid structure and save the initial solution to the data file slv1:

```
opt tek
$opt plotdev=save
$load the mesh and solution files
mesh geom infile=ldd.mesh outf=hmesh3
plot.2d grid bound pause
$regrid doping abs log ign=1 ratio=0.2 smooth=1 outf=hmesh2
contact num=1 n.poly
symb carriers=0
models temp=300 print
solve init outf=slv1
$regrid poten ratio=0.2 outf=hmesh3
$plot.2d grid bound
end
```

The next program plots the dopping profiles:

```
title plot 1-d cross-sectional dopping profile
$option plotdev=lw plotfile=plot.ps
opt tek
```

```
opt term=save
$load the mesh and solution files
mesh infile=hmesh3
load infile=slv1
plot.1d doping abs log min=15 max=17
+ x.s=0.0 y.s=0.0 x.e=0.0 y.e=1 pause
plot.1d doping abs log min=15 max=17
+ x.s=2.0 y.s=0.0 x.e=2.0 y.e=1 pause unch
plot.1d doping abs log min=15 max=17
+ x.s=7.0 y.s=0.0 x.e=7.0 y.e=1 pause unch
plot.1d doping abs min=2e16 max=1.5e17
+ x.s=-7.7 y.s=0.1 x.e=7.7 y.e=0.1 pause
plot.1d doping abs min=2e16 max=1.5e17
+ x.s=-7.7 y.s=0.2 x.e=7.7 y.e=0.2 pause unch
plot.1d doping abs min=2e16 max=1.5e17
+ x.s=-7.7 y.s=0.3 x.e=7.7 y.e=0.3 pause unch
end
```

The next PISCES program shows how the burried channel in BCCD is depleted by slowly changing the N.bias voltage.

```
Title PISCES INPUT DECK
Comment OPTIONS PLOTDEV=psraw
Comment Read in simulation mesh
MESH INFILE=hmesh3
Comment These to override defaults to match LOADFILE.
CONTACT NUM=1 n.POLY
SYMB CARRIERS=0
```

```
METHOD ITLIMIT=60
models temp=300 print
Comment Read in saved solution
LOAD INFILE=slv1
SOLVE V1=0 V2=0 N.BIAS=1 P.BIAS=0 previous OUTF=qf.1
SOLVE V1=0 V2=0 N.BIAS=2 P.BIAS=0 previous OUTF=qf.2
SOLVE V1=0 V2=0 N.BIAS=3 P.BIAS=0 previous OUTF=qf.3
SOLVE V1=0 V2=0 N.BIAS=4 P.BIAS=0 previous OUTF=qf.4
SOLVE V1=0 V2=0 N.BIAS=5 P.BIAS=0 previous OUTF=qf.5
SOLVE V1=0 V2=0 N.BIAS=6 P.BIAS=0 previous OUTF=qf.6
SOLVE V1=0 V2=0 N.BIAS=7 P.BIAS=0 previous OUTF=qf.7
SOLVE V1=0 V2=0 N.BIAS=8 P.BIAS=0 previous OUTF=qf.8
SOLVE V1=0 V2=0 N.BIAS=9 P.BIAS=0 previous OUTF=qf.9
SOLVE V1=0 V2=0 N.BIAS=10 P.BIAS=0 previous OUTF=qf.10
END
```

The PISCES program to plot the potential profiles is shown next:

```
title plot 1-D potential profile
$opt plotdev=lw plotfile=plot.ps x.s=7
opt tek
$opt plotdev=save
$ load the mesh and solution files
mesh infile=hmesh3
interface x.min=0 x.max=5 y.min=-0.05 y.max=6 qf=1e10
+ s.n=1e4 s.p=1e4
contact num=1 n.poly
models temp=300 print
```

```
load infile=qf.14
plot.1d poten a.x=0 b.x=0 a.y=-0.05 b.y=6 pause
load infile=qf.12
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.10
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.8
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.7
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.6
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.5
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.4
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.3
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.2
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=qf.1
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch pause
load infile=slv1
plot.1d poten a.x=0 b.x=0 a.y=0.0 b.y=6 unch
end
```

The PISCES program to plot the electric field profiles is shown next: title plot

2-D contour plot of e.field

$opt plotdev=lw plotfile=plot.ps x.s=7

opt plotdev=save

$ load the mesh and solution files

mesh infile=hmesh3

contact num=1 n.poly

symb carriers=0

method itlimit=60

models temp=300 print

load infile=qf.13

plot.1d e.field a.x=0.0 b.x=0.0 a.y=0.0 b.y=3 points pause

load infile=qf.11

plot.1d e.field a.x=0.0 b.x=0.0 a.y=0.0 b.y=3 points unch pause

load infile=qf.9

plot.1d e.field a.x=0.0 b.x=0.0 a.y=0.0 b.y=3 points unch pause

load infile=qf.7

plot.1d e.field a.x=0.0 b.x=0.0 a.y=0.0 b.y=3 points unch pause

load infile=qf.5

plot.1d e.field a.x=0.0 b.x=0.0 a.y=0.0 b.y=3 points unch pause

load infile=qf.3

plot.1d e.field a.x=0.0 b.x=0.0 a.y=0.0 b.y=3 points unch pause

load infile=slv1

plot.1d e.field a.x=0.0 b.x=0.0 a.y=0.0 b.y=3 points unch pause

$load inf=pin.10

$plot.1d e.field a.x=0.0 b.x=0.0 a.y=0.0 b.y=3 points unch pause

$plot.1d e.field a.x=4.0 b.x=4.0 a.y=8.0 b.y=3 points unch pause

$plot.1d e.field a.x=-4.0 b.x=-4.0 a.y=0.0 b.y=3 points unch pause

plot.2d boundary

contour e.field min=5 max=6 nc=10

vector e.field scale=1.e+5

end

The next program prints out all useful data which are need for calculating the number of electrons in BCCD and the distribution area

title print points and solution (data files)

$opt plotdev=lw plotfile=plot.ps x.s=7

$opt tek

$opt plotdev=save

$ load the mesh and solution files

mesh infile=hmesh3

interface x.min=0 x.max=5 y.min=-0.05 y.max=6 qf=1e10

+ s.n=1e4 s.p=1e4

interface qf=1e10

contact num=1 n.poly

models temp=300 print

symb carriers=0

method itlimit=60

load infile=qf.14

print points

print solution

end

APPENDIX D

Parameter Extract Program

```
      DIMENSION A(1184,7), B(1184,6),C(1184), D(1184),X(1184),Y(1184)


      OPEN(UNIT=1,FILE='DATA')
      DO 100 I=1,1184
      READ(1,*)(A(I,J),J=1,7)
C     WRITE(*,*)(A(I,J),J=1,7)
100   CONTINUE
      DO 200 I=1,1184
      READ(1,*)(B(I,J),J=1,6)
C     WRITE(*,*)(B(I,J),J=1,6)
200   CONTINUE
      CLOSE(1)
      D(1)=A(1,3)
      DO 300 I=2,1184
      D(I)=A(I,3)-A(I-1,3)
      IF (D(I) .LE. 0.0) THEN
      D(I)=A(I,3)
      ENDIF
```

```
C       WRITE(*,*)(I)
C       WRITE(*,*)(D(I))
300     CONTINUE
        S=0
        J=0
        DO 400 I=1,1184
        C(I)=0.5*B(I,3)*D(I)
C       WRITE(*,*)(C(I))
        S=S+C(I)
        IF (B(I,3) .GE. 1E11) THEN
        J=J+1
        X(J)=A(I,2)
        Y(J)=A(I,3)
        ENDIF
400     CONTINUE
        XMIN=0
        XMAX=0
        YMIN=0
        YMAX=0
        DO 500 I=1,J
        IF (XMIN .GT. X(I)) THEN
        XMIN=X(I)
        ENDIF
        IF (XMAX .LT. X(I)) THEN
        XMAX=X(I)
        ENDIF
```

```
      IF (YMIN .GT. Y(I)) THEN
      YMIN=Y(I)
      ENDIF
      IF (YMAX .LT. Y(I)) THEN
      YMAX=Y(I)
      ENDIF
500   CONTINUE
      AREA=(XMAX-XMIN)*(YMAX-YMIN)
      WRITE(*,*)(S*1E-12)
      WRITE(*,*)(AREA)
      WRITE(*,*)(J)
      STOP
      END
```

APPENDIX E

Overview of VLSI CAD Environment in NJIT

It has become generally recognized that the computer is an essential tool for designing VLSI circuits[19]. One of the principal goals behind the design aids is to significantly reduce the time between the initial concept of a complex system and the generation of IC masks. A second equally important goal is to allow the designer to efficiently explore design alternatives. Since design aids can consider a large number of design trade-offs per unit time, it is even conceivable that for complex designs the computer aids could help produce designs superior to those produced manually. A third purpose of computer-aided design system is to assist designers in verifying the correctness of their designs.

At NJIT extensive computing services support both academic study and research in VLSI. The equipment, used by graduate students and faculty, includes 7 Apollo computer workstations running the complete Mentor Integrated Circuit design software and six Sun workstations for semiconductor device simulation. 15 additional Sun workstation using MAGIC software to support integrated circuit layout design. Fig. .1 shows the VLSI CAD tools distribution in NJIT. The following sections will give brief descriptions of these CAD tools.

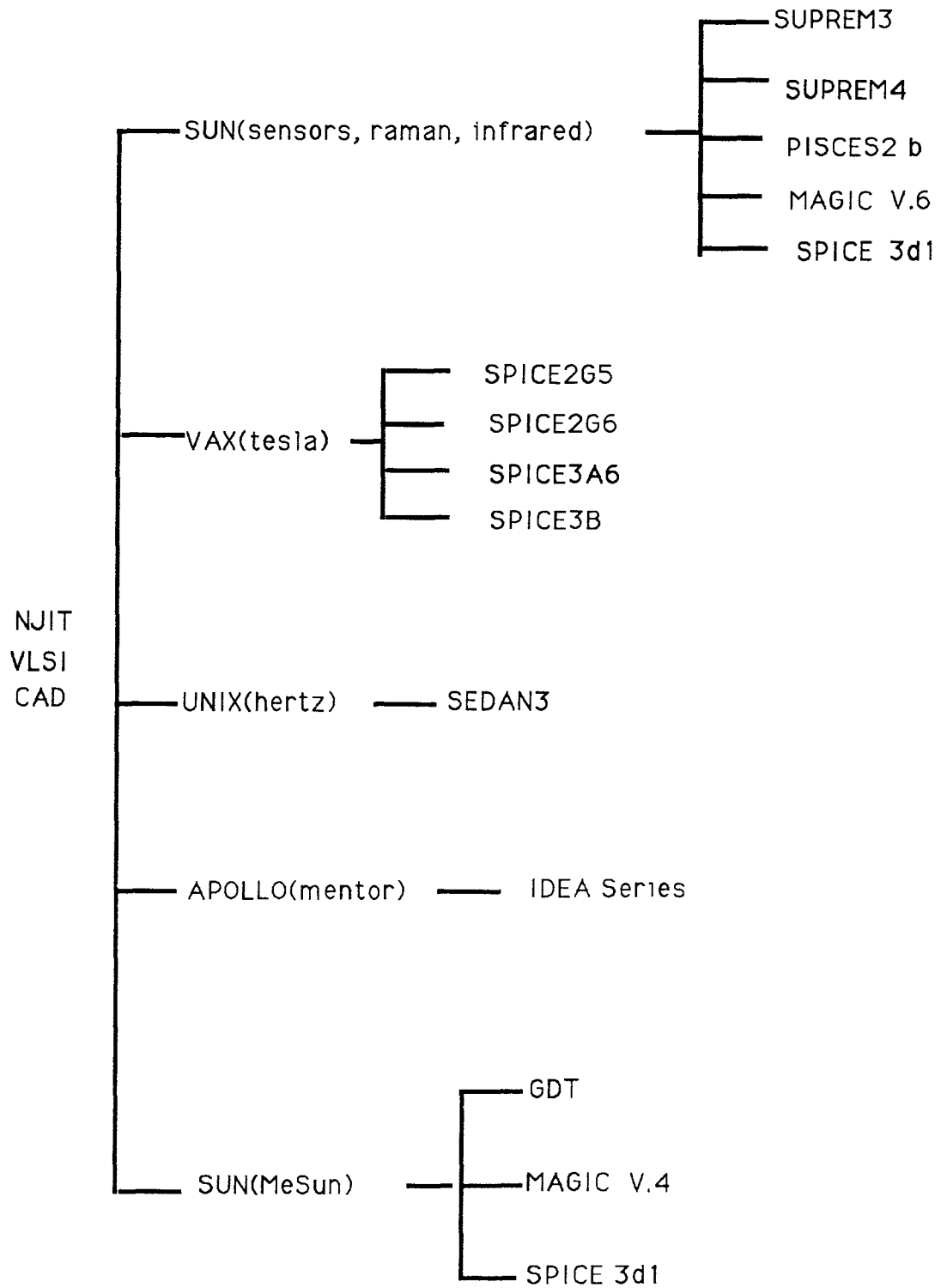

Figure .1: NJIT VLSI CAD ENVIRONMENT

1. SUPREM

Silicon integrate circuit (IC) technology has evolved to fabricate multi- million transistors on a single chip. Trial-and-error methodology to optimize such a complex process is no longer desirable because of the enormous cost and turn-around time. From this point of view, computer simulation is a cost- effective alternative, not only supplying a right answer for increasingly tight processing windows, but also serving as a tool to develop future technologies. Process simulation is the modeling of the process steps involved in wafer fabrication. There are various CAD Tools (e.g. SUPREM3 and SUPREM4) to simulate such effects. When coupled with a device analysis program, a process simulator has proven to be a powerful design tool because the process sensitivity to device parameters can be easily extracted by simple changes made to processing conditions in computer inputs.

SUPREM3 (Stanford University PRocess Engineering Models) was introduced in 1977[20] and was the first program capable of simulating most IC fabrication steps in a one-dimension(1-D). The program accepts a process-runsheet-like input and gives an output containing the impurity distributions in the vertical direction. SUPREM3, therefore, can be applied to any regions where impurity distribution changes only in the vertical direction as indicated in a CMOS cross-section of Fig. .2. The SUPREM3 program consists of various models based on experimental data as well as physical assumptions.

With the trend toward shallow junctions and lower heat cycles in VLSI technologies, two-dimensional impurity profiles and structures are more crucial to device characteristics. Threshold voltage and parasitic capacitance, for example, are strong functions of lateral diffusion of arsenic in the source/drain

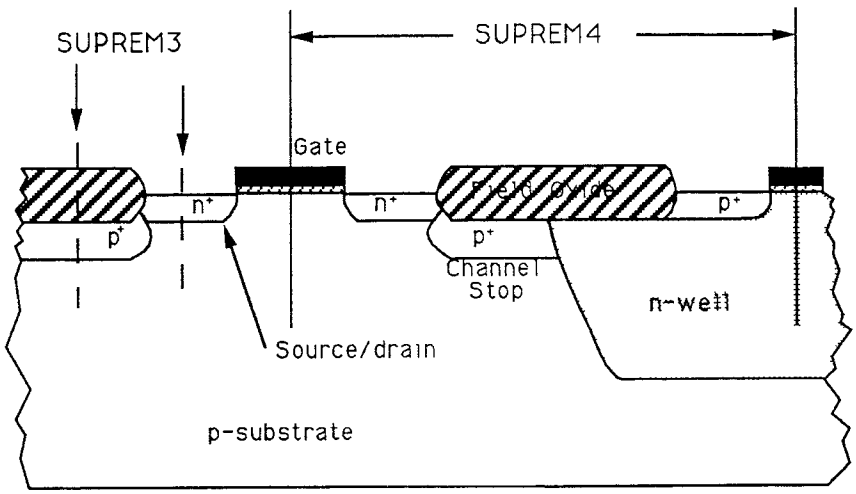

Figure .2: The cross section of a CMOS device

and boron in the channel-stop region. Simple extension of SUPREM3 to two dimensions may not be desirable because the degree of equivalent numerical accuracy requires tremendous computing resources. Furthermore, device structures change continuously during such processes as reactive-ion etching and local oxidation of silicon (LOCOS), which impose more difficulties to establishing simulation algorithms. SUPREM4 introduced in 1988 was one of the pioneer works in the two-dimensional process modeling and it can be applied to the areas where impurity distributions and device structures change not only in the vertical direction but in the lateral direction as indicated in figure .2. It had already been demonstrated that the two-dimensional process simulator could be a powerful design tool when coupled with a device analysis program.

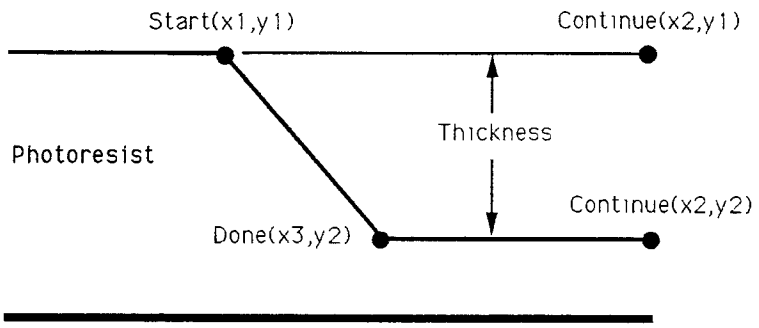

Figure .3: Structure definition in SUPREM4

SUPREM4 simulates the incorporation and redistribution of impurities in a two-dimensional (2-D) cross-section of a device as indicated in figure .2. Such two-dimensional(2-D) cross-section of a device as indicated by modeling actual lithographic patterning. A photoresist layer deposition in figure .3 for example, is formed by an ETCH car. The parameters (START, CONTINUE and DONE) allow the user to specify an arbitrarily complex region to be etched. Several lines can be combined to specify the several points that make up the region.

Input commands and the internal organization of suprem4 are similar to those of PISCES2 and SUPREM3. Here is a brief introduction to the commands and their actions in SUPREM4. These are commands that usually have some action associated with them, as opposed to the models section commands which just set coefficients.

There are several groups of commands in this section. The first are commands which are used for i/o of data. The second are simulation commands of SUPREM IV. The third are commands which are primarily for the post processing. The remainder are bunched in the aptly named miscellaneous category.

Data Input and Output Commands

boundary This command allows the user to specify lines which are exposed to gas in a rectangular grid.

initialization This command allows the user to set up the initial grid and specify background concentrations.

line This command allows the user to position x and y grid lines for a rectangular mesh.

profile This command allows the user to read in ascii data file of depth and doping data.

region The region command allows the user to specify which sections of the rectangular mesh are which material.

structure The structure command allows the user to read and write mesh and solution values. This is the main i/o of data to and from the program.

Simulation Commands

etch This command allows the user to etch layers.

deposit This command allows the user to deposit layers.

diffuse This command allows the user to specify a time temperature step.

implant This command allows the user to model an implant with either a gaussian or a pearsonIV distribution.

method This command allows the user to pick the numerical options for solving the equations.

stress This command computes the thermal elastic stresses.

Post Processing Commands

color This command is similar to the contour card except that it allows area fill between two contours of the fill of a specific material. It is usually used with the plot.2d statement.

contour This command allows the user to plot an isoconcentration line of the selected variable. It is usually used with the plot.2d statement.

label This allows the user to place a label on the plot at a given location.

option This command allows the user to pick the type of graphics device to use, specify graphics hard copy files, or specify the program's verbosity level.

plot.1d This command allows the user to plot the selected variable in one dimensional cross sections through device.

plot.2d This command allows the user to plot the outline and/or grid lines in the two dimensional mesh. It is very useful for setting up the display for the contours.

plot.3d This command lets the user plot a three dimensional bird's eye view of the device and selected variable.

print.1d This prints the information that a plot.1d would draw.

select This command allows a variable to be chosen as the z coordinate for the plot command to follow.

viewport This allows plotting into subsets of the terminal screen.

Miscellaneous Commands

cpulog This command instructs the program to dump cpu statistics whenever it feels like it.

echo This command prints a string.

pause This command waits for the user to input a command or a simple return.

printf This command passes each white space separated token to the expression parser.

2. PISCES

PISCES-II is a full 2-D semiconductor device simulation program which has been developed by Stanford University. It solves the Poisson equation and current continuity equations for up to two carriers in two dimensions to simulate the electrical characteristics of devices under either steady- state or transient conditions. The program solves these equations on non- uniform triangular grids so that the device structure can be completely arbitrary with general doping profiles, obtained either from analytical functions or SUPREM-III.

The details of the physical models and input syntax are described in PISCES-II user's manual.

PISCES-II has many applications. It is ideally suited to simulate and study new device structures because it solves all governing equations in the semiconductor with very few approximations. Combined with SUPREM-III, it can be used in the early phases of process and device development to design process experiments and understand device operation and problems. It will reduce the development cost and time. PISCES-II is also useful to device geometry and process parameters.

PISCES-II has no limit on device operation region and geometry. It provides simulations of full-range operation of any homogeneous semiconductor device with arbitrary geometry and doping profile. There are several problems , however. An arbitrary geometry inevitably complicates the grid generation. The inclusion of the current continuity equation brings the possibility of non-convergence. Thus, a user needs some knowledge of optimal grid generation and solution methods to avoid no-con vergence. In the worst case, the user needs to adjust the grid and experiment with solution methods to solve the convergence problem.

Generally speaking, there are three phases of PISCES-II simulations. First is the specification of the device structure. Doping profiles should be specified and optimum grid should be generated. All information is saved in a mesh file. Then, device characteristics at specified bias conditions are simulated and the solutions are saved. Finally, graphical displays of I-V characteristics or internal distributions are performed to extract the desired information from

the solutions. The detailed input specifications are presented in PISCES-II User's Manual. Some basic rules are summarized as follow:

PISCES-II takes its input from a user specified disk file. The input is read by GENII, the same input processor that is used in SUPREM. Each line is a particular statement, identified by the first word on the card. The remaining parts of the line are the parameters of that statement. The words on a line are separated by blanks or tabs. If more then one line of input is necessary for a particular statement, it may be continued on the continuation lines. Parameter names do not need to be typed in full, only enough characters to ensure unique identification is necessary. Parameters may be one of three types: numerical, logical or character.

The order of occurrence of cards is significant in some cases. The following card sequence can not be changed in the input file.

1) The mesh card must precede all other cards, except title and comment.

2) When defining a rectangular mesh, the order of specification is

Mesh

X.Mesh (all)

Y.Mesh (all)

Eliminate

Spread

Region

Electrode

Eliminate and spread cards are optional but if they occur they must be in that

order.

3) Doping and QF cards must follow directly after the mesh definition.

4) Before a solution, a symbolic factorization is necessary. Unless solving for the equilibrium condition, a previous solution must also be loaded to provide an initial guess.

5) Physical parameters may not be changed using the material, contact or model cards after the first solve or load card is encountered. The material and contact cards precede the model card.

6) A plot.2d, plot.1d or regrid cards which access solution quantities (potential, carrier concentrations, currents, recombination) must be preceded by a load or solve card to provide those quantities.

3. MAGIC

Magic is an interactive system for creating and modifying VLSI circuit layouts. With Magic, one can use a color graphics display and a mouse or graphics tablet to design basic cells and to combine them hierarchically into large structures. The system is unusual because it contains knowledge about geometrical layout rules, transistors, connectivity, and routing. It understands quite a bit about the nature of circuits and uses this information to provide you with additional operations. For example, Magic has built-in knowledge of layout rules; as you are editing, it continuously checks for rule violations. Magic also

knows about connectivity and transistors, and contains a built-in hierarchical circuit extractor. Magic also has a plow operation that you can use to stretch or compact cells. Lastly, Magic has routing tools that you can use to make the global circuits. Moreover, Magic makes it easy to modify existing layouts; this encourages designers to fix design errors, experiment with alternative designs, and enhance performance.

Magic is based on the Mead-Conway style of design. This means that it uses simplified design rules and circuit structures. The simplifications make it easier to design circuits and permit Magic to provide powerful assistance that would not be possible otherwise. However, they result in slightly less dense circuits than you could get with more complex rules and structures. For example, Magic permits only Manhattan design (those whose edges are vertical or horizontal).

4. MENTOR GRAPHICS

The IDEA Series developed by Mentor Graphics Co. is a family of computer workstations and software applications that help improve the productivity of electrical engineers, printed circuit board designers, and IC designers. The entire design process is covered by the IDEA Series: from schematic capture and circuit simulation to printed circuit board (PCB) and integrated circuit (IC) layout, test and verification, and project documentation.

IDEA Series workstations are computer systems that operate within an environment that is comprised of three independent and concurrently functioning environments:

1. Hardware

2. Operating System Software

3. CAE/CAD Applications Software

IDEA Series applications can be logically grouped as follows:

Schematic capture applications: NETED, SYMED, DTR, and EXPAND.

Digital and analog circuit simulators: QuickSim, QuickFault, TVER, MSPICE PLUS, MSPICE, and MSIMON.

PCB design applications: LIBRARIAN, PACKAGE, LAYOUT, AND Fablink.

Electronic packaging application: 3D Design (geometric modeling and drafting), AutoTherm, PCB Portal, and Package Station IGES.

Full custom IC layout applications: ChipGraph, REMEDI, DRACULAII, TRANSLATE, AND MCIF.

Standard cell IC layout application: CellGraph, Cellplace,and CellRoute.

Gate array IC layout applications: GateGraph, GatePlace, and GateRoute.

Document preparation applications: DOC and PicED.

Reference

[1] W. F. Kosonocky, et al, "A 320x244-Element IR-CCD Imager with PtSi Schottky-barrier detectors", Presented at IRIS Specialty Group on Infrared Detectors, Applied Phys. Lab. John Hopkins Univ., 16,17,18, August, 1988.

[2] W. F. Kosonocky, "Charge-Coupled Device Channel Structure," U.S. Patent No. 4,667,213, May 13, 1987.

[3] B. J. Esposito, "Charge transfer inefficiency of Buried-Channel Charge Coupled Device Registers for Low Temperature Operation of PtSi Infrared Image Sensors", Thesis, 1988.

[4] T. S. Villani, W. F. Kosonocky, et al, "Construction and performance of a 320 x 244-Element IR-CCD Imager with PtSi SBDs," SPIE Vol. 1170-01, March, 1989.

[5] D. K. Schroder, "Advanced MOS Devices", text book.

[6] W. F. Kosonocky and J. E. Carnes, "Basic Concepts of Charge-Coupled Devices," RCA Review, Vol. 36, No. 3, pp 566-593, Sep, 1975.

[7] A. M. Mohsen, Michel F. Tompsett, "The Effect of Bulk traps on the Performance of Bulk Channel Charge-coupled Devices", IEEE trans. on Electronic Devices, Vol. ED-21, pp 701-712, Nov. 1974.

[8] M. G. Collet, "The Influence of Bulk Traps on the Charge Transfer Inefficiency of Bulk Charge Coupled Devices." IEEE Trans. on Electronic Devices, Vol ED-23, No. 2, Feb. 1976, pp 224-227.

[9] J. D. E. Beynon and D. R. Lamb., "Charge Coupled Devices and their Applications", text book.

[10] S. M. Sze, "Physics of Semiconductor Devices", text book.

[11] G.W. Gaylor, P.K. Chatterjee and H.H. Chao, : A device Model for Buried Channel CCD's and MOSFET's with Guassian Impurity profiles," IEEE trans. on Electronic Devices Vol. ED-27, No.3, pp 199, Jan. 1980

[12] J. E. Carnes and W. F. Kosonocky, "Noise Sources in CCD's", RCA Review., Vol. 33, pp327, Jun 1972.

[13] Donald s. Wu, comments on 'A Device Model for Buried-Channel CCD's and MOSFET's with Gaussian Impurity Profiles', IEEE trans. on Electronic Devices, Vol., ED-27, No. 11, Nov., 1980.

[14] S.M. Sze, "VLSI technology", Second edition, 1988.

[15] W. F. Kosonocky, "Advances in Solid State Image Sensors", EE course at NJIT.

[16] Private communication with Dr. W. F. Kosonocky.

[17] Private communication with Elie I. Mourad.

[18] M. Kimata, M. Denda, et al, "Low-Temperature Characteristics of Buried Channel Charge Coupled Devices," Jap. J. of Appl. Phys.,

Vol. 22, No. 6, June 1983, pp 975-980.

[19] C. Niessen, "Hierarchical Design Methodologies and tools for VLSI chips", Proc. of the IEEE, Vol. 71, No. 1, pp 66-75, Jan. 1983.

[20] Kit Man Cham, Soo-Young OH, Johg L. Moll, Paul Vande Voorde, Dareje Chin, "Computer Aided Design and VLSI Device Development"' text book.