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Design, fabrication, and testing of temperature compensated MAGFET

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Abstract

A simple model based on dc behaviour of MOS transistors operating in weak inversion is derived on the basis of previous publications. The bipolar like source to drain transfer characteristics of MOS transistor in weak inversion was used to implement a voltage source that is proportional to absolute temperature (PTAT); a cell that can be stacked to obtain the desired voltage. A CMOS temperature compensated current reference is implemented using PTAT cell with MOSFET as current defining element. A CMOS magnetic field sensor has been developed. The sensitivity of sensor is dependant on the bias current; incorporation of temperature independent biasing current (current reference) will increase the sensitivity of the sensor. Simulation and test results observed have been presented and compared.

Design, Fabrication, and Testing of Temperature Compensated MAGFET.

by

Dilip K. Sampath

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Contents

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Chapter 1

Introduction

The temperature compensated reference biasing a Dual Drain MAGFET described in this thesis was designed, fabricated and tested at the Siemens Corporate Research Inc., Princeton, N.J, under the direction and with support of Dr. Durga Misra, Asst.Professor, ECE Dept, NJIT and Mr. James H. Atherton, Group Leader, Advance IC Group at Siemens. Technical support for this project was also provided by Mr. Steve Kosonocky and Mr. Greg Kazmierczak of Siemens Corporate Research.

The major goal of this thesis was to develop an temperature independant biasing circuitry for the MAGFET, and thereby develop a temperature independant MAGFET. The Magnetic Field Sensor (MFS) have typical application in areas like : speed sensing, current sensors, position sensing, machine tool controls and etc. where they are applied over wide ranges of temperature. Conventional Hall sensors have undergone considerable changes and MOS technology have been used to develop a high gain MFS with dual drain MOSFET, as presented by Misra[6]. Various designs have been discussed by Gray et al[5], on temperature compensation using bandgap references. Operation of MOS devices and temperature effects have been discussed in details by Sze[3] and Tsvidis[9] and models have been developed by them. Operations of transistors in weak inversion have been modelled and presented by Vittoz et al [10],[12]. They have also developed a temperature

independant source using this model which is independant of temperature. An enhanced temperature compensated current refernce was discussed by Sansen et al [13]. This thesis shall discuss the realisation of temperature compensated current reference circuit developed to bias the MAGFET.

Chapter 2, deals with an overview of MAGFET and the Hall element [1],[2]. Also the hypothetical bandgap reference as discussed by Gray et al [5] is presented.

Device performance parameters and the operation of Dual Drain MOSFET as MFS is dealt in Chapter3. A review on figure of merit for MFS [7] is also presented in this chapter.

The basic theory of Current with the drift and diffusion component [9], different region of operation of MOS transistor are dealt in Chapter4. A model on weak inversion region of the transistor is developed and also a voltage source which is proportional to absolute temperature (PTAT), using the above model is also presented. This chapter also deals with the realisation of the temperature compensated current source with PTAT voltage source.

The circuit simulation and fabrication of integrated MFS with temperature compensated current reference circuit is presented. Results of simulation and test results are also discussed in this Chapter 5.

Chapter 6 discusses the conclusion and the possible areas of future development.

Chapter 2

Hall Element and Magfet - An Overview

2.1 MOS Hall element

The surface inversion layer of the MOSFET can be used for generating a Hall effect device compatible with integrated circuit technology[6]. This thesis describes the design of magnetic field sensor (MAGFET) with a novel geometry which, when used in appropriate circuits, results in improved sensitivity. The device and the associated circuit are to be fabricated using CMOS technology.

The first MOS Hall element was proposed by Gallagher and Corak. With the development of planar technology and MOSFET, fully isolated Hall elements have been incorporated into monolithic silicon integrated circuit. Leaving aside the problems like lower mobility of silicon and withstanding the fact that Hall effect is a bulk phenomenon, the surface inversion layer of MOS structure can be readily used for generating a Hall element compatible with integrated circuit technology with very precise control of dimensions. About 10^3 V/AT, [2] (where A is consumption current in Amperes and T is the magnetic induction in Tesla) sensitivity has been reported in such devices.

When the MOS device is properly biased and placed in a magnetic field so that the field is orthogonal to the drain current, then Hall voltage is generated in the

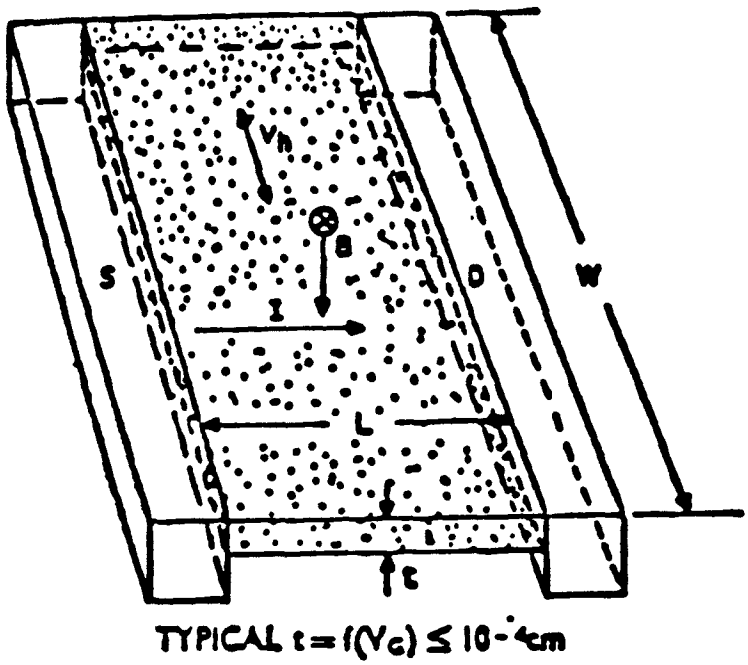


Figure 2.1: Generation of Hall voltage

inversion layer as shown in Fig 1.1. The voltage is generated within the inversion layer and not in the bulk silicon. The thickness t of the inversion layer is determined by the gate voltage and is typically between 30 to 300 $\AA$ [3]. The construction of an MOS Hall generator now requires only the addition of Hall contacts to the MOS device. The Hall contacts are formed in an identical manner to the drain and source region by selective diffusion through a silicon oxide mask. They are in fact, diffused simultaneously in the same step as the source and drain. As seen in Fig. 2.2 the gate electrode G, overlaps the two diffused contact regions so that when the inversion layer is formed, the drain source and contact regions are resistively connected.

When the gate voltage V_{GS} is increased above the threshold voltage V_{Th},

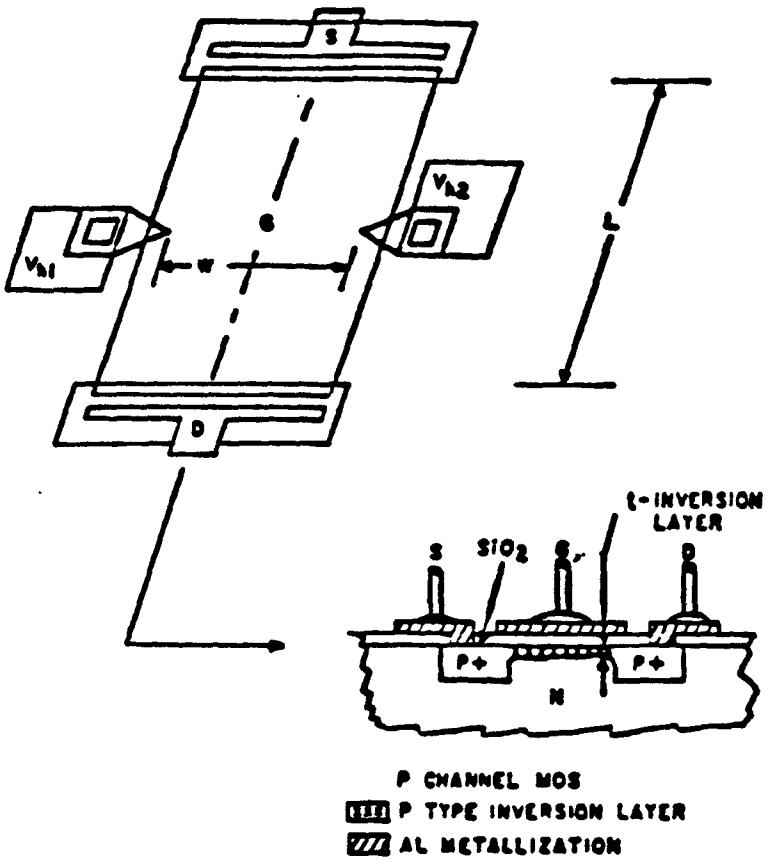


Figure 2.2: MOS Hall contacts.

the drain source current rises only when $|(V_{GS} - V_{Th})| < |V_{DS}|$. At the same time, however, the thickness of the inversion layer in which the Hall voltage is generated also increases. Since Hall voltage varies directly with drain current and inversely with thickness, the two effects tend to offset each other. Above the threshold voltage V_{Th} of the device, the effect of the gate-source voltage on the inversion layer thickness predominates, while below the threshold voltage the current falls so rapidly (exponentially) that it then becomes the controlling factor. Assuming that for the field strength considered, the Hall co-efficient for silicon is constant, the effective inversion layer thickness is decreases at the drain-end as the pinch-off current is approached. That is, as current flows from drain to source through the purely resistive inversion layer path, a voltage gradient is set up. This voltage gradient alters the depletion region thickness near the drain region there by reducing the effective inversion layer thickness of the device.When a magnetic field is applied perpendicular to the current flow a higher Hall potential is to be generated because of the concentration of electrons in one of the sides due to the Lorentz force for a thinner inversion layer if the Hall contacts are put close to the drain end. Therefore appreciably higher Hall voltages are attainable if the device is operated beyond pinch-off. It is to be noted that the integrated Hall element and the MOS transistor require conflicting geometries to optimize their performance.

2.2 Advantages of CMOS technology

In CMOS technology, on the other hand the self isolation for the devices is an important advantage. Here the inversion layer is formed close to the surface of the semiconductor. The current within the MOS transistor flows at the semiconductor surface between the source and the drain diffusion unknown as the channel region. The current flowing into the drain leaves the source because there is no gate current.

Thus the MOS channel region is considered to be completely isolated and it forms an effective Hall element in monolithic silicon.

2.3 Split Drain MAGFET

The split drain MOS transistor was proposed by Fry and Hoey [1] where drain of a MOS transistor was split into two equal regions. The asymmetry in current flow into the drains could be detected when the device is exposed to a magnetic field. If the voltage on these two drain were higher than the gate voltage, the depletion layers formed between the drains and the channel would prevent voltage changes on the drains from affecting the channel voltages. The output impedance would therefore be high and so the device would be capable of producing high output voltages under suitable load conditions. Thus it shows a higher sensitivity of about 10^4 V/AT [2] where A is in amperes and T is in teslas.

Since signal current is obtainable only at the edge of the channel, if the drain is split into three regions, of which the center one is largest and take the majority of the device current, we should obtain the large fractional current changes in the outer drains.

Putting resistive load in a split drain configuration similar to that of differential pair configuration has been discussed by Hollis. In this in this arrangement it is seen that at high magnetic field, the change in drain voltage has an influence on the drain current due to channel- length modulation.

2.4 Mobility Consideration

The normal mobility in the channel is expected to be influenced by the thickness of the inversion layer. When a very small longitudinal field E_y is applied (E_y is parallel to the current flow), the drift velocity varies linearly with E_y and the slope is the

drift mobility ($v = \mu E_y$). Experimental measurements on $< 100 >$ p-type silicon inversion layers show that this mobility is a unique function of the transverse field E_x, which is perpendicular to the current flow[3]. This mobility is not a function of surface processing or doping density in the range $N_A < 10^{17} cm^{-3}$. At a given temperature, mobility decreases with increasing effective transverse field, defines as the field averaged over the electron distribution in the inversion layer. However, to simulate the MAGFET [4] the mobility used is given by

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N/N_{ref}^{\alpha})} \tag{2.1}$$

where for electrons $\mu_{min} = 65$, $\mu_{max} = 1330$, $N_{ref} = 8.5 \times 10_{16}$ and $\alpha = 0.72$ [6] these give

$$\mu_n = \left[65.0 + \frac{1265}{1 + (N/8.5 \times 10^{16})^{0.72}}\right] \tag{2.2}$$

where N denotes the total impurity concentration. For the Hall mobility the relation used is $\mu_H = r\mu$ where r = 1.18 for phonon scattering and 1.93 for ionized impurity scattering. However, lattice scattering is is the dominant mechanism in limiting the mobility of free carriers at high temperature and low impurity concentration. At low temperatures and high impurity concentration, scattering by impurities may take over as the limiting mechanism [6]. However, mobility in the channel can be expressed as

$$\frac{1}{\mu} = \frac{1}{\mu_B} + \frac{1}{\mu_s} \tag{2.3}$$

where μ_B is the bulk mobility and μ_S is the surface mobility. According to Schwart and Russek the surface mobility in Eqn (2.4) is replaced as in Eqn (2.5).

$$\frac{1}{\mu} = \frac{1}{\mu_B} + \frac{\overline{p} m_* v_{tk}}{2q(Z_{QM} + ZCL)} \tag{2.4}$$

where $\overline{p}$ is the probability of diffused scattering and depends on surface phonon and surface charge cross-section as well as surface roughness, v_{tk} is the thermal electron

velocity, Z_{QM} is the quantum mechanical channel thickness, where as Z_{CL} is the classical channel thickness, and m_* is the effective mass of the electron. Baccarani et al [18] suggested that the channel layer broadens in thickness at higher temperatures and this may largely be due to carrier degeneracy i.e. Fermi-Dirac statistics should be used in place of Boltzmann statistics. This dependence predicted by the diffused scattering model is the consequence of the simultaneous variation with temperature of both relaxation time and the fermi level in the bulk. For lower impurity concentration the mobility decreases as $T^{-3/2}$. But the measured slopes, however, differ from -3/2 because of the other scattering mechanisms. For intrinsic materials near room temperature the mobility varies as $T^{-2.42}$ and $T^{-2.30}$ for n and p-type silicon respectively.

Hence at high temperature, the differential current in a split drain MAGFET should fall rapidly because of the decrease in mobility and increase of channel thickness at the pinch-off point (reducing Hall field).

2.5 Bandgap Reference - Hypothetical

As we had discussed so far the temperature dependance of the biasing current, this dependance shall affect the sensitivity of the MAGNETIC FIELD SENSOR (MFS) being developed. We shall now discuss the concept of Bandgap references[5] and thereby design a temperature compensated current reference.

Let us consider the hypothetical circuit of fig(2.3). An output voltage is developed that is equal to $V_{BE(on)}$ plus a constant K times V_T. In order to determine the required value for K, we must determine the TC of $V_{BE(on)}$ precisely. The $V_{BE(on)}$ can be written neglecting base current,

$$V_{BE(on)} = V_T ln \frac{I_i}{I_S} I_S = \frac{qAn_i^2 \overline{D}_n}{Q_B} = Bn_i{}^2 \overline{D}_n = B' n_i^2 T \overline{\mu}_n. \tag{2.5}$$

The saturation current I_S, is related in terms of the device structure where n_i

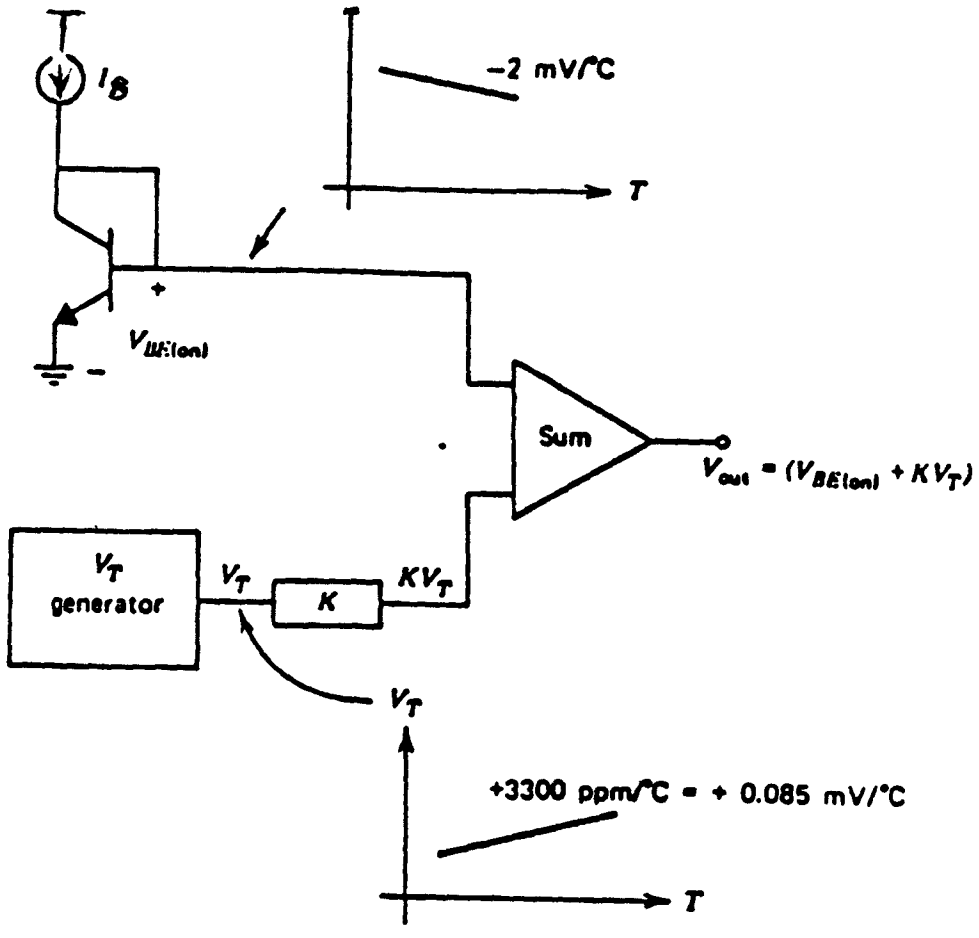


Figure 2.3: **Hypothetical Bandgap Reference Circuit**

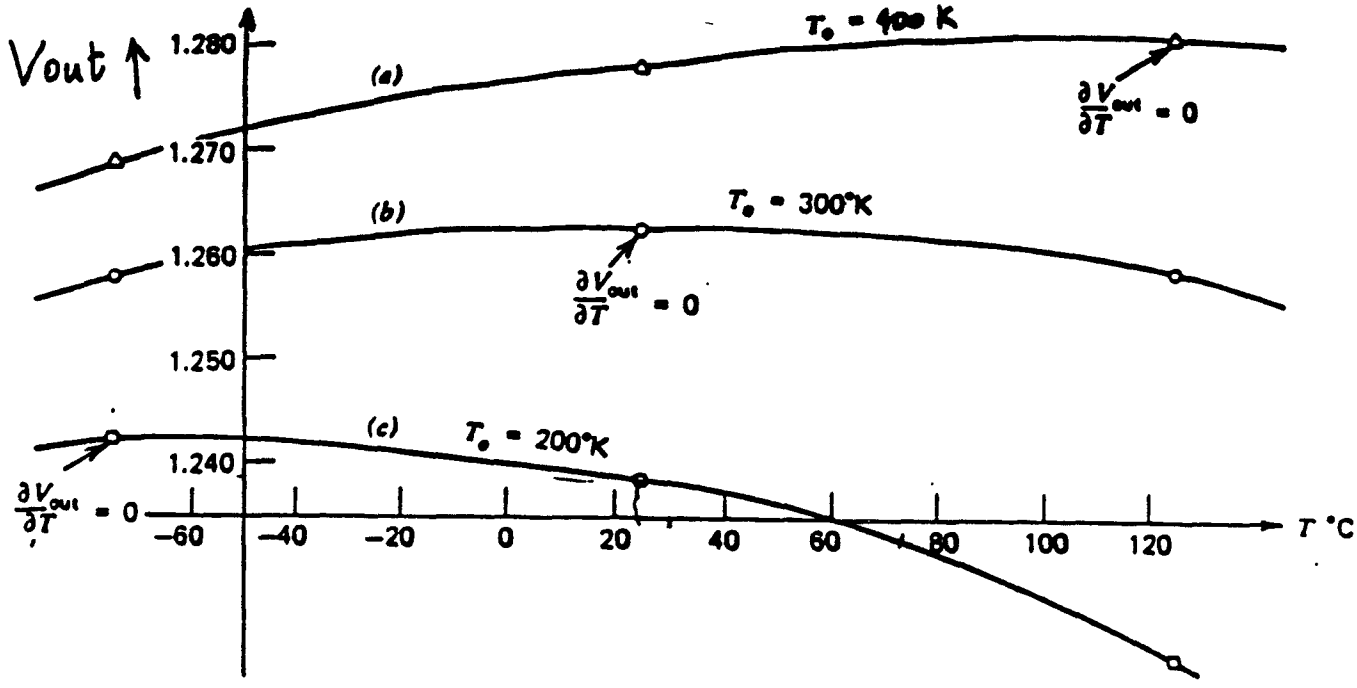


Figure 2.4: Variation of band gap reference output voltage with temperature

independent of temperature, we can take derivative of V_{out} w.r.t. temperature to find the required values of G, γ, and K to give zero TC_F. Differentiating,

$$0 = \frac{dV_{out}}{dT}|_{T=T_o} = \frac{V_{To}}{T_o}(K + lnEG) - \frac{V_{To}}{T_o}(\gamma - \alpha)lnT_o - \frac{V_{To}}{T_o}(\gamma - \alpha). \qquad (2.11)$$

where V_{To} is thermal voltage, V_T is evaluated at T_o. Rearranging,

$(K + lnEG) = (\gamma - \alpha)lnT_o + (\gamma - \alpha)$. This equation gives the required values of circuit parameters, K, γ and G, and the device parameters, E and γ. We have,

$$V_{out}(T) = V_{GO} + V_T(\gamma - \alpha)(1 + ln\frac{T_o}{T}). \qquad (2.12)$$

Thus the temperature dependance of the output voltage is entirely described by the single parameter, T_o, which in turn is determined by the constants K, E and G. Figure 2.4, shows voltage variation for different values of T_o, for the special case when $\gamma = 0$ and I_1 is temperature independent. The output voltage at zero TC_F temperature ($T = T_o$) is given by

$$V_{(out)}(T)|_{T=T_o} = V_{GO} + V_{To}(\gamma - \alpha). \qquad (2.13)$$

For example, in order to achieve to zero TC_F at $25°C$, assuming that $\gamma = 3.2$ and $\alpha = 1$,

$$\begin{aligned} V_{(out)}(T)|_{T_o=25°C} &= V_{GO} + 2.2V_{To} \\ V_{(out)}(T_o)|_{T_o=25°C} &= 1.205V + (2.2)(26mV) \\ &= 1.262V \end{aligned} \tag{2.14}$$

where band-gap voltage is silicon is $V_{GO} = 1.205V$

The parameter of interest in reference voltage sources is the variation in the output voltage for the entire range of temperature. Since the TC_F expresses the temperature sensitivity only at one temperature, an effective TC_F to characterize the behavior over broad temperature range is given below:

$$TC_F = \frac{1}{V_{out}}\left(\frac{V_{max} - V_{min}}{T_{max} - T_{min}}\right) \tag{2.15}$$

where V_{max} and V_{min} are the largest and smallest output voltages observed over the temperature range and $T_{max} - T_{min}$ is the temperature excursion. V_{out} is the nominal output voltage.

Chapter 3

Magfet Design and Performance Parameters

3.1 Introduction

In this chapter the device theory of the MAGFET is presented and the advantages of MOS technology for implementing a magnetic sensor are highlighted. Some ideas leading to a modified device geometry in a split drain configuration are discussed. A brief discussion on the figure of merit of the device is also included.

3.2 Figure of Merit

This section discusses the figure of merit used to compare various magnetic sensors[7]. These include sensitivity, noise, offset signal, linearity, and temperature coefficients. As the device proposed in this thesis is closely related to the split drain MAGFET, which operates via carrier deflection, much of the discussion in this section will relate only to such devices.

3.2.1 Sensitivity

One of the most important figure of merit of any sensor is the sensitivity. This can be simply defined as the incremental change in the output signal due to an incremental change in the applied magnetic field. For magnetic field sensors many

units of sensitivity have been used in the literate. These include T^{-1}, V/T, and the V/AT. This makes comparison of magnetic sensors difficult and a standardized unit is desirable. The Lorentz condition as defined below explains the Hall field:

$$V_H = \frac{R_H I B_Z}{t} \tag{3.1}$$

where

R_H = Hall coefficient in cm^2/coulomb

I = Bias current in amperes

B_Z = Normal component of magnetic field, in Gauss

t = Thickness in cm

V_H = Hall voltage in volts.

For devices which exploit the Hall field the output signal is clearly the Hall voltage, V_H. This leads to a unit of sensitivity of V/T. But as indicated by Eqn (3.1), V_H is proportional to the bias current. Hence a preferable unit is the V/AT.

Devices that operate via carrier deflection (magnetotransistors and split drain MAGFETs) sometimes have their sensitivities reported in units of V/T or V/AT. This is due to the fact that the current imbalance is usually converted to a voltage by a resistive (or active) network. Nonetheless, the actual output signal is still the current imbalance. Hence, the sensitivity of the device is really the ratio of the current imbalance of the applied magnetic field. This is usually proportional to the bias current and a preferred unit would be T^{-1} arising from:

$$S_r = \frac{1}{I_D} \cdot \frac{\partial I_D}{\partial B} \tag{3.2}$$

To facilitate comparison the sensitivities of the various devices, discussed in the next chapter, will be quoted in units of V/AT, for Hall plates and T^{-1}, for device operating via carrier deflection, where possible.

3.2.2 Noise

Noise phenomena can severely limit sensor performance. In fact, the signal-to-noise ration (SNR) can be a more important figure of merit than sensitivity.

At low frequencies, flicker (1/f) noise is the fundamental limitation. This determines B_{min}, the minimum detectable magnetic field. At high frequencies, thermal (Nyquist) noise dominates.

For split-drain MAGFETs the mean square current per unit bandwidth is given by [13]:

$$\frac{< i_{DF}^2 >}{\Delta f} = \frac{(q\mu_n V_D)^2 N_s W}{L^3 f} \tag{3.3}$$

N_s is the density of surface states and the remaining symbols have their usual meaning. From this equation we see that a long device with a thin channel is preferable. However the choice of the width, W, cannot be made arbitrarily small as it is limited not only by technology but also the fact that the device current is proportional to W. The SNR increases as the bias current is increases, however, the maximum current is limited by power dissipation considerations.

3.2.3 Offset Signal

The offset signal (current in split-drain MAGFETs and voltage in Hall plates) refers to the output signal in the absence of an applied magnetic field. As the offset is usually static, or slowly-varying, it is not a problem in the case of high-frequency measurements. However, it can be a serious problem at low frequencies since it can not be distinguished from the component of the output that is proportional to $\vec{B}$.

The major factor contributing to the offset signal in MFS is the fabrication process (i.e. alignment errors and non-uniform dopings).

The offset voltage of the Hall plate is also very sensitive to mechanical strain; this effect has been used in design of pressure sensors.

3.2.4 Linearity

Obviously, it is desirable to have a sensor whose output is linear over a range of magnetic fields. Most MFS show no appreciable non-linearities at low fields. In two-dimensional numerical simulations of split-drain MAGFETs, Natan et al. [13] found slight deviations from linear behavior at field approaching 1T.

3.2.5 Temperature Coefficients

The effects of temperature can be separated into two categories: narrow range and wide range. As the names imply narrow range refers to the operation at a fixed temperature which may fluctuate by a small amount, and wide range refers to operating the device at widely separated range of temperatures.

For most applications, the sensitivity should be measured at the temperature which the device is to be operated and the narrow range temperature sensitivity should be checked to see if it is acceptable.

The effects of temperature on MAGFET sensitivity has been investigated [6]. It was found that at temperatures below room temperatures below room temperature, the sensitivity varied as $T^{-2.18}$ for $0.2T < B < 1T$. This was attributed to the T^{-2} variation of the electron mobility. At higher temperatures the sensitivity decreased rapidly. This was attributed to the broadening of the inversion layer with increasing temperature. Temperature dependance of MOS transistors are discussed in Chapter 5.

3.3 Device Geometry

The physical dimensions of the devices are shown in Fig. 3.1. The three devices are of similar type with different aspect ratios as 0.5, 0.25 and 1.0 respectively. In case of device-1 the W = $20\mu m$ and L = $40\mu m$ device-2 the W = $10\mu m$ and L = $40\mu m$

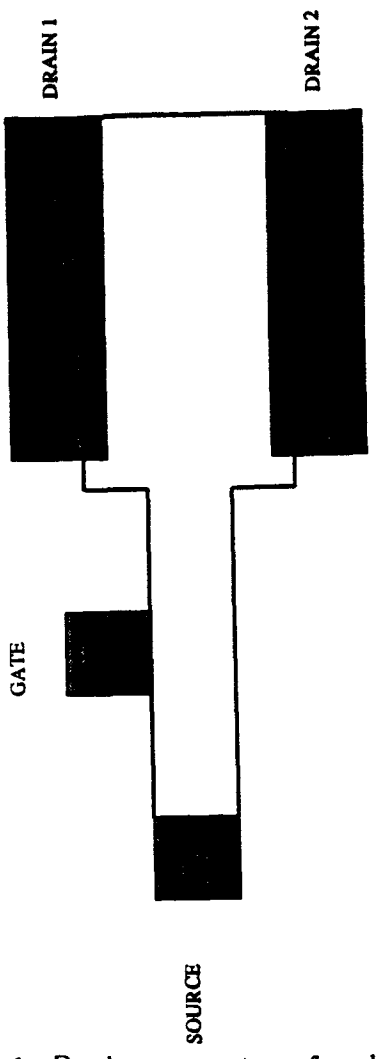


Figure 3.1: Device geometry of n-channel MAGFET.

and in case of device-3 the W = $40\mu m$ and L = $40\mu m$. In these types of devices the drain has been split into two parts. To make sure there is no diffusion between them the polysilicon gate has sufficient overlap over the device well. The drains are bent perpendicularly sideways for more drain area and to make the slope of the surface potential smooth for better carrier collection i.e. all the carriers deflected by the magnetic field will go to a lower energy state and will be collected by the drains.

Notches were made on both sides of the gate to squeeze the carriers in the channel. In this way the carriers of the channel can be collected when they are deflected by a small magnitude of the Lorentz force giving rise to a maximum

variation in the drain current. The single source is continuous and bent sideways like the drains in these devices.

Adequate care was taken to avoid the short circuiting between drains through diffusion. For this device the source is continuous and the gate is of normal rectangular shape. To find the actual gate area of the devices, the area covered by the poly-silicon over the device well has been taken as the actual gate area.

3.4 Operational Principle

The operation of the device can be explained in terms of the current variations in the drains [6]. A magnetic field perpendicular to the planar surface affects the current in the the split drain transistor. The deflection of the carriers due to the Lorentz force leads to an increase of current in one drain at the expense of the current in the other drain.

Looking at the three dimensional surface charge distribution [8], surface potential and the electric field at the surface of MOSFET device, it is easily understandable that almost all the carriers, deflected by the Lorentz force, will be collected by one drain at the expense of the other. The notch in the gate helps to squeeze the carriers towards the drain.

The device acts like a differential pair because of the split drain structure and since the drains are connected to the resistive of dynamic loads, a small variation in the drain currents will lead to large variation in the differential output voltage. Because of better carrier collection, there is a considerable amount of current variation giving rise to a better gain.

3.5 Device Performance Parameters

When a magnetic field is applied to a dual-drain MAGFET, a differential voltage is generated between the drains using Fig. 3.2. Without the magnetic field, this differential voltage is arranged to be zero using a potentiometer. We define the transduction constant (or simply the gain constant) 'χ' of the circuit containing the MAGFET, as the change of differential voltage per unit change in the magnetic field, expressed as

$$\chi = |\delta V/\delta B| \tag{3.4}$$

which has the dimension of volts per tesla. The voltage parameterχ can be converted to current by dividing χ by the load resistance. i.e.

$$\chi = |\delta V/\delta B| = 2\left(|\delta I_1/\delta B| + |\delta I_2/\delta B|\right) R \tag{3.5}$$

where I_1 and I_2 are the currents in each drain (as in Fig.3.2) and R is the load resistance. With B = 0

$$I_1 = I_2 = I \tag{3.6}$$

The magnetic field, applied to the MAGFET at right angles to the direction of current flow, causes a change in the currents in the drains while the total current is maintained constant (i.e. current increases in one drain at the expense of the current in the other drain) by the bias arrangement. Representing the currents flowing in drain-1(I_1) and drain-2 (I_2) by I + i and I = i respectively, where i is the small change in the current called the signal component due to the magnetic field. Here we define another quantity as the signal to common mode component ration 'ξ' (SCCR) expressed as the fractional change in current per the initial current flowing in the drain, i.e.

$$\xi = \frac{i}{I} \tag{3.7}$$

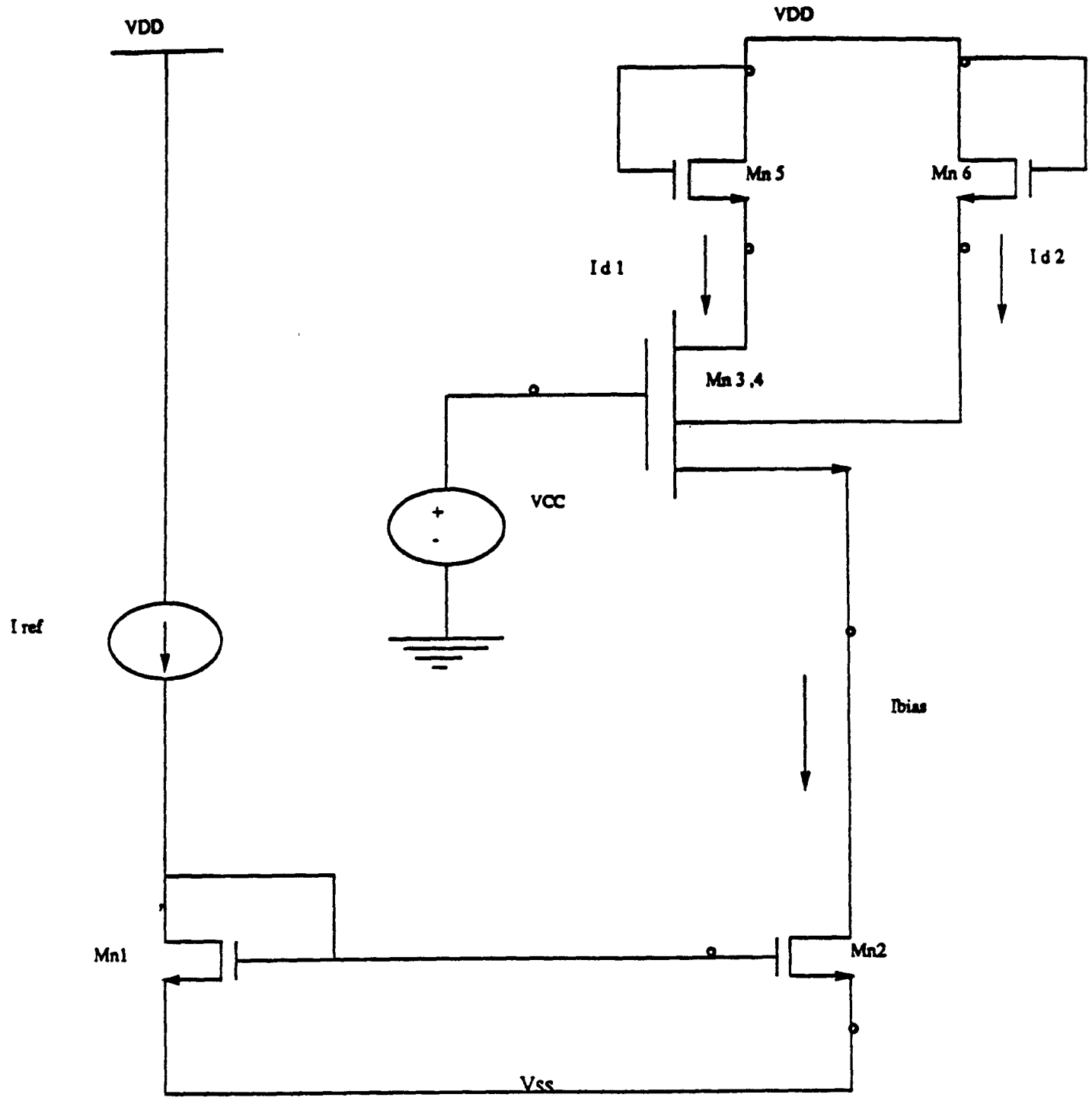


Figure 3.2: **Magnetic Field Sensor**

We must subtract the current I_2 from I_1 to obtain 2i. The subtracting circuit will have non-idealization. Characterizing the current differencing circuit in terms of differential gain (A_d) and common-mode gain (A_{cm}) we have

$$I_o = A_d(I_1 - I_2) + A_{cm}(\frac{I_1 + I_2}{2}) \tag{3.8}$$

where $I_1 = I_2 = 2i$ and $\frac{I_1+I_2}{2} = I$. A finite A_{cm} will give rise to a large offset if the common mode component in the input is large. So to obtain an accurate transduction constant χ, the SCCR should be as high as possible.

Chapter 4

Current reference - Temperature compensation

4.1 Introduction

Having developed the design of Magfet, its operation principle and also the dependance of the MFS sensitivity on temperature; we shall design a current reference circuit which shall be compensated for temperature variation for the range -55^{o} *to* 125^{o} C. In the following subsections we shall develop the conduction mechanism in a semiconductor, discuss the transistor region of operation, discuss a simple model in weak inversion or sub-threshold region which will be used in our design of PTAT. Proportional To Absolute Temperature, (PTAT), transistors shall be used in the current reference circuit. We would then substantiate the design of temperature compensated circuit with our simulated results.

4.2 Conduction

4.2.1 Drift

Let us consider a piece of semiconductor with no electric field applied to it [9]. A random "thermal" motion is exhibited by holes and electrons in all direction; however, on the average these random movements cancel out and there is no net

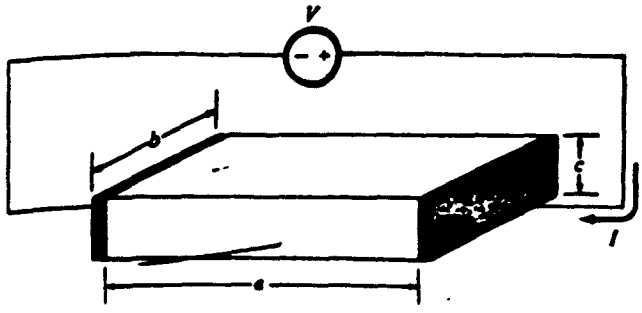


Figure 4.1: **A n type semiconductor with a uniform electric field under external bias**

current produced. If an electric field is now applied (by connecting a battery across the terminals of the semiconductor), it will exert forces on the charged particles. Thus there will be a net movement along the field lines which can be observed macroscopically as an electric current. This phenomenon is known as *drift*; it would occur when particles were not are charged.

We can calculate the average current, ignoring noise fluctuation, and this current will be a non zero because the net movement caused by the nonzero electric field. The quantity I can be calculated from the carrier's average velocity called *drift velocity*, v_d and the magnitude charge per unit area, $\frac{|Q|}{ab}$. Hence,

$$\begin{aligned} |Q'| &= \tfrac{|Q|}{ab} \\ &= nqc, \\ I &= b|Q'||v_d| \end{aligned} \tag{4.1}$$

In case of low electric fields, the above relations assume special and useful form. For silicon, low means roughly less than $0.3\frac{V}{\mu m}$ for electrons, and less than $0.6\frac{V}{\mu m}$ for holes. For such fields the drift velocity is proportional to the electric field, were proportionality constant is called *mobility*, μ_B.

$$|v_d| = \mu_B|E| \tag{4.2}$$

$$|E| = \frac{V}{a} \tag{4.3}$$

Hence we obtain,

$$I = \mu_B n q \frac{bc}{a} V; \tag{4.4}$$

which is nothing but Ohm's law. this equation can be written of the form I = GV, where G is called the *conductance* and is given by:

$$\begin{aligned} G &= \sigma \tfrac{bc}{a} \\ \sigma &= \mu_B n q \end{aligned} \tag{4.5}$$

where σ, is the conductivity, using Eqn 4.2 and Eqn 4.4 we can express conductivity as follows:

$$G = \mu_B |Q'| \frac{b}{a} \tag{4.6}$$

The I - V relation is thus,

$$I = \mu_B |Q'| \frac{b}{a} V \tag{4.7}$$

4.2.2 Diffusion

Drift is only one of the two mechanism responsible for the flow of electric current in the semiconductors. The other mechanism known as *diffusion* occurs whenever the particles are not distributed uniformly over space, that is when there is "concentration gradients", [9], then the random motion of particles tend to spread out from region of high concentrations to a region of low concentrations. This phenomena is not due to electric fields and can thus occur independently of whether or not the particles are charged. However, if the particles are as electrons and holes, diffusion gives rise to movement of charge and thus electric current. From the figure 4.2, we can define the origin of diffusion. Here a piece of semiconductor of rectangular cross section with 'a' length, 'b' width and 'c' as thickness is assumed to contain electrons uniformly distributed in any vertical plane, but nonuniformily along the length. No holes are assumed in this present case. We would find that the electrons

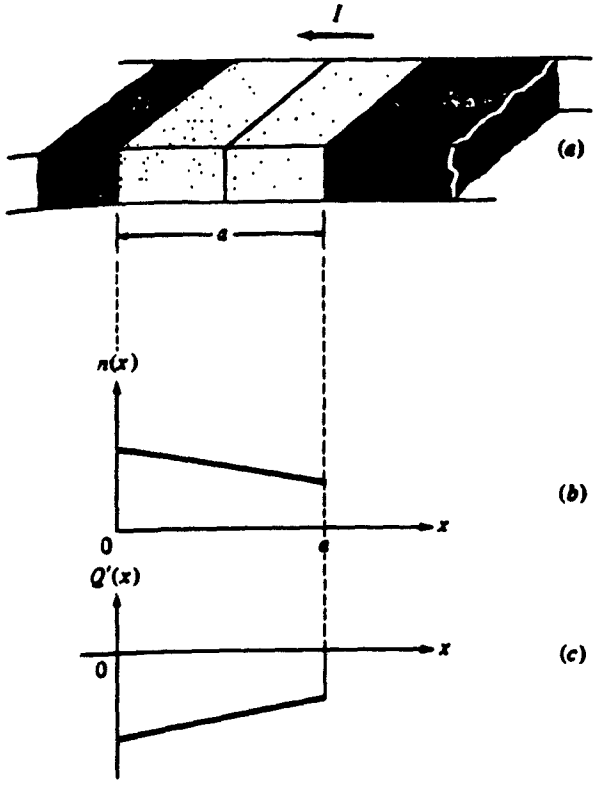


Figure 4.2: (a) A semiconductor bar with nonuniform electron concentration along its length; (b) the electron concentration in (a) for a special case of interest; (c) charge per unit area corresponding to (b).

at the left are of higher concentration than those in the left. Hence one can expect electrons to move from left to right, in a given interval of time. This corresponds to movements of electrons from left to right. Since each carries a negative charge, the current is proportional to the magnitude of the charge q carried by each electron and the cross section bc. Also, more the negative is the slope $(-\frac{dn}{dx})$, the more positive is the current:

$$I = Dq(bc)(-\frac{dn}{dx}) \tag{4.8}$$

where D is a constant of proportionality called *diffusion constant.* This constant is related to the mobility by the Einstein relationship:

$$D = \mu_B U_T \tag{4.9}$$

where $U_T = \frac{kT}{q}$, the thermal voltage.

Consider a thin vertical slice of the material in Fig 4.1 of volume $bc\triangle x$ centered around a point at x. The charge in this slice is $(-q)n(x)bc\triangle x$, where the -sign corresponds to the negative electron charges. Dividing the slice charge by the area of the slice $\triangle x$ as seen from the top of the fig 4.8 and letting $\triangle x$ go to zero, we obtain charge per unit area which is function of x:

$$Q'(x) = (-q)cn(x) \tag{4.10}$$

This figure is shown in the figure 4.2c. Using equation 4.7, 4.8 and 4.9 we obtain:

$$I = \mu_B U_T b \frac{dQ'(x)}{dx} \tag{4.11}$$

4.3 Temperature Effects

Effective mobility, is one of the main parameters responsible for the strong temperature dependance of the MOS transistors[9]. An often used approximation to

describe the decrease of effective mobility with temperature is,

$$\mu(T) = \mu(T_r)\left(\frac{T}{T_r}\right)^{-k_3}. \tag{4.12}$$

where T is absolute temperature, T_r is room temperature, and k_3 is a constant, with values between 1.5 and 2.0.

Other temperature dependant parameters are ψ_B and V_{FB}, which manifest in the values of V_T which aalmost decrease linearly with temperature which can be approximated by :

$$V_T(T) = V_T(T_r) - k_4(T - T_r) \tag{4.13}$$

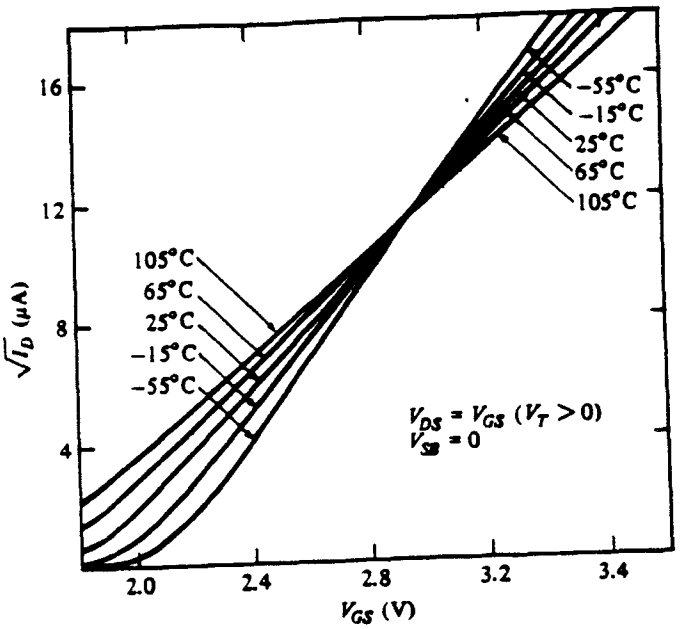
where k_4 is constant with values between $0.5mV/K$ and $4mV/K$, with larger values corresponding to heavier doped substrates, thicker oxides, and smaller values of V_{SB}.

The effeect of temperature on transistor characteristics, can be studied by considering a device operating in saturation. From the saturation equation, we have:

$$\sqrt{I_D} = \sqrt{\mu(T)}\sqrt{\frac{1}{2}\frac{W}{L}C_{ox}}\,[V_{GS} - V_T(T)] \tag{4.14}$$

. Thus a temperature increase should tend to increase the drain current through $V_{GS} - V_T(T)$, and to decrease it through $\mu(T)$. A measured set of $\sqrt{I_D} vs V_{GS}$ is shown in figure 4.3. At high currents, the decrease of $\mu(T)$ with temperature and at low currents the increase with temperature can be noticed. At certain V_{GS}, current becomes pratically temperature independant over a large temperature range. These effects are evident in the figure. The bottom, curved part of the characteristics is due to moderate and weak inversion.

As can be deduced from the above figure, in weak inversion and for a given V_{GS} the drain current increases with temperature. Plots of $I_D(log) vs V_{GS}$ are shown in the figure 4.4. It can be observed increasing temperature decreases the slopes of the curves and the junction leakage (broken curves) drastically increases with



Measured $\sqrt{I_D}$ vs. V_{GS} for a device with $V_T > 0$, with fixed V_{SB} and $V_{DS} = V_{GS}$, for various temperatures.

Figure 4.3

temperature and masks the weak inversion current, thus diminishing the range of currents over which exponential behaviour is observed.

4.4 Transistor Regions of operation

Having discussed the concept of flow of electric current due to Drift and Diffusion mechanisms in semiconductors and temperature effects of MOS transistors, we shall discuss the model on the basic feature of Metal Oxide Semiconductor(MOS) transistors region of operations. Corresponding current-voltage characteristics of the above NMOS transistors, in fig 4.2 is shown in fig.4.5.

We shall define the transistor region of operation as shown in the table in fig 4.5.

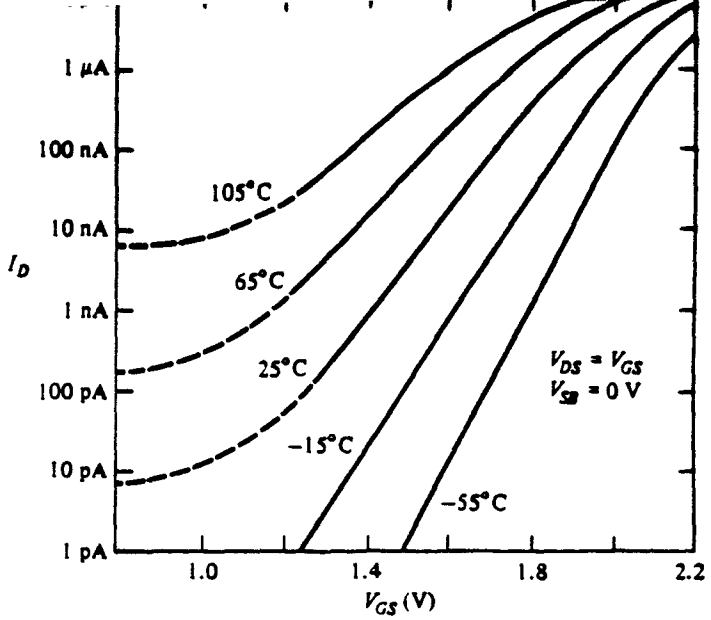


Figure 4.4: Measured $I_D vs V_{GS}$ at low currents for various temperatures. The broken part indicates the effect of leakage.

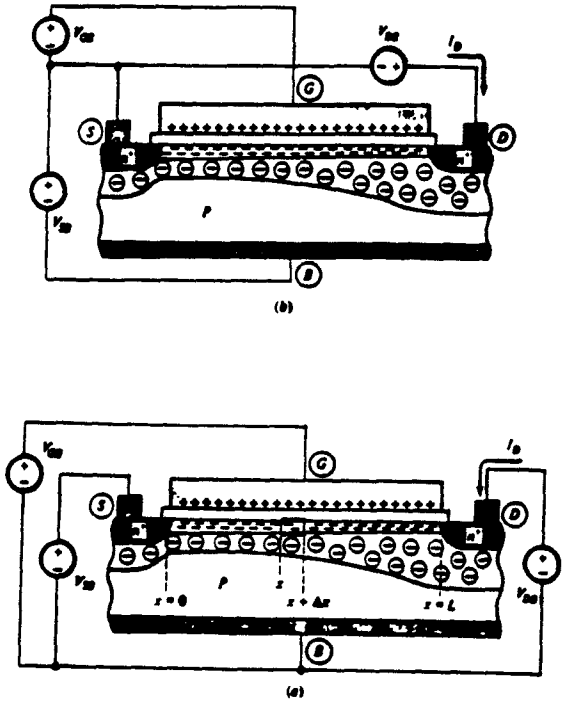


Figure 4.5: A n-channel MOS transistor. (a) Terminal voltages referred to the substrate; (b) terminal voltages referred to the source.

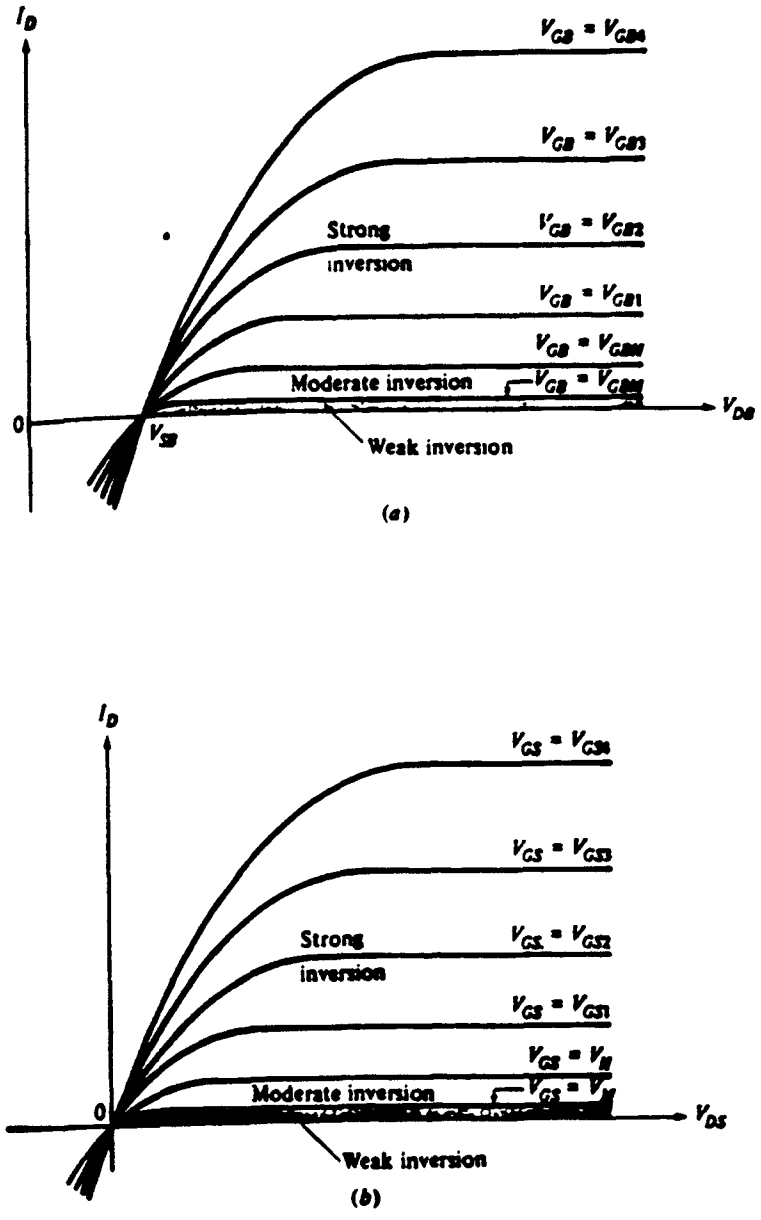


Figure 4.6: Current voltage characteristics, where V_{SB} is assumed fixed.

Transistor regions of operation

Region	Channel condition
Strong inversion	The most heavily† inverted channel end is in strong inversion
Moderate inversion	The most heavily† inverted channel end is in moderate inversion
Weak inversion	The most heavily† inverted channel end is in weak inversion

† If both ends are equally inverted, either end can be considered.

Figure 4.7: Transistor regions of operations

4.4.1 A general charge sheet model

We shall derive an expression for the drain current valid in all regions of operation, in this section. A key to the generality of the results we are about to develop is the recognition of the fact that the current in the channel can be caused by the both drift and diffusion. Thus, let x be the horizontal position in the channel and measured from the source end. If the inversion layer current at x is denoted by I(x), we will have

$$I(x) = I_{drift}(x) + I_{diff}(x) \tag{4.15}$$

We should remember that we are trying to develop a hypothetical model for region of transistors operation. We can write an expression for the drift component by considering a small element between x and $x + \Delta x$ in the inversion layer in fig 4.1, as shown magnified in fig. 4.5. The potential difference across this element under consideration is

$$\Delta\, \psi_S(x) = \psi_S(x + \Delta x) - \psi_S(x) \tag{4.16}$$

We shall replace bulk mobility μ_B with the surface mobility μ_S which is smaller value because the electrons move with difficulty parallel to the surface due to the

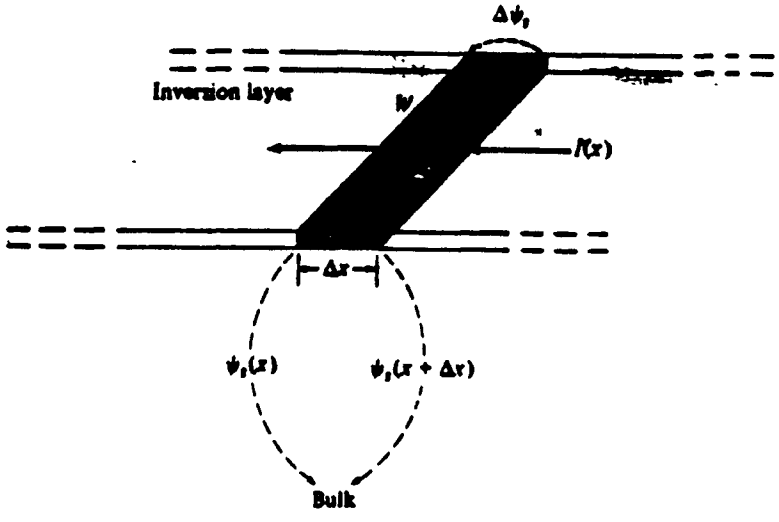


Figure 4.8: Small element of inversion layer in the device of Fig.3.1

horizontal field(the semiconductor - oxide interface), being pulled toward it by the vertical field.

$$I_{drift} = \mu(-Q'_I)\frac{W}{\Delta x}\Delta\psi_S(x) \tag{4.17}$$

where, $Q'_I = \frac{dQ_I}{dA}$, is the inversion layer charge per unit area (negative) at x. As Δx approaches zero,

$$I_{drift}(x) = \mu W(-Q'_I)\frac{d\psi_S}{dx}. \tag{4.18}$$

The diffusion current component can be obtained as:

$$I_{diff}(x) = \mu W U_T \frac{dQ'_I}{dx} \tag{4.19}$$

In d.c. state ,

$$I_D = \mu W(-Q'_I)\frac{d\psi_S}{dx} + \mu W U_T \frac{dQ'_I}{dx}. \tag{4.20}$$

Let the surface potential at the source end of the channel (x=0) be denoted by ψ_{s0} and Q'_I by the $Q'_{I,source}$. Corresponding quantity at the drain end of channel (x=L) by ψ_{sL} and $Q'_{I,drain}$.

$$\begin{aligned} \int_0^L I dx &= W\int_{\psi_{s0}}^{\psi_{sL}} \mu(-Q'_I)d\psi_s + WU_T\int_{Q'_{I,source}}^{Q'_{I,drain}} \mu dQ'_I \\ I &= \frac{W}{L}\left[\int_{\psi_{s0}}^{\psi_{sL}} \mu(-Q'_I)d\psi_s + U_T\int_{Q'_{I,source}}^{Q'_{I,drain}} \mu dQ'_I\right]. \\ I &= I_{drift} + I_{diffusion} \end{aligned} \tag{4.21}$$

If we assume μ is constant along the channel,

$$I_{drift} = I_{D1} = \frac{W}{L}\mu\int_{\psi_{s0}}^{\psi_{sL}}(-Q'_I)d\psi_s \tag{4.22}$$

$$I_{diff} = I_{D2} = \frac{W}{L}\mu U_T(Q'_{I,drain} - Q'_{I,source}) \tag{4.23}$$

Having developed the basic drift and diffusion current models, we can apply these models to define the regions of operation as in fig 4.7; $logI_D vs V_{GB}$.

At strong inversion, from the figure, it is seen that $I_D = I_{D1}$, which is mainly due to the presence of drift.

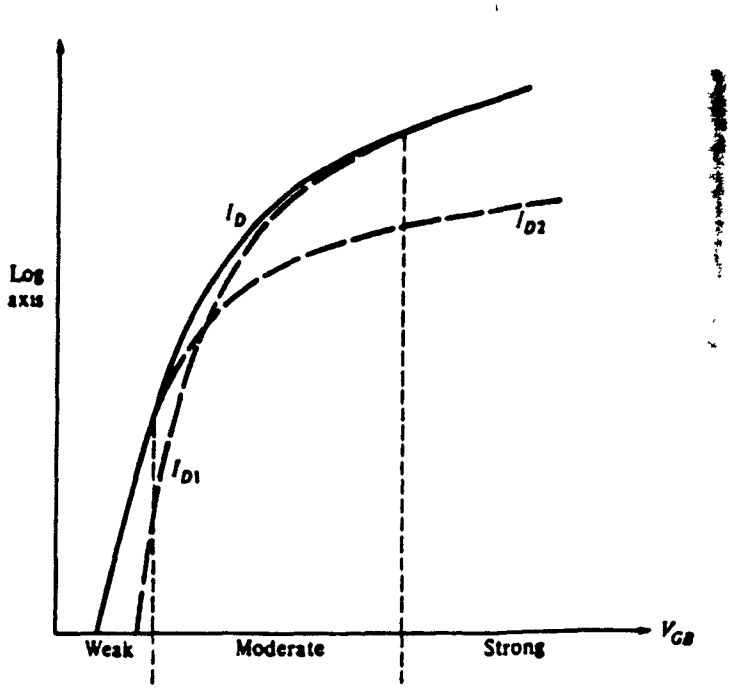


Figure 4.9: $I_D vs V_{GB}$

At weak inversion, from the figure, it is seen that $I_D = I_{D2}$, which is mainly due to the presence of diffusion.

However in moderate inversion both the drift and the diffusion component, I_{D1} and I_{D2} resply., play an important role in the transistor operation.

4.5 Simple Model In Weak Inversion

Let us make the following assumptions [10].

1. The channel is sufficiently long so that the gradual channel approximation can be used and channel-length modulation effects are negligible.

2. Generation currents in the drain, channel and source depletion regions are negligible; source and drain currents are then equal.

3. The density of fast surface states and the fluctuations of surface potential are negligible.

The basic derivation of Barron [11] may then be used and can be easily extended to the case of nonzero source-to-substrate voltage. His approximate expression for the weak inversion current may then be rewritten, for an channel transistor, as

$$I_D = S\mu U_T^2 \left(\frac{1}{2} q\epsilon_s n_i\right)^{1/2} e^{(3\phi/2U_T)} \cdot \frac{e^{\psi_s/U_T}}{(\psi_s - U_T)^{1/2}} \cdot (e^{-(V_S/U_T)} - e^{-(V_D/U_T)} \qquad (4.24)$$

where

S = geometrical shape factor of the transistor (effective width over effective length of the channel),

μ = mobility of carriers in the channel,

U_T = KT/q,

ϵ_s = permittivity of Si,

$\phi = U_T \ln(N_B/n_i)$ bulk Fermi potential,

N_B = constant bulk impurity concentration,

n_i = intrinsic carrier concentration,

ψ_s = surface potential, constant along the channel in weak inversion,

V_S = source-to-substrate voltage,

V_D = drain-to-substrate voltage,

V_G = gate-to-substrate voltage, and

I_D = drain current

It is valid for

$$4U_T + \phi + V_S < \psi_s < 2\phi + V_S \qquad (4.25)$$

that is within a range $\phi - 4U_T$ below the value $2\phi + V_S$ for which strong inversions starts at the source end of the channel.

On the other hand, the surface depletion capacitance C_d can be expressed as

$$C_d = \left(\frac{\frac{1}{2}\epsilon_s q n_i}{\psi_s - U_T}\right)^{1/2} e^{\phi/2U_T}. \tag{4.26}$$

It may be inserted into Eqn (4.19), which yields,

$$I_D = S\mu U_T^2 C_d e^{-(2\phi/U_T)} e^{\psi_s/U_T} \left(e^{-(V_S/U_T)} - e^{-(V_D/U_T)}\right) \tag{4.27}$$

Due to the very slow variation of C_d with ψ_s, I_D is essentially depending exponentially on ψ_s/U_T.

Variations of the gate-to-substrate voltage V_G are shared between the oxide capacitance per unit area Cox and the semiconductor total surface capacitance per unit area C_s. Therefore,

$$\frac{\partial \psi_s}{\partial V_G} = \frac{C_{ox}}{C_{ox} + C_s} = 1 - \frac{C_G}{C_{ox}} \tag{4.28}$$

where C_G is the gate capacitance per unit. Fig. 4.8 shows typical normalized $C_G - V_G$ curves calculated at the source end of the channel by assuming a negligible density of fast surface states. The first part of the curves corresponding to a decrease of C_G with increasing V_G is valid for the whole channel as long as $V_D \geq V_S$.

Corresponding values of the surface potential ψ_s have been reported along the curves. It can be seen that C_G is fairly constant for

$$4U_T + \phi + V_S < \psi_s < 2\phi + V_S - 2U_T \tag{4.29}$$

that is within a range $\Delta\psi_s = \phi - 6U_T$ of ψ_s included in the limits of validity Eqn (4.20) to Eqn (4.22), which corresponds to more than three orders of magnitude for I_D if $\phi \geq 13U_T$

According to Eqn (4.23), ψ_s is linearly depending on V_G inside this range and Eqn (4.24) takes the simple form

$$I_D = SI_{DO} e^{V_G/nU_T} \left(e^{-(V_S/U_T)} - e^{-(V_D/U_T)}\right) \tag{4.30}$$

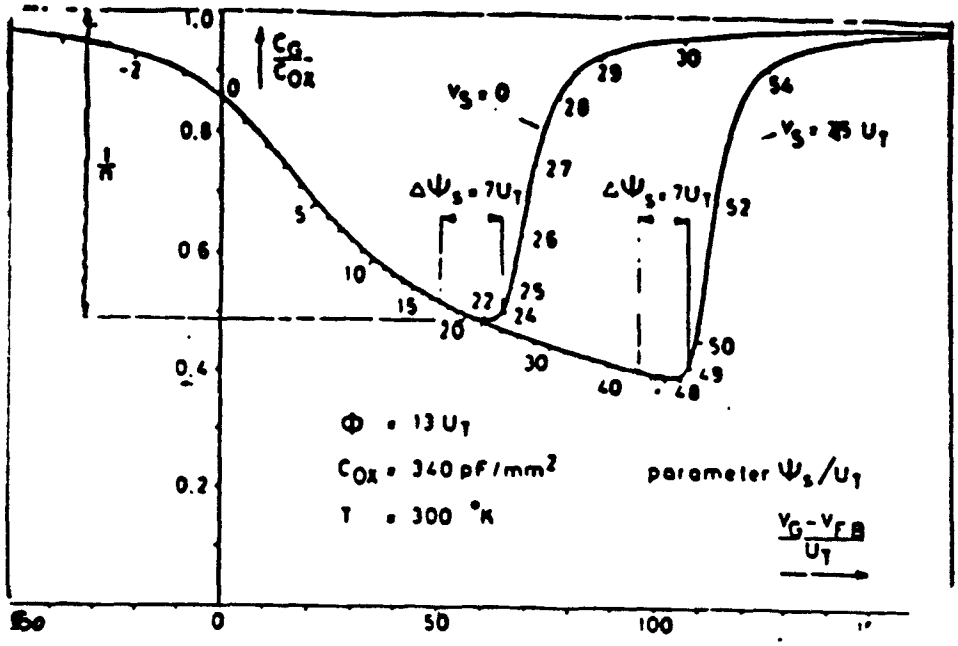


Figure 4.10: Normalized $C_G - V_G$ curve at the source end of the channel calculated for typical parameters. The range $\Delta\psi_S$ of surface potential corresponding to weak inversion operation is located at the minimum of the curve. The slope factor n is closely related to the value of this minimum

where I_{DO} is a characteristic current and n a slope factor.

As a negligible density of fast surface states is assumed, C_s is equal to C_d within the range of interest and eqn (4.28) yields the slope factor.

$$n = 1 + \frac{C_d}{C_{ox}} \tag{4.31}$$

As shown in Fig.4.8, n can be evaluated at the minimum of the $C_G - V_G$ based on drain current ratios, as is common practice for bipolar circuits. On the contrary, n is reproducible parameter available for circuit design.

$$\begin{aligned} n &= \frac{1}{1-(\frac{C_G}{C_{ox}})_{min}} \\ &= 1 + \frac{1}{C_{ox}}\left(\frac{qN_B\epsilon_S}{2(2\phi - 5U_T + V_T)}\right)^{1/2} \end{aligned} \tag{4.32}$$

As shown by Eqn (4.27), n takes different values for transistors biased by widely different values of V_S. The same is true for I_{DO}, so that the technique of drain current ratios can only be applied to transistors with differential values of V_S not

exceeding a few U_T, which is not a real limitation to design flexibility.

Eqn (4.30) is seen to be symmetrical in V_D and V_S, as can be expected from the symmetrical structure of the device. It is applicable to p-channel transistors as well by changing the signs of V_G, V_S, and V_D. The transconductance in weak inversion is

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{I_D}{nU_T}. \tag{4.33}$$

For $V_D - V_S \gg U_T$, a source transconductance can be defined as

$$g_{ms} = \frac{\partial I_D}{\partial V_S} = \frac{I_D}{U_T} \tag{4.34}$$

The upper limit of validity for Eqn (4.30) is obtained by introducing in Eqn (3.22) the upper limit of ψ_s given by Eqn (4.24) and by replacing C_d by its value taken from Eqn (4.26); this yields, for $V_D - V_S > 3U_T$(saturated drain current)

$$I_D \leq \frac{n-1}{e^2} S\mu C_{ox} U_T^2. \tag{4.35}$$

The minimum value of S ensuring weak inversion operation can be calculated from this relation; the factor (n - 1)/e^2 can be dropped if a rough order of magnitude is all that is needed, so that this upper limit is a direct function of the strong inversion transfer parameter.

$$\beta = S\mu C_{ox} \tag{4.36}$$

The model of Eqn (4.30) is therefore still valid, with an increased and less controllable value of n.

The influence of surface states is negligible as long as $qN_{ss} \ll C_d + C_{ox}$. This condition is always fulfilled for $N_{ss} \ll 2 \cdot 10^{11} cm^{-2} ev^{-1}$ if the oxide thickness does not exceed 120nm.

4.6 PTAT, voltage sources

Bandgap voltage references [12] are widely used in bipolar technology where they reach very high standards of accuracy and stability. Their principle relies on the fact that the voltage V_J across p - n junction that is forward biased by a constant current increases fairly linearly with decreasing temperature, and tends toward the bandgap value V_{GO} when the absolute temperature is extrapolated to 0. If a voltage that is proportional to absolute temperature (PTAT) is added to V_J to exactly compensate the difference between V_J and V_{GO}, one obtains a total voltage that is independent of temperature.

The realization of a bandgap reference in MOS technology has long been hindered by the difficulty of realizing a PTAT voltage. Solutions to this problem may be found by considering the behavior of a MOS transistor in weak inversion. For a negligible density N_{SS} of fast surface states, the drain current in weak inversion may be expressed as in previous subsection.

$I_D = SI_{Do}e^{V_G/nU_T}\left(e^{-(V_S/U_T)} - e^{-(V_D/U_T)}\right)$

where S is the effective geometrical shape factor of the transistor; $V_G, V_S, and V_D$ are the gate, source, and drain potentials with respect to the substrate, and U_T = kT/q. The slope factor n is fairly controllable, whereas the characteristic current I_{DO} is very sensitive to process and temperature.

This relation is valid below the weak inversion limit, which may be expressed as [10]

$$I_D \ll \beta U_T^2 \tag{4.37}$$

where β is the well-known strong inversion transfer parameter.

A PTAT voltage source based on the exponential $I_D - V_G$ characteristics included in Eqn (4.30) has been used in a CMOS bandgap reference circuit; a voltage proportional to nU_T was extracted as the voltage difference across two stacks

of three diode-connected transistors ($V_S = 0, V_D = V_G$) having different values of I_D/S. A slightly parabolic temperature dependence was observed, mainly due to the nonnegligible variation of the slope factor n with temperature. Furthermore, the need to sum up three gate-to-source voltages is not compatible with low-voltage operation.

It is interesting now to compare the MOS transistor in weak inversion with a bipolar transistor having high-value direct and inverse gains. By using the simple fundamental Ebers-Moll model assuming ideal junctions, the collector current may be expressed as

$$I_C = I_S \left(e^{V_{BE}/U_T} - e^{-V_{BC}/U_T} \right) \tag{4.38}$$

comparison of eqn (4.30) and eqn (4.38) shows that a MOS transistor in weak inversion is equivalent to a bipolar transistor with the additional possibility of adjusting the characteristic current I_S by means of the gate voltage V_G.

4.6.1 Principle of the reference

Fig. 4.11 shows the block diagram of the CMOS voltage reference supplying an output voltage V_R. The diode voltage V_J is obtained across the base-emitter junction of a bipolar substrate transistor T_S which is available in any CMOS technology by using the n-type substrate as the collector, a p-type well as the base, and n_+ diffusion as the emitter. This transistor is biased by a constant current source I_E which does not have to be more accurate than about percent. The current reference may thus be an n-channel transistor with gate-source voltage equal to V_R.

The PTAT source supplies a voltage V_2, which is compared to

$$V_1 = \frac{R_2}{R_1 + R_2} \cdot V_R - V_J \tag{4.39}$$

by a differential amplifier A. The output S of this differential amplifier drives the

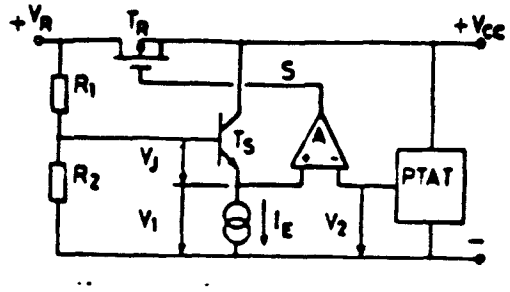


Figure 4.11: Block diagram of the bandgap voltage reference.

gate of the p-channel regulating transistor T_R. The loop is at equilibrium at

$$V_R = \left(1 + \frac{R_1}{R_2}\right)(V_J + V_2) \tag{4.40}$$

which is independent of temperature, according to the bandgap reference scheme, if

$$V_J + V_2 = V_{GO} \tag{4.41}$$

at any temperature.

The reference voltage V_R may be adjusted to any value above V_{GO} by properly choosing the ratio R1/R2. The resistors can be implemented by means of p-well strips, and binary weighted pads may be provided for final adjustments.

4.6.2 Realization of the PTAT source.

The basic cell of a novel PTAT voltage source,[12], is shown in Fig. 4.12. The two transistors T_a *and* T_b are in the same p-well, which may be connected to the source of T_a or to any more negative potential. If both transistors operate in weak

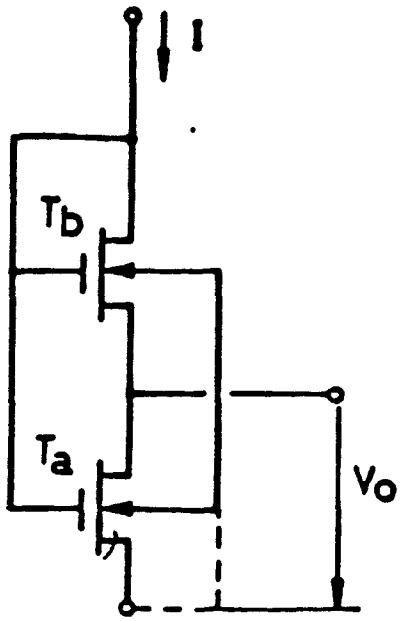


Figure 4.12: Elementary PTAT voltage source. Both transistors must operate in weak inversion.

inversion, Eqn (4.25) may be applied, which yields

$$V_o = U_T \ln\left(1 + \frac{S_b}{S_a}\right) + \Delta V_o \tag{4.42}$$

This result is independent of the current I flowing through the transistors, as long as this current is smaller than the weak inversion limit and much larger than the leakage currents. Furthermore, the common gate potential must exceed that of the intermediate point by 3 or $4U_T$ in order to maintain T_b in saturation. Again, an offset voltage ΔV_o is added because of the mismatch of the two transistors. By adding ΔV_{Gn} to the gate voltage of transistor T_b, ΔV_o is found to be equal to $\Delta V_{Gn}/n_n$ for $S_b \gg S_a$.

Experimental results on this cell with $S_b/S_a = 10$ are reported in Fig 4.12 for various values of current I. The dimensions of transistor T_a corresponds to $\beta_a U_T^2$=20nA.

Up to about 40°C, measurements for currents ranging from 30 pA to 1 nA all coincide on the same straight line; this line is fairly parallel to the theoretical behavior with an offset ΔV_o of about 3 mV. Due to the effect of leakage currents,

temperature dependance of the reference current at a high temperature and will prevent thermal runaway.

4.8 Circuit Realisation and Experimental Results

Complete schematic of the current reference is Fig. 4.16. It is detailed version of fig (4.15), the transistors $M_{n,p1} - M_{n,p2}$ from the reference circuit, $M_{n4} - M_{n13}$ from the voltage source. Current through the PTAT voltage sources are derived from the reference current through $M_{p3} - M_{p8}$. To obtain low supply and load regulation sensitivities, cascade transistors M_{p9} and M_{p10} are added to the current mirror.

We have to address the problem of Bistable operating point [5]. Although this operating point is theoretically unstable, it can cause a stable latch up state due to leakage currents. To avoid this a stable latch up network must be added. In this circuit, no separate start up network is added, however, start up is made available externally.

The current was measured in the temperature range $-55\ to\ 125°C$, the results are available in Chapter 5 in form of spice output.

Chapter 5

Integrated Magnetic Field Sensor, with temperature compensated bias current.

5.1 Introduction

The MFS are fabricated without additional processing steps in CMOS technology. The MFS, we have designed is with temperature compensated current reference circuit for bias and with a diode connected load.

5.2 Circuit Design in CMOS Technology

The circuit of CMOS MFS is shown in Fig. 5.1. Here the sensor consists of

- current reference circuit
- biasing transistor
- Dual drain magfet.

Transistor MN_1, MN_2, MP_1, MP_2 forms current reference to the circuit, MN_{14} forms the bias arrangement for the transistor, MN_{15} *and* MN_{16} the dual drain MAGFET, MN_{17} *and* MN_{18} forms the diode connected load.

Separate P wells for the PTAT voltage sources, the biasing transistors MN_{14}, the diode connected load MN_{17}, MN_{18} and dual drain MOSFET, MN_{15} *and* MN_{16}; to avoid back gate effects. In the current reference circuit, MP_9 and MP_{10}, are cascoded p channel devices which keep the drain voltages of MN_1 and MN_2 constant, thereby reducing the channel length modulations effects. Transistors MN_3 and MP_3 form the gain stage to reduce the reference current to 1nA as to keep the PTAT voltage sources in weak inversion.

MN_{14}, biasing transistor to the MAGFET, designed as current multiplier. The diode connected loads, in effect are designed to have 100 K ohms, any increase in the resistance value shall increase the channel length therby affecting the frequency response of the device.

5.2.1 Circuit Simulation and Layout

The circuit was simulated by HSPICE circuit simulation packages; with nodal parameters of Siemens. The objective of simulation are:

1. To determine the dc operating conditions over -55 to 125°C
2. To evaluate the effectiveness of the temperature compensated bias current,
3. To determine the incremental output impedance and finally,
4. To estimate the frequency response limitation imposed by the circuit arrangement.

The circuit simulated with model points is given in Fig. 9.1 [App C]. To simulate the dual drain MAGFET we split the single device with same length and half the width of the existing MAGFET, and connected the gates of devices.

To determine the dc conditions, the dc operation was carried out in the temperature range -55 to 125°C. To determine, secondly, the I_{ref} vs Temperature

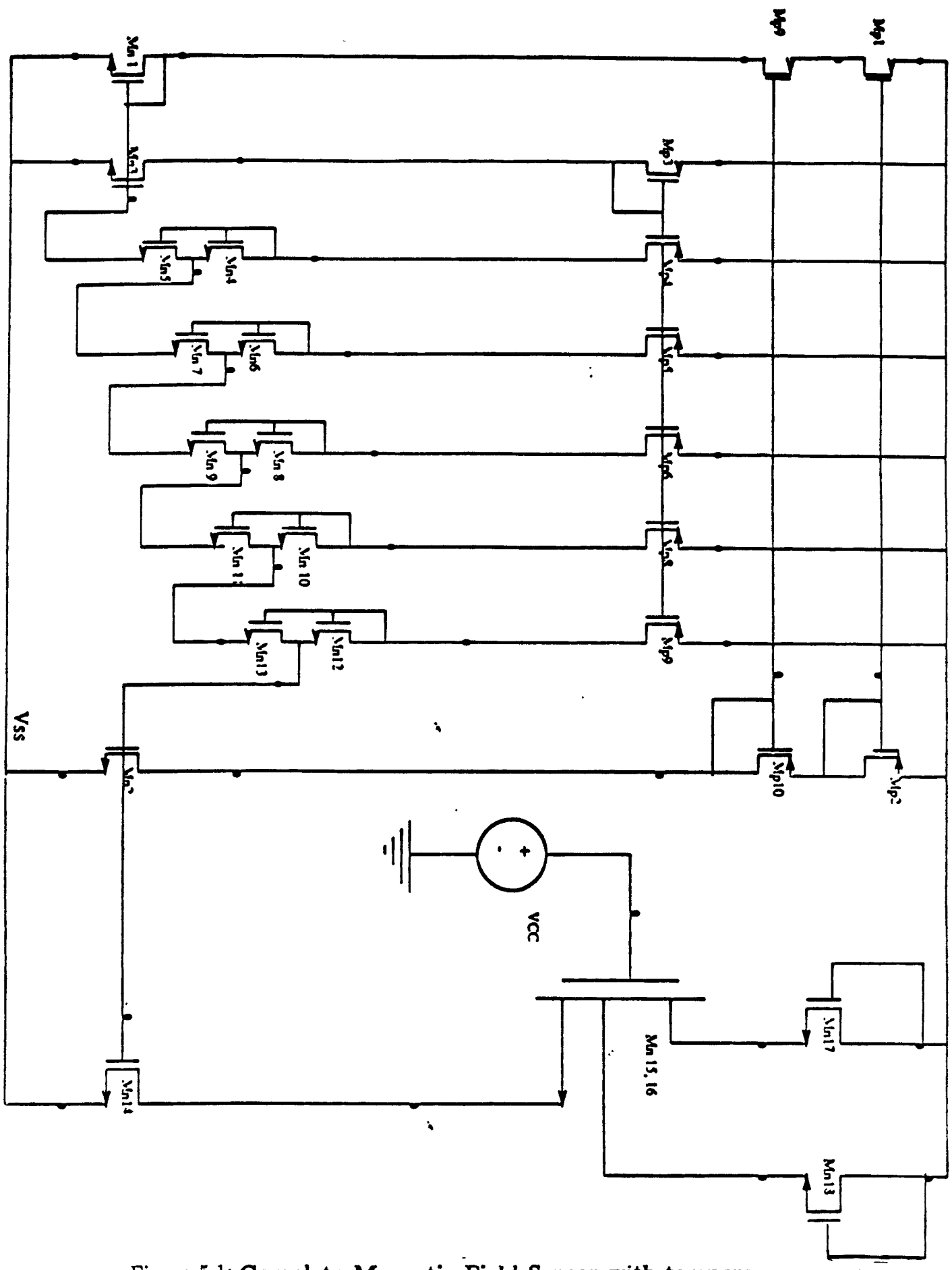


Figure 5.1: **Complete Magnetic Field Sensor with temperature compensated Current reference.**

and find variation of current to the temperature. The small signal and various temperature was observed. Thirdly, to find the small signal output impedance of MAGFET differential pair, with diode connected loads, the bias voltages were chosen to keep all the devices in saturation. Finally, to verify the ability of circuit to serve the time varying magnetic field, the frequency response was estimated. To determine this, an ac signal was applied to the input and the output was observed as a function of frequency. Both magnitude and phase response was obtained.

5.2.2 Model Parameters

The circuit was simulated using level2 parameters in HSPICE. Model parameters have been modified by Siemens Corporate Research for typical MOSIS design rules and are set to give accurate results for this process, for defined channel length. The model parameters for some typical values can be referred from Appendix C.

5.2.3 Layout

Schematic capture was done using MAGIC cad tool, using standard $2\mu m$ CMOS P-Well Technology with help of MOSIS design rules. The chip was fabricated at ORBIT fab facilities. Starting with n -substrate, the p-wells are formed to implement n-channel transistors. The p-channel transistors are formed on the n-substrate itself.

5.3 Output Analysis

From the DC analysis, the operating conditions over the temperature range $-55°C to 125°C$ was evaluated. It was observed that all the transistors were operating in saturation. Also, I_{Bias}, the output current of current reference, was almost linearly proportional to temperature. A curve fiiting analysis on the output characteristic was done,

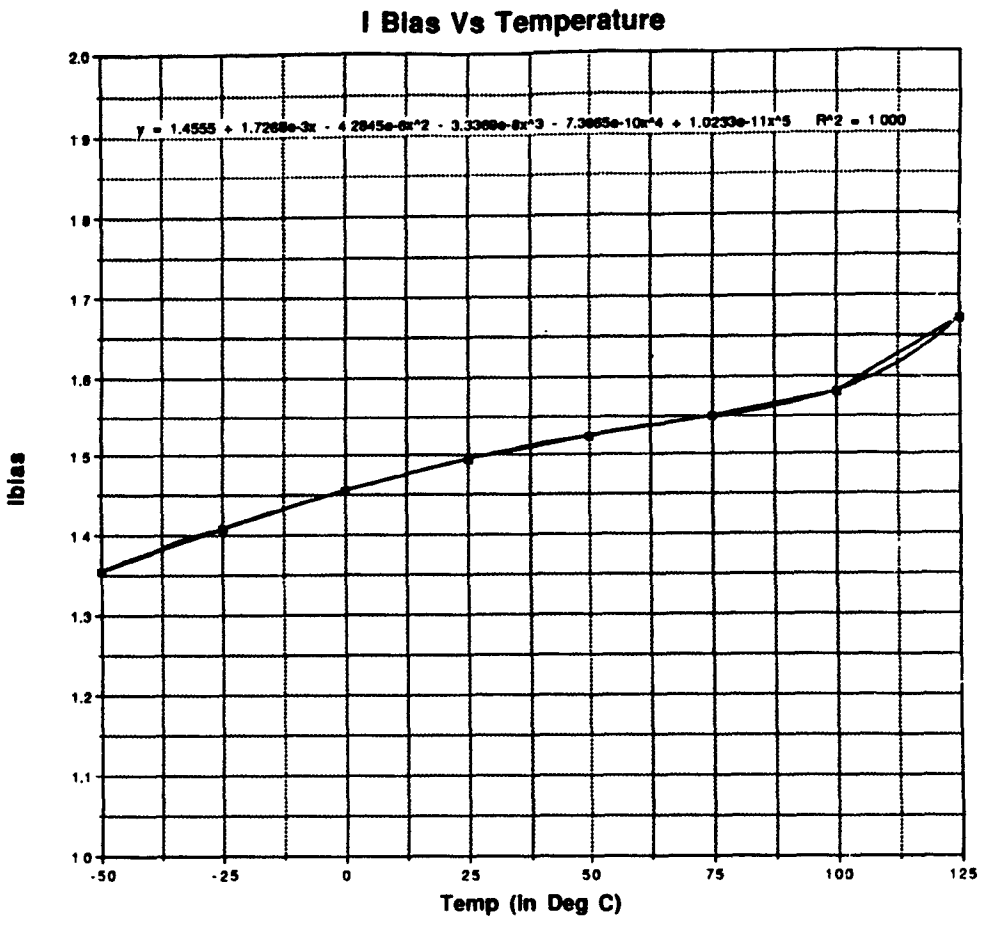


Figure 5.2: I_{Bias} **Vs Temperature**

which further reduces to the form $I_{Bias}pplT$. The output characteristic is shown in the fig 5.3.

Similarly, for the given temperature the PTAT voltage source (V_{PTAT}) was found to vary liearly with the temperature as shown in fig 5.4.

However, due to the early voltage effect V_A, there was a small mismatch observed between I_{ref} and I_{Bias}, as shown in the fig 5.5.

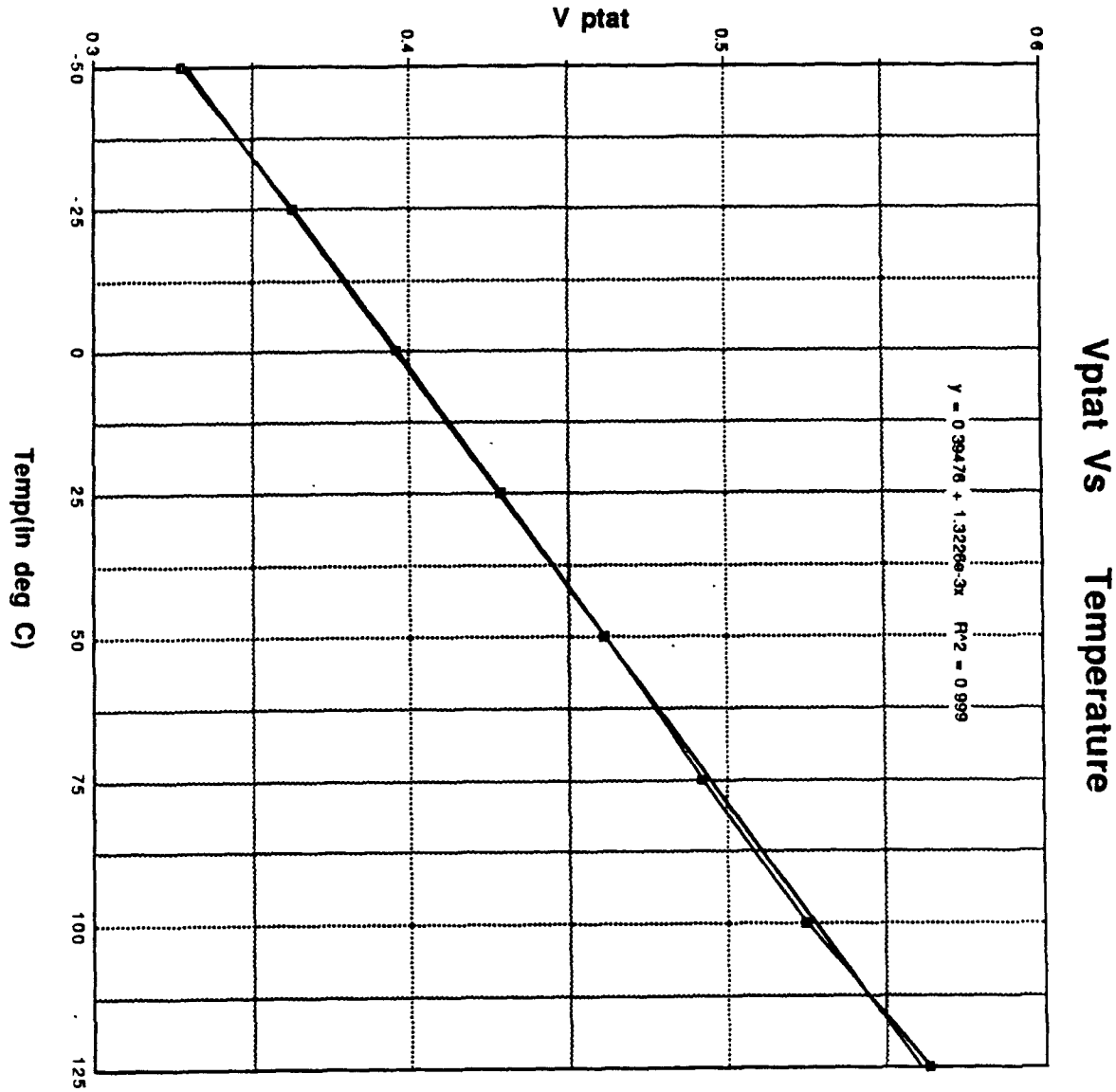


Figure 5.3: V_{PTAT} **Vs Temperature.**

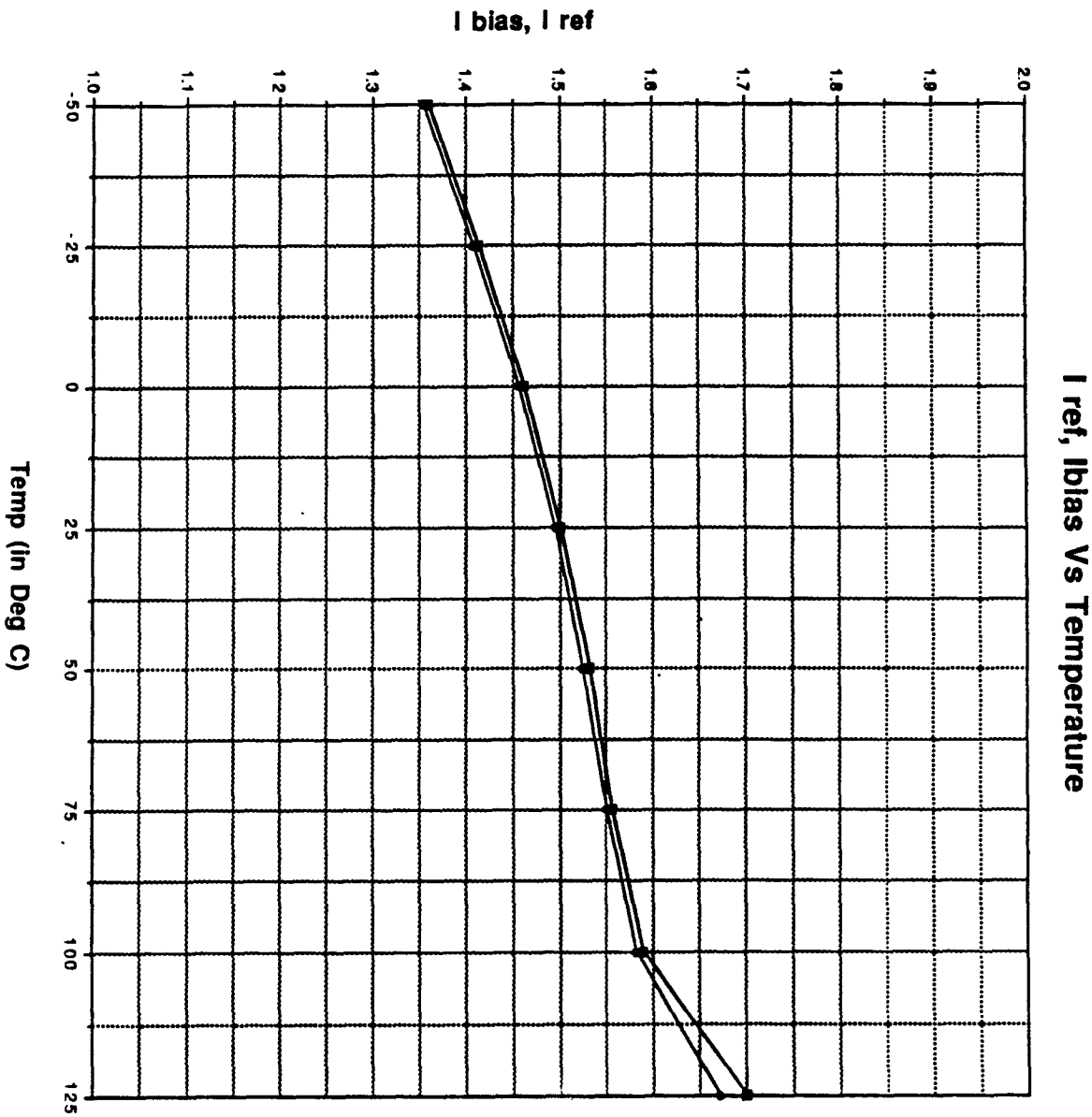


Figure 5.4: Mismatches bet $I_{ref} and I_{Bias}$ Vs Temperature.

Chapter 6

Conclusion

In this thesis, a novel CMOS magnetic field sensor, has been implemented using earlier models. It has been observed from the theoretical expression that sensitivity of MAGFET can be improved considerably using temperature independent biasing circuitry. A temperature compensated CMOS current reference has been developed and tested. From the results, it can be compared that this current reference has a current $I\alpha T$ and can be implemented with less number of devices than the earlier version. In general the circuit behavior is in agreement with theoretical equations.

While testing the sensor, a severe latch up problem has been observed. This is attributed to fact that since PTAT working in weak inversion were laid in P Well, care must be taken by laying out the PTATs' and also following the precautions for latch up. The above design, is expected to give very good sensitivity to the sensor. The current reference can be used in most amplifier biasing applications and also for current comparators.

Appendix A

Evaluation of Current Reference

We shall derive the basic equation for the PTAT, which is given in Fig 4. , consisting of transistors A and B.

Condition:

$$\begin{aligned} V_{Ga} &= V_{Gb} \\ V_{Sa} &= 0 \\ V_{Sb} = V_{Da} &= V_o. \end{aligned} \tag{A.1}$$

Assumption: $V_{Db} \gg U_T$, to keep T_b in saturation;

therefore $I_a = I_b$.

$$S_a I_{Do} e^{\frac{V_{Ga}}{nU_T}} [e^{\frac{-V_{Sa}}{U_T}} - e^{\frac{-V_{Da}}{U_T}}] = S_b I_{Do} e^{\frac{V_{Gb}}{nU_T}} [e^{\frac{-V_{Sb}}{U_T}} - e^{\frac{-V_{Db}}{U_T}}]. \tag{A.2}$$

We know that $I_{Do} e^{\frac{V_{Ga}}{nU_T}} = I_{Do} e^{\frac{V_{Gb}}{nU_T}}$, hence we have:

$$S_a [e^{\frac{-V_{Sa}}{U_T}} - e^{\frac{-V_{Da}}{U_T}}] = S_b [e^{\frac{-V_{Sb}}{U_T}} - e^{\frac{-V_{Db}}{U_T}}]. \tag{A.3}$$

We know $e^{\frac{-V_{Db}}{U_T}} = 0$; since $V_{Db} \gg U_T$, we can write the above equation as:

$$S_a [e^{\frac{-V_{Sa}}{U_T}} - e^{\frac{-V_{Da}}{U_T}}] = S_b [e^{\frac{-V_{Sb}}{U_T}}]. \tag{A.4}$$

since $V_{Sa} = 0$, we can simplify the above equation to

$$S_a [1 - e^{\frac{-V_{Da}}{U_T}}] = S_b [e^{\frac{-V_{Sb}}{U_T}}]. \tag{A.5}$$

$$S_a - S_a e^{\frac{-V_{Da}}{U_T}} = S_b[e^{\frac{-V_{Sb}}{U_T}}]. \tag{A.6}$$

Dividing both sides by $e^{\frac{-V_{Da}}{U_T}} = 0$, we have

$$S_a e^{\frac{V_{Da}}{U_T}} - S_a = S_b e^{\frac{-V_{Sb}}{U_T} + \frac{V_{Da}}{U_T}}. \tag{A.7}$$

Since, $V_{Sb} = V_{Da}$, above equation reduces as

$$S_a(e^{\frac{V_{Da}}{U_T}} - 1) = S_b \tag{A.8}$$

$$e^{\frac{V_{Da}}{U_T}} - 1 = \frac{S_b}{S_a} \tag{A.9}$$

$$e^{\frac{V_{Da}}{U_T}} = \frac{S_b}{S_a} + 1 \tag{A.10}$$

$V_{Sb} = V_{Da} = V_o$ is the condition we have defined earlier, hence

$$e^{\frac{V_o}{U_T}} = \frac{S_b}{S_a} + 1 \tag{A.11}$$

Simplifying,

$$\frac{V_o}{U_T} = \ln[\frac{S_b}{S_a} + 1] \tag{A.12}$$

So finally, we have the V_{PTAT} :

$$V_o = U_T \ln[\frac{S_b}{S_a} + 1] \tag{A.13}$$

Appendix B

An Analysis of the Current Reference

From the fig 4. ; we can write the saturation current equations for the transistors.

$$I_1 = K_1(V_{GS1} - V_{T1})^2 \tag{B.1}$$

$$I_2 = K_2(V_{GS2} - V_{T2})^2 \tag{B.2}$$

$$I_3 = K_3(V_{GS3} - V_{T3})^2 \tag{B.3}$$

$$I_4 = K_4(V_{GS4} - V_{T4})^2 \tag{B.4}$$

In the above equations; $K_{1,2,3,4} = \frac{K_{Px}}{2}\frac{W}{L}$, where x = 1, 2, 3, 4

Now,

$$V_{GS2} = V_{T2} + \sqrt{\frac{I_2}{K_2}} \tag{B.5}$$

We have from the figure that

$$V_{GS1} = V_{GS2} + V \tag{B.6}$$

Hence eqn .1 becomes

$$I_1 = K_1(V_{GS2} + V - V_{T1})^2 \tag{B.7}$$

Substituting eqn in eqn

$$I_1 = K_1(V_{T2} + V + \sqrt{\frac{I_2}{K_2}} - V_{T1})^2 \tag{B.8}$$

Since $I_2 = I_4$, substituting the eqn .4 in eqn .7 we have,

$$I_1 = K_1 \left(V_{T2} + V - V_{T1} + \sqrt{\frac{K_4(V_{GS4} - V_{T4})^2}{K_2}} - V_{T1} \right)^2 \tag{B.9}$$

Substitute for $V_{GS4} = V_{GS3}$ in eqn .8

$$I_1 = K_1 \left(V_{T2} + V - V_{T1} + \sqrt{\frac{K_4(V_{T3} + \sqrt{\frac{I_3}{K_3}} - V_{T4})^2}{K_2}} \right)^2 \tag{B.10}$$

where $V_{GS3} = V_{T3} + \sqrt{\frac{I_3}{K_3}}$.

Since, $V_{T4} = V_{T3}$, we can reduce the above equation as

$$\frac{I_1}{K_1} = \left(V + V_{T2} - V_{T1} + \sqrt{\frac{K_4 I_3}{K_2 K_3}} \right)^2 \tag{B.11}$$

Since $I_3 = I_1$, substituting,

$$\frac{I_1}{K_1} = \left(V + V_{T2} - V_{T1} + \sqrt{\frac{K_4 I_1}{K_2 K_3}} \right)^2 \tag{B.12}$$

$$\left(\frac{I_1}{K_1} \right)^{\frac{1}{2}} = (V + V_{T2} - V_{T1}) + \sqrt{\frac{K_4 I_1}{K_2 K_3}} \tag{B.13}$$

$$\sqrt{I_1} = \sqrt{K_1}(V + V_{T2} - V_{T1}) + \sqrt{\frac{K_4 K_1}{K_2 K_3}} \sqrt{I_1} \tag{B.14}$$

Let us assume that,

$$\sqrt{m} = \sqrt{\frac{K_4 K_1}{K_2 K_3}} \tag{B.15}$$

$$\sqrt{I_1} - \sqrt{\frac{K_4 K_1}{K_2 K_3}}\sqrt{I_1} = \sqrt{K_1}(V + V_{T2} - V_{T1}) \tag{B.16}$$

$$\sqrt{I_1}(1 - \sqrt{m}) = \sqrt{K_1}(V + V_{T2} - V_{T1}) \tag{B.17}$$

Squarring on both sides,

$$I_1(1 - \sqrt{m}) = K_1(V + V_{T2} - V_{T1})^2 \tag{B.18}$$

$$I_1 = \frac{K_1(V + V_{T2} - V_{T1})^2}{(1 - \sqrt{m})^2} \tag{B.19}$$

Appendix C

Spice Simulation

```
.option post
****** copyright 1990 meta-software,inc. *****site:siemens_princeton
******  input listing                     evaluation expires 900930
******
   .width out=80
   * this simulation is complete  current reference with ptat of 300mv.
   *
    .model n10 nmos (vto=.90 uo=571 gamma=.605 phi=.65 lambda=.012
    +tox=40.0n cgso=.086n cgdo=.086n cgbo=.138n cj=.24m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.35u level=2 ucrit=9.17e4 uexp=.10
    +kf=2.00e-28 nfs=3.5e+11)
    .model n7  nmos (vto=.90 uo=571 gamma=.605 phi=.65 lambda=.02
    +tox=40.0n cgso=.086n cgdo=.086n cgbo=.138n cj=.24m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.35u level=2 ucrit=9.17e4 uexp=.10
    +kf=2.00e-28 nfs=3.5e+11)
    .model p10 pmos (vto=-.72 uo=215 gamma=.24 phi=.66 lambda=.017
    +tox=40.0n cgso=.259n cgdo=.259n cgbo=.138n cj=.25m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.45u level=2 ucrit=1.07e5 uexp=.23 vmax=2.e4
    +kf=.75e-28 nfs=4.5e+11)
    .model p7  pmos (vto=-.72 uo=215 gamma=.24 phi=.66 lambda=.026
    +tox=40.0n cgso=.259n cgdo=.259n cgbo=.138n cj=.25m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.45u level=2 ucrit=1.07e5 uexp=.23 vmax=2.e4
    +kf=.75e-28 nfs=4.5e+11)
    .model n5 nmos (vto=.90 uo=571 gamma=.605 phi=.65 lambda=.04
    +tox=40.0n cgso=.086n cgdo=.086n cgbo=.138n cj=.24m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.35u level=2 ucrit=9.17e4 uexp=.15 vmax=5.e4
    +kf=2.00e-28 nfs=3.5e+11)
    .model n4 nmos (vto=.90 uo=571 gamma=.605 phi=.65 lambda=.06
    +tox=40.0n cgso=.086n cgdo =.086n cgbo=.138n cj=.24m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.35u level=2 ucrit=9.17e4 uexp=.15 vmax=5.e4
    +kf=2.00e-28 nfs=3.5e+11)
    .model n3 nmos (vto=.90 uo=571 gamma=.605 phi=.65 lambda=.1
    +tox=40.0n cgso=.086n cgdo=.086n cgbo=.138n cj=.24m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.35u level=2 ucrit=9.17e4 uexp=.15 vmax=2.5e4
    +kf=2.00e-28 nfs=3.5e+11)
    .model p5 pmos (vto=-.72 uo=215 gamma=.24 phi=.66 lambda=.04
    +tox=40.0n cgso=.259n cgdo=.259n cgbo=.138n cj=.25m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.45u level=2 ucrit=1.07e5 uexp=.23 vmax=2.e4
    +kf=.75e-28nfs=4.5e+11)
    .model p3  pmos (vto=-.72 uo=215 gamma=.24 phi=.66 lambda=.13
    +tox=40.0n cgso=.259n cgdo=.259n cgbo=.138n cj=.25m mj=.4
    +js=1.0m pb=.9 xj=.0u ld=.45u level=2 ucrit=1.07e5 uexp=.23 vmax=.8e4
    +kf=.75e-28 nfs=4.5e+11)
    * the suggested delta_w is 0.21um
    *
    mn1  6  6  4  4  n10  w=20u l=50u
    mn2  5  18  4  4 n10 w=5u   l=50u
```

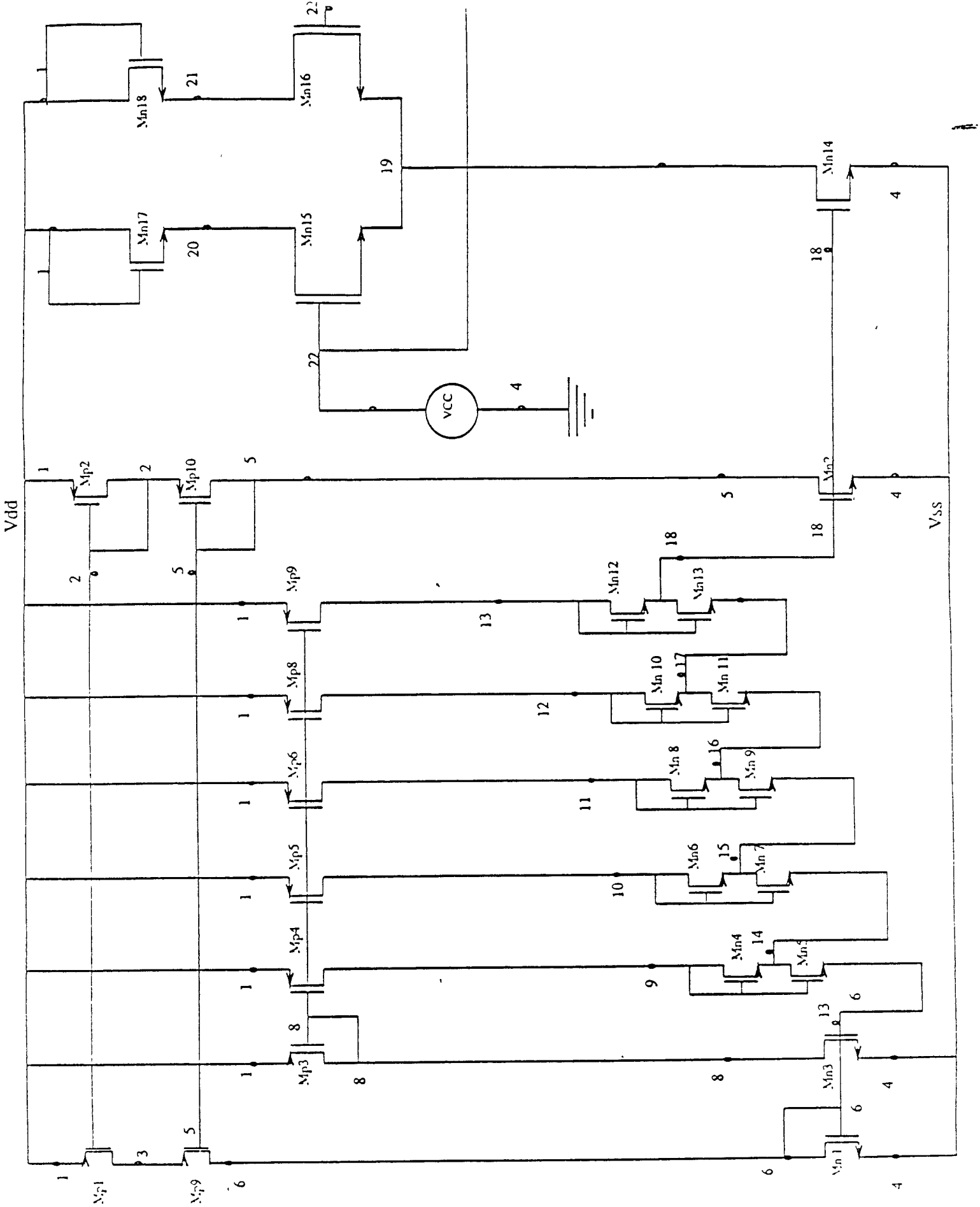


Figure C.1: MFS with nodal points

```
    mn3  8  6  4   4 n10 w=5u  l=400u
    mn4  9 9  14 6  n7  w=70u l=7u
    mn5  14 9  6 6  n7  w=35u  l=7u
    mn6  10 10 15 14  n7  w=70u l=7u
    mn7  15 10 14 14  n7  w=28u  l=7u
    mn8  11 11 16 15  n7   w=70u  l=7u
    mn9  16 11 15 15  n7   w=21u  l=7u
    mn10 12 12 17 16  n7  w=70u  l=7u
    mn11 17 12 16 16  n7  w=14u  l=7u
    mn12 13 13 18 17  n7  w=70u  l=7u
    mn13 18 13 17 17  n7  w=7u  l=7u
    mp1  3  2  1  1  p7   w=14u  l=7u
    mp2  2  2  1  1  p7  w=14u   l=7u
    mp3  8  8  1  1  p7  w=335u  l=7u
    mp4  9  8  1  1  p7  w=7u  l=7u
    mp5  10 8  1  1  p7  w=7u  l=7u
    mp6 11  8  1  1  p7  w=7u  l=7u
    mp7 12  8  1  1  p7  w=7u  l=7u
    mp8 13  8  1  1  p7  w=7u  l=7u
    mp9  6  5  3  3  p7  w=14u l=7u
    mp10 5  5  2  2  p7  w=14u l=7u
    mn14 19 18  4  4  n10 w=50u l=50u
    mn15 20 22 19 19 n10  w=20u l=40u
    mn16 21 22 19 19  n10 w=20u l=40u
    mn17 1   1  20 20 n10 w=15u l=80u
    mn18 1   1  21 21 n10 w=15u l=80u
    *
    vdd 1 0 dc  2.5
    vss 4 0 dc -2.5
    *
    *.temp -50c -25c 0c 25c 50c 75c 100c 125c
     .set dcon=1
     v22 22 0 dc 0.5
    .op
    .end
****** copyright 1990 meta-software,inc. *****site:siemens_princeton
******  mos   model parameters           tnom=  25.000 temp=  25.000
******
*******************************************************************************
*** common model parameters  model name:   0:n10      model type:nmos   ***
*******************************************************************************
    names  values   units     names  values   units     names  values   units
    -----  ------   -----     -----  ------   -----     -----  ------   -----
  1*** geometry parameters ***
      ld= 350.00n meters      lmlt=   1.00                wd=   0.    meters
    wmlt=   1.00                xl=   0.    meters        xw=   0.    meters

  2*** threshold voltage parameters ***
     vto= 900.00m volts         nss=   0.    1/cm**2      tpg=   1.00
     phi= 650.00m volts       gamma= 605.00m v**0.5       bulk=  gnd
   ngate=   0.    cm**3        nsub= 8.2e+15 1/cm**3    delvto=   0.    volts

  3*** gate overlap capacitance parameters ***
    cgbo= 138.00p f/meter     cgdo=  86.00p f/meter     cgso=  86.00p f/meter
    meto=   0.    meters

  4*** gate capacitance parameters ***
   capop=   2.00                cf1=   0.    volts        cf2= 100.00m volts
     cf3=   1.00  volts         cf4=  50.00               cf5= 666.67m
     cf6= 500.00                xqc= 500.00m              tox=  40.00n meters
```

```
   capop=   2.00                cf1=   0.     volts        cf2= 100.00m volts
     cf3=   1.00  volts         cf4=  50.00                cf5= 666.67m
     cf6= 500.00                xqc= 500.00m               tox=  40.00n meters
     cox= 863.29u f/m**2

   5*** diffusion parasitic parameters ***
      acm=   0.                  is=  10.00f amps           js=   1.00m a/m**2
      jsw=   0.    amp/m         nds=   1.00              cbd=   0.     farad
      cbs=   0.    farad          cj= 250.00u f/m**2      cjsw=   0.     f/m
       mj= 400.00m               mjsw= 330.00m             pb= 900.00m volts
      php= 900.00m volts           tt=   0.     secs       hdif=   0.     meters
     ldif=   0.    meters         rd=   0.     ohms         rs=   0.     ohms
      rsh=   0.    ohms/sq        fc=   0.                cjgate=   0.     farad
    alpha=   0.                   vcr=   0.     volts      rdc=   0.     ohms
      rsc=   0.    ohms            n=   1.00               vnds=  -1.00  volts

   6*** temperature effect parameters ***
     tlev=   0.                 tlevc=   0.                eg=   1.11  ev
     gap1= 702.00u ev/deg       gap2=   1.11k deg         xti=   0.
      bex=  -1.50                tcv=   0.     v/deg k     trd=   0.     /deg
      trs=   0.    /deg          cta=   0.     /deg        ctp=   0.     /deg
    lamex=   0.                  fex=   0.

   7*** noise parameters ***
       kf= 7.5e-29                af=   1.00              nlev=   2.00

   ***  level  2  model parameters  ***

    delta=   0.                ecrit=   0.     v/m        lambda= 130.00m /v
      nfs= 450.00g 1/cm**2     ucrit= 107.00k v/cm          uexp= 230.00m
     utra=   0.                   uo= 215.00 cm**2/vs       xj=   0.     meters
     neff=   1.00                vmax=   8.00k  m/sec      kp=  18.56u a/v**2
      mob=   0.
1 ******    h s p i c e      9001b          15: 5:40   9-dec90   apollo
 .option post
 ****** copyright 1990 meta-software,inc. *****site:siemens_princeton
 ******  operating point information      tnom=  25.000 temp=  25.000
 ******
 ***** operating point status is all      simulation time is     0.
    node    =voltage      node    =voltage      node    =voltage

 +0:1       =   2.5000  0:2       =   1.5008  0:3       =   1.4946
 +0:4       =  -2.5000  0:5       = 501.5995m 0:6       =  -1.1538
 +0:8       =   1.8917  0:9       =-405.8924m 0:10      =-320.2837m
 +0:11      =-234.6316m 0:12      =-148.9399m 0:13      = -63.2240m
 +0:14      =  -1.0682  0:15      =-982.4319m 0:16      =-896.6656m
 +0:17      =-810.8587m 0:18      =-725.0232m 0:19      =  -1.2723
 +0:20      = 172.3518m 0:21      = 172.3518m 0:22      = 500.0000m



 ****  voltage sources


 subckt
 element  0:vdd      0:vss      0:vcc
  volts      2.5000    -2.5000   500.0000m
  current  -17.6712u   17.6712u    0.
```

power 44.1779u 44.1779u 0.

total voltage source power dissipation= 88.3559u watts

**** mosfets

subckt element	0:mn1	0:mn2	0:mn3	0:mn4	0:mn5	0:mn6
model	0:n10	0:n10	0:n10	0:n7	0:n7	0:n7
id	1.5006u	1.4950u	48.1066n	1.0748n	5.3526n	1.0720n
ibs	0.	0.	0.	-8.568e-16	0.	-8.572e-16
ibd	-13.4617f	-30.0160f	-43.9174f	-7.4794f	-8.568e-16	-7.4787f
vgs	1.3462	1.7750	1.3462	662.2621m	747.9397m	662.1482m
vds	1.3462	3.0016	4.3917	662.2621m	85.6776m	662.1482m
vbs	0.	0.	0.	-85.6776m	0.	-85.7226m
vth	952.0203m	952.0203m	952.0203m	982.5935m	952.0203m	982.6091m
vdsat	333.8422m	668.1409m	333.8422m	38.1551m	37.9743m	38.1552m
beta	20.3258u	5.1862u	651.5899n	555.0589u	274.3236u	555.0576u
gam eff	605.0000m	605.0000m	605.0000m	605.0000m	605.0000m	605.0000m
gm	6.7856u	3.4651u	217.5282n	20.8929n	102.8938n	20.8397n
gds	18.3034n	18.6108n	609.3945p	21.7838p	107.2350p	21.7281p
gmb	2.2831u	1.0727u	73.1903n	6.2519n	33.7508n	6.2355n
cbd	0.	0.	0.	0.	0.	0.
cbs	0.	0.	0.	0.	0.	0.
cgs	569.1895f	142.2974f	1.1495p	20.9353f	9.6101f	20.9296f
cgd	3.2478f	1.2817f	10.5226f	6.0398f	8.4708f	6.0397f
cgb	18.0186f	8.1809f	77.8125f	111.8298f	56.3496f	111.8333f

subckt element	0:mn7	0:mn8	0:mn9	0:mn10	0:mn11	0:mn12
model	0:n7	0:n7	0:n7	0:n7	0:n7	0:n7
id	4.2764n	1.0693n	3.2029n	1.0666n	2.1322n	1.0639n
ibs	0.	-8.577e-16	0.	-8.581e-16	0.	-8.584e-16
ibd	-8.572e-16	-7.4780f	-8.577e-16	-7.4773f	-8.581e-16	-7.4763f
vgs	747.8708m	662.0340m	747.8003m	661.9189m	747.7257m	661.7993m
vds	85.7226m	662.0340m	85.7662m	661.9189m	85.8069m	661.7993m
vbs	0.	-85.7662m	0.	-85.8069m	0.	-85.8355m
vth	952.0203m	982.6242m	952.0203m	982.6383m	952.0203m	982.6482m
vdsat	37.9743m	38.1553m	37.9743m	38.1554m	37.9743m	38.1554m
beta	219.4590u	555.0563u	164.5944u	555.0550u	109.7297u	555.0537u
gam eff	605.0000m	605.0000m	605.0000m	605.0000m	605.0000m	605.0000m
gm	82.2061n	20.7867n	61.5711n	20.7339n	40.9887n	20.6813n
gds	85.6746p	21.6727p	64.1690p	21.6175p	42.7182p	21.5625p
gmb	26.9641n	6.2192n	20.1951n	6.2030n	13.4437n	6.1868n
cbd	0.	0.	0.	0.	0.	0.
cbs	0.	0.	0.	0.	0.	0.
cgs	7.6934f	20.9240f	5.7739f	20.9183f	3.8515f	20.9127f
cgd	6.7824f	6.0397f	5.0910f	6.0397f	3.3965f	6.0397f
cgb	45.2550f	111.8370f	34.1597f	111.8408f	23.0637f	111.8455f

subckt element	0:mn13	0:mp1	0:mp2	0:mp3	0:mp4	0:mp5
model	0:n7	0:p7	0:p7	0:p7	0:p7	0:p7
id	1.0643n	-1.4953u	-1.4950u	-48.1142n	-1.0703n	-1.0678n
ibs	0.	0.	0.	0.	0.	0.
ibd	-8.584e-16	10.0538f	9.9920f	6.0826f	29.0589f	28.2028f
vgs	747.6348m	-999.2002m	-999.2002m	-608.2592m	-608.2592m	-608.2592m
vds	85.8355m	-1.0054	-999.2002m	-608.2592m	-2.9059	-2.8203
vbs	0.	0.	0.	0.	0.	0.
vth	952.0203m	-770.9437m	-770.9437m	-770.9437m	-770.9437m	-770.9437m
vdsat	37.9743m	-240.4162m	-240.4162m	-44.3060m	-44.3060m	-44.3060m
beta	54.8649u	43.7416u	43.7344u	1.0357m	23.0398u	22.9845u
gam eff	605.0000m	240.0000m	240.0000m	240.0000m	240.0000m	240.0000m
gm	20.4585n	10.7400u	10.7382u	951.8178n	21.1740n	21.1231n
gds	21.3218p	39.9210n	39.9079n	1.2711n	30.1032p	29.9588p
gmb	6.7098n	1.4612u	1.4609u	125.7804n	2.7981n	2.7914n
cbd	0.	0.	0.	0.	0.	0.
cbs	0.	0.	0.	0.	0.	0.
cgs	1.9263f	52.7760f	52.7760f	215.5213f	4.5034f	4.5034f
cgd	1.6989f	3.7248f	3.7242f	86.9216f	1.8286f	1.8282f
cgb	11.9670f	1.6062f	1.6062f	244.0511f	5.9238f	5.9238f

subckt element	0:mp6	0:mp7	0:mp8	0:mp9	0:mp10	0:mn14
model	0:p7	0:p7	0:p7	0:p7	0:p7	0:n10
id	-1.0652n	-1.0627n	-1.0601n	-1.4953u	-1.4950u	14.6274u
ibs	0.	0.	0.	0.	0.	0.
ibd	27.3463f	26.4894f	25.6322f	26.4846f	9.9920f	-12.2770f
vgs	-608.2592m	-608.2592m	-608.2592m	-993.0238m	-999.2002m	1.7750
vds	-2.7346	-2.6489	-2.5632	-2.6485	-999.2002m	1.2277
vbs	0.	0.	0.	0.	0.	0.
vth	-770.9437m	-770.9437m	-770.9437m	-770.9437m	-770.9437m	952.0203m
vdsat	-44.3060m	-44.3060m	-44.3060m	-235.1686m	-240.4162m	668.1409m
beta	22.9294u	22.8745u	22.8199u	45.7484u	43.7344u	50.7411u
gam eff	240.0000m	240.0000m	240.0000m	240.0000m	240.0000m	605.0000m
gm	21.0725n	21.0220n	20.9718n	10.9826u	10.7382u	33.9022u
gds	29.8153p	29.6728p	29.5312p	41.7525n	39.9079n	178.1530n
gmb	2.7847n	2.7780n	2.7714n	1.4966u	1.4609u	10.4951u
cbd	0.	0.	0.	0.	0.	0.
cbs	0.	0.	0.	0.	0.	0.
cgs	4.5034f	4.5034f	4.5034f	52.7760f	52.7760f	1.4230p
cgd	1.8277f	1.8273f	1.8268f	3.8863f	3.7242f	7.7834f
cgb	5.9238f	5.9238f	5.9238f	1.6257f	1.6062f	20.5786f

subckt element	0:mn15	0:mn16	0:mn17	0:mn18
model	0:n10	0:n10	0:n10	0:n10
id	7.3137u	7.3137u	7.3137u	7.3137u
ibs	0.	0.	0.	0.
ibd	-14.4466f	-14.4466f	-23.2765f	-23.2765f
vgs	1.7723	1.7723	2.3276	2.3276
vds	1.4447	1.4447	2.3276	2.3276
vbs	0.	0.	0.	0.
vth	952.0203m	952.0203m	952.0203m	952.0203m
vdsat	666.0264m	666.0264m	1.1123	1.1123
beta	25.5284u	25.5284u	9.3803u	9.3803u

gam eff	605.0000m	605.0000m	605.0000m	605.0000m
gm	17.0026u	17.0026u	9.9018u	9.9018u
gds	89.3125n	89.3125n	90.2860n	90.2860n
gmb	5.2660u	5.2660u	2.7549u	2.7549u
cbd	0.	0.	0.	0.
cbs	0.	0.	0.	0.
cgs	454.0841f	454.0841f	685.8792f	685.8792f
cgd	3.0270f	3.0270f	4.4770f	4.4770f
cgb	9.8298f	9.8298f	14.9584f	14.9584f

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