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Computer aided design of a broadband microwave power divider

Jaideep Mukherjee
New Jersey Institute of Technology

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ABSTRACT

Title of Thesis: Computer Aided Design of a Broadband Microwave Power Divider

Name: Jaideep Mukherjee, Master of Science, 1991

Thesis directed by: Associate Professor, Dr. Edip Niver.

The purpose of this thesis to provide alternative design procedure for a power divider that has broadband characteristics. The Wilkinson power divider consisting of cascaded quarter wave sections is known to increase the bandwidth while maintaining high isolation and good match conditions at individual ports. Resistors placed between the quarter wave sections served to increase isolation. The values of required components were determined using odd and even mode analysis. In this work, the approximate theory developed previously is used as a preliminary design model, and it is extended further by considering optimization techniques and coupling between adjacent arms. This novel approach is implemented on the existing software package "Microwave Design System", Hewlett-Packard Company. Results for uncoupled and coupled lines were obtained and comparisons were made. The overall performance of this design resulted in higher isolation and better matching properties. Furthermore, it was observed that monotonic change in separation between coupled lines and isolation resistor values became non-monotonic. The designed hybrid power dividers are currently being fabricated to be measured experimentally to validate the design.

COMPUTER AIDED DESIGN OF A BROADBAND MICROWAVE POWER DIVIDER

by
Jaideep Mukherjee

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by

Jaideep Mukherjee

Dr. Edip Niver, Thesis Advisor

Associate Professor of Electrical Engineering, Electrical and Computer Engineering, NJIT

Dr. Gerald Whitman, Committee member

Professor of Electrical Engineering, Electrical and Computer Engineering, NJIT

Dr. Shih-Chang Wu, Committee member

Assistant Professor of Electrical Engineering, Electrical and Computer Engineering, NJIT

BIOGRAPHICAL SKETCH

Author: Jaideep Mukherjee

Degree: Master of Science in Electrical Engineering

Date: December 1991

Date of Birth:

Place of Birth:

Undergraduate and Graduate Education:

- Master of Science in Electrical Engineering, New Jersey Institute of Technology, Newark, NJ, 1991.
- Bachelor of Science in Electrical Engineering, New Jersey Institute of Technology, Newark, NJ, 1989.

Major: Electrical Engineering

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CHAPTER 1
INTRODUCTION

Power divider splits the incoming signal that enters the input port and distributes it among the remaining output ports. A variety of directional couplers also serve as power dividers, with the condition that there is in-phase power split. In a hybrid junction, output ports are isolated from the input port, and the input signal is coupled equally between the two output ports. Some applications for the power dividers are in satellite communication, splitting and combining power in mixers, and on dividing power on a number of loads [1]. Many applications especially in test instruments require wide band operation, which necessitates more stringent design specifications.

A three port hybrid with special properties is considered for power dividers. The power into port 1 is divided equally and in-phase between ports 2 and 3. All ports must be well matched and the output ports exhibit high isolation. As an example, the Wilkinson power divider satisfies such conditions. The single stage Wilkinson power divider yields a bandwidth of 1.44:1 for an input VSWR of 1.22 and isolation of 20 dB between the output ports [2]. This device can also be used as a power combiner, with two in-phase signals.

A compensated Wilkinson power divider gives slightly wider bandwidth compared to the Wilkinson power divider [1]. In the compensated case, there is a quarterwave transmission line between port 1 and the T-junction. One way, to achieve broadband response from the three port hybrid, is to cascade pairs of quarterwave transmission lines with an isolation resistor between them [1-3]. This approach leads to increase in bandwidth and isolation, and decrease in VSWR.

Due to the presence of isolation resistors, the physical separation between the transmission lines can not be large. Therefore, one can consider two different hybrid models, one without coupling and one with coupling. A method to solve the multisection power divider is based on decomposition into even and odd modes [1-4]. In the uncoupled model, the even mode network consists of cascaded quarterwave transmission lines, and the odd mode equivalent network consists of the same transmission lines with isolated conductances connected to ground.

In the coupled case, the odd mode line admittances are not equal to the even mode ones and also the related isolated conductances are unknown [1]. This leads to an increasing complexity in the design procedure.

In this thesis, initially the approximate method based on Cohn's approach [2] is followed. The computer code for general transmission line model was developed to optimize multisection power divider with the Chebyshev polynomial approximation. Numerical results were translated into a microstrip geometry and were used as initial values for further optimization within the Microwave Design System.

The equivalent model developed for a three port hybrid took into account the T-junction and step discontinuities. In the optimization process the tolerable bounds for isolation and matching at individual ports were set to desirable values. The optimized parameters such as values for characteristic impedance, and isolation resistors were determined thereafter. Further improvement was introduced by considering the presence of coupling between adjacent sections, the spacing between these lines left as a parameter to be optimized. Numerical results were generated considering various parameters suitable for fabrication.

CHAPTER 2
THEORY OF A MICROWAVE POWER DIVIDER

2.1 Wilkinson Power Divider

The general topology of the power divider can be viewed as an n-way junction, with a resistor connected between each adjacent pair of output ports [8]. The circuit splits the incoming signal (n-1)-ways equally in all (n-1) output ports and all the output signals are assumed to be in-phase. The three port hybrid, is a special case of Wilkinson power divider, where such a device operates with only two output ports.

Common specifications require a good design where VSWR at all ports is close to unity and that there is high isolation between the remaining two output ports [2]. Better isolation is achieved by placing an isolation resistor between the output ports [9]. When a signal enters port 1 and is equally split between the output ports, there is no current flow through the resistor, therefore the isolation resistor is decoupled from the input port. The power divider consists of two quarter-wave lines with the characteristic impedance of $\sqrt{2}\,Z_0$ and the output terminating resistor has a value of $2Z_0$, where Z_0 is the characteristic impedance [10]. The equivalent circuit of such a topology is given in Figure 1.

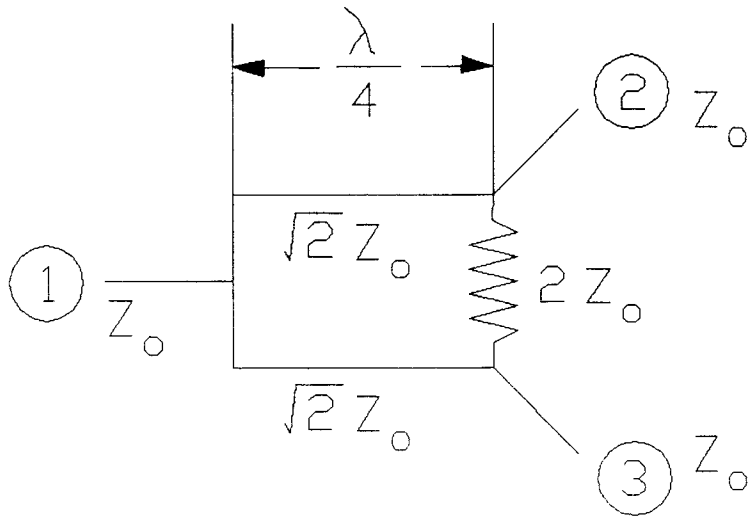


Figure 1. Wilkinson power divider.

By reciprocity a three way power divider can also be used as a power combiner of two equal in-phase input signals. If power is only fed to port 2 or 3, then only half of the power is at port 1 and the other half is dissipated in the isolation resistor. In either case the output ports are mutually isolated. Another way of looking at how the isolation resistor functions is to assume that the reflected wave has to travel π radians through the two quarter wavelength transmission lines, while a wave of equal amplitude passes through the resistor, yielding zero sum at output ports and leading to ideal isolation. In this interpretation it is assumed that the resistor has zero propagation delay.

A three-port T-junction, shown in Figure 2 cannot be matched theoretically at all three ports simultaneously. Let port 1 be matched to the input port. The phase factors ϕ_{21} and ϕ_{31} of S_{21} and S_{31} respectively, can be equalized to zero by properly selecting the reference planes [11]. The scattering matrix can then be written as [8]

$$[S] = \begin{bmatrix} 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & S_{22} & S_{23} \\ \frac{1}{\sqrt{2}} & S_{23} & S_{33} \end{bmatrix} \tag{2.1}$$

Note that $S_{23} = S_{32}$ and applying the unitary condition applicable to lossless junctions $[S][S]^* = [U]$ one obtains

$$S_{22} = -S_{23} \text{ and } |S_{22}| = |S_{33}| = |S_{23}| = \frac{1}{2} \tag{2.2}$$

Therefore ports 2 and 3 are not matched and the voltage reflection coefficient is $\frac{1}{2}$.

The isolation resistor introduced by Wilkinson into a 3-port power divider of Figure 1 results in

- perfect match at all three ports
- high isolation between ports 2 and 3

at the chosen center frequency. Figure 3 shows a possible layout of such a power divider [7]. Addition of more quarter-wave stages leads to a possibility of expanding the desired bandwidth.

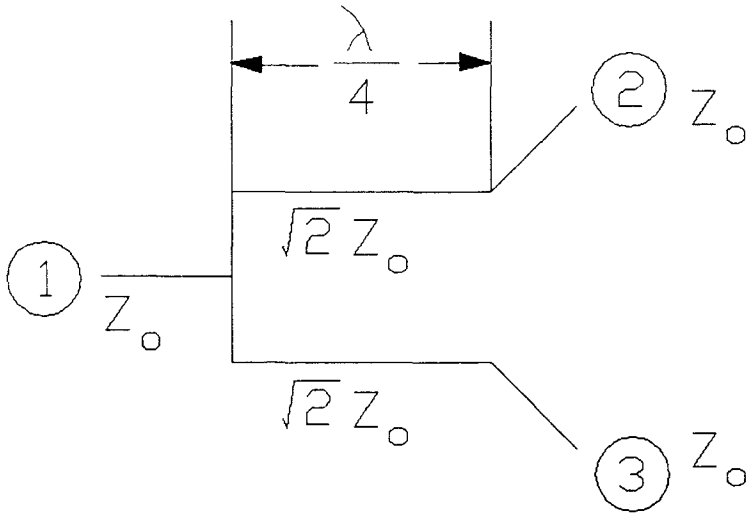


Figure 2. A 3-port T-junction with no isolation resistor.

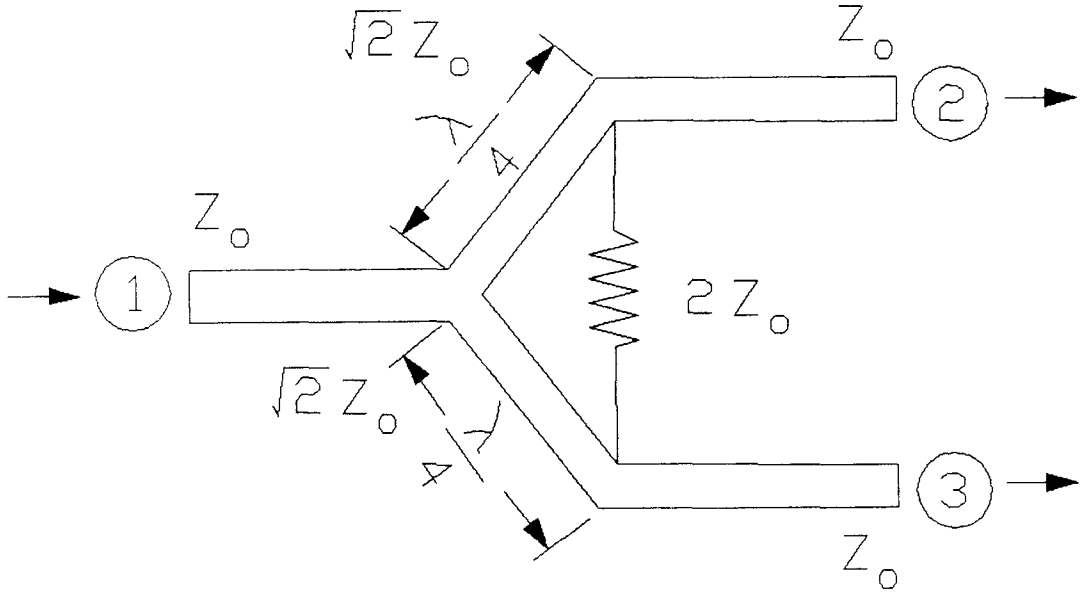


Figure 3. A possible layout for the Wilkinson power divider.

2.2 Multisection Wilkinson Power Divider

The multisection topology in a power divider yields a better bandwidth performance while giving an opportunity to match the real impedances [2]. With improved impedance matching, one obtains reduction in frequency sensitivity, maximum power transfer, and reduced insertion loss.

The multisection hybrid has N cascaded sections along the output arms. In this case, $N > 1$ and a section is defined as a pair of quarter-wave transmission lines followed by an isolation resistor between them. The resistor does not effect the input port, but it is vital for isolation of the output ports. It should be noted that the complexity in analysis and synthesis of the hybrid increases as N increases. It has already been shown by Cohn [2,12] that more cascaded sections results in the increased bandwidth of the power divider.

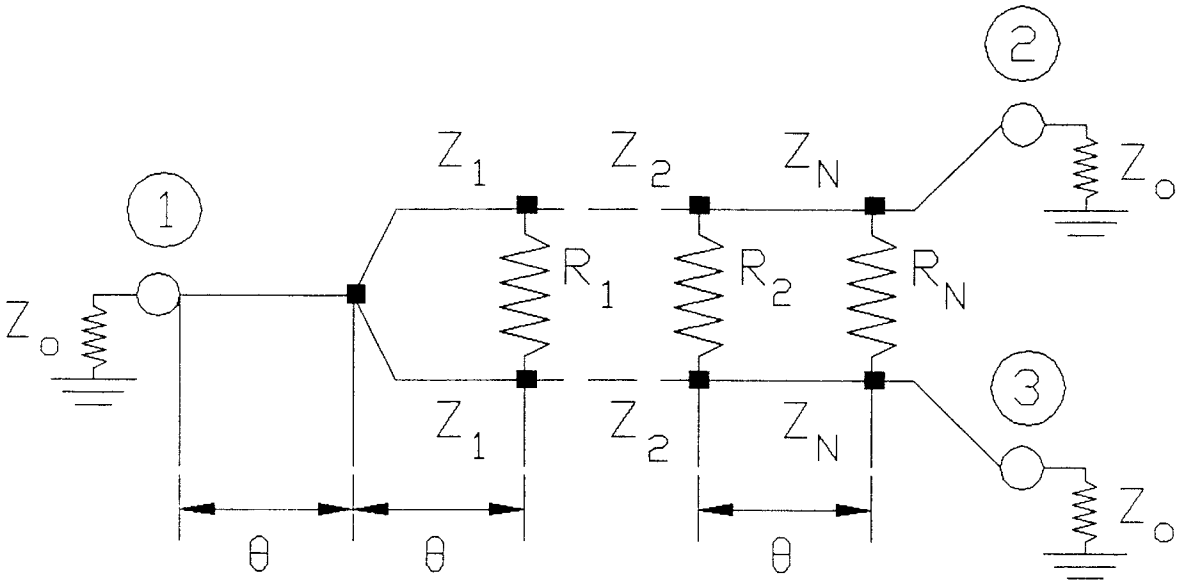
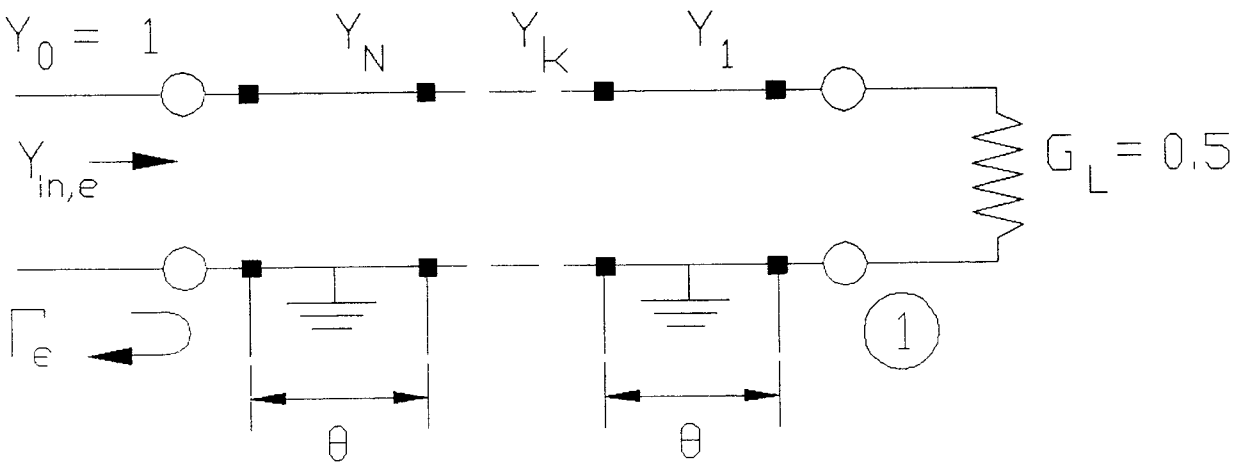
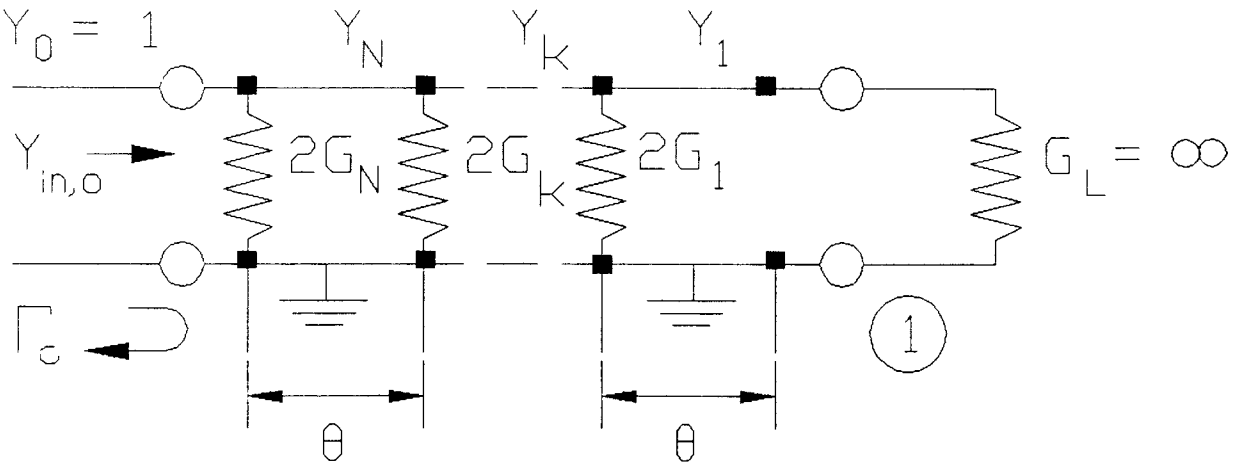


Figure 4. A multisection three port hybrid.



a) Bisection for even mode case, admittance circuit.



b) Bisection for odd mode case, admittance circuit.

Figure 5. Decomposition of a power divider into odd and even modes.

Required specifications such as low VSWR at all ports and high isolation between the two output ports is applicable to multisections at a broader bandwidth. Analysis of a three port hybrid with N sections is based on using odd and even mode decomposition. Figure 4 shows a symmetrical multisection power divider, followed by Figure 5 where the equivalent circuits for even and odd modes are depicted.

For the odd mode case, the line of symmetry is the virtual ground, as shown in Figure 5(b). Here, the voltages at ports 2 and 3 have the same amplitude but are out of phase [8]. Also, the values of the resistors are $\frac{R_n}{2} = 2G_n$ because at ports 2 and 3 are matched and the output ports are isolated at the centre frequency.

While in the even mode, the incident voltages are equal in magnitude and phase at ports 2 and 3. Therefore, there is no amplitude difference between all other junctions in each section and there is no current flow through the isolation resistors. We can bisect along the line of symmetry with a magnetic wall (no transverse current flow). Note that the matched input impedance doubles to $2Z_0$ as a result of such a bisection, as shown in the equivalent circuit of Figure 5(a).

One way to calculate the characteristic impedance of each quarter-wave section is to use the impedance transformer approach, which is based on the theory of small reflections [12-13]. In general, the odd and even analysis is carried out separately, then the equations can be combined to obtain a superimposed result for the power divider.

The following assumptions are made, to simplify the equations: the coupling between the adjacent lines are negligible, or else Z_k (odd) < Z_k (even) which increases the design difficulty and degrades the performance. The other assumption that simplifies the analysis is the length of each section is assumed to be the same and there should be a small difference between each section. Since each section handles a small range of frequencies, addition of all these cascaded sections leads to the final desired bandwidth.

2.3 Power Divider Analysis

Due to the cascaded structure of the multisection power divider it is easier to handle the equivalent admittance circuits rather than impedance equivalent for both even and odd modes. The values obtained by this approach will have normalized values ($Z_0 = 1$).

$$Y_1 = \frac{1}{Z_1}, \qquad Y_2 = \frac{1}{Z_2}, \ \ldots \qquad Y_N = \frac{1}{Z_N}$$

$$G_1 = \frac{1}{R_1}, \qquad G_2 = \frac{1}{R_2}, \ \ldots \qquad G_N = \frac{1}{R_N} \tag{2.3}$$

$$Y_0 = \frac{1}{Z_0} = 1, \qquad G_L = \frac{1}{2Z_0} = 0.5$$

Let the reflection coefficients Γ_e and Γ_o be for even and odd modes, respectively. The combined reflection coefficients for ports 1, 2 and 3 of the complete power divider be Γ_1, Γ_2 and Γ_3. The transmission coefficients for the respective ports are T_{12}, T_{13} and T_{23}, and are shown in Figure 6. Figure 6 also shows a simple way to depict the odd and even modes. Then the ABCD parameters of the even and odd mode circuits are defined. In the even mode circuit, the network consists of cascaded quarter-wave sections. In the odd mode circuit, it consists of quarter-wave sections terminated by shunt admittances. From Reed and Wheeler [14] the input reflection coefficient, output reflection coefficient and transmission coefficient are expressed as

$$\Gamma_{in} = \frac{\overline{A} + \overline{B} - \overline{C} - \overline{D}}{\overline{A} + \overline{B} + \overline{C} + \overline{D}} \qquad \Gamma_{out} = \frac{\overline{B} + \overline{D} - \overline{A} - \overline{C}}{\overline{A} + \overline{B} + \overline{C} + \overline{D}} \tag{2.4}$$

$$T = \frac{2}{\overline{A} + \overline{B} + \overline{C} + \overline{D}} \tag{2.5}$$

in terms of ABCD parameters.

Due to presence of symmetry in the equivalent circuits, A=D. Since the isolation resistors do not effect the input port,

$$|\Gamma_1| = |\Gamma_e| \tag{2.6}$$

The power is divided equally between ports 2 and 3 (symmetrical).

$$T_{12} = T_{13} \tag{2.7}$$

Using the energy conservation, and assuming lossless conditions, one can obtain the following equation

$$|T_{12}| = |T_{13}| = \sqrt{\frac{1}{2}\left[1 - \Gamma_e^2\right]} \qquad (2.8)$$

Due to the symmetry, the reflection coefficients at ports 2 and 3 are equal. The total reflection and transmission can be calculated from superposition of the even and odd modes as well as the incident and reflected signals. Hence, the reflection and transmission coefficients for a general three port symmetrical circuit become

$$\Gamma_2 = \Gamma_3 = \frac{1}{2}\left[\Gamma_e + \Gamma_o\right] \qquad T_{23} = \frac{1}{2}\left[\Gamma_e - \Gamma_o\right] \qquad (2.9)$$

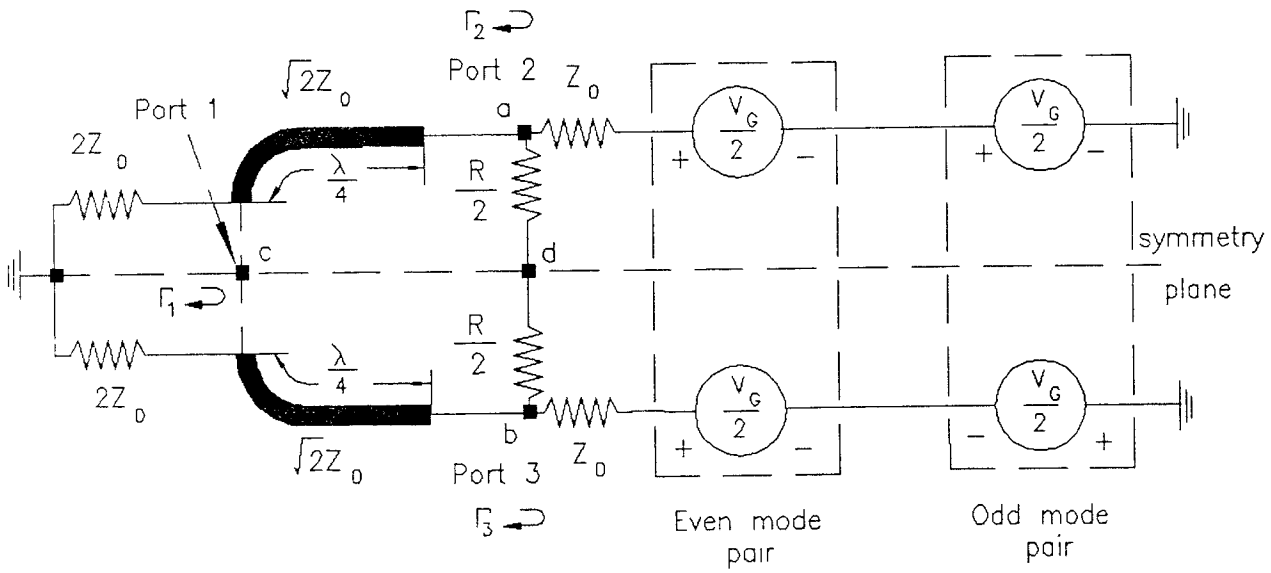


Figure 6. Wilkinson power divider for even and odd mode analysis.

In general the reflection coefficient at the input of the matching network is given by a sum of the series of multiple partial reflections arising at each of the impedance discontinuity. For $|\Gamma^k|$ small the equation is [4], where Γ^k is the reflection coefficient between stages k and k-1,

$$\Gamma = |\Gamma^1| + |\Gamma^2|e^{-j2\theta} + |\Gamma^3|e^{-j4\theta} + \ldots + |\Gamma^{N+1}|e^{-j2N\theta} \qquad (2.10)$$

A Chebyshev polynomial of order N is used to approximate equation (2.10), such that the each term in the Chebyshev polynomial corresponds

to a term in equation (2.10). Results for the case N=2 of a Chebyshev polynomial approximation are given in Figure 7.

Until now coupling between various transmission lines was omitted. The properties of coupled lines can be analyzed by suitable linear combination of odd and even modes. In general the phase velocity of the odd and even modes is different.

$$V_{pe} \neq V_{po} \qquad \theta_e \neq \theta_o \tag{2.11}$$

In case of weak coupling the phase velocity can by assumed to be equal. For tight coupling, the condition for input matching becomes [7]

$$Z_0 = \left[\frac{Z_{0e} \sin \theta_e + Z_{0o} \sin \theta_o}{Z_{0o} \sin \theta_o + Z_{0o} \sin \theta_e} \right]^{1/2} \sqrt{Z_{0o} Z_{0e}} \tag{2.12}$$

where the electrical length at the center frequency is

$$\theta = \frac{1}{2} \left[\theta_e + \theta_o \right] = \frac{2\pi}{\lambda_o} \frac{\sqrt{\varepsilon_{ee}} + \sqrt{\varepsilon_{eo}}}{2} \ell = 90^\circ \tag{2.13}$$

and ℓ is the physical length of the each section. To accommodate for coupling at the band edges properly, one can introduce the over coupling at the center frequency. In general, maximum coupling occurs at the center frequency. The coupling factor is given as

$$C' = 20 \log \left| \frac{Z_{0e} - Z_{0o}}{Z_{0e} - Z_{0o}} \right| \text{ dB} \qquad Z_0^2 = Z_{0e} Z_{0o} \tag{2.14}$$

Note that for uncoupled and coupled lines, the even mode analysis remains the same. It differs only in the case of an odd mode. There are tabulated results in [15], but only modified design which contains only one resistor just after the first stage was treated.

The general procedure as outlined by Cohn [2] to determine characteristic impedance and isolation resistor for each individual stage followed in this thesis. The computer code developed to determine these values is given in Appendix A.

2.4 Power Divider Synthesis

There are different methods to solve the multisection quarterwave stepped transformer. Hansen had proposed a binomial-coefficient method to solve the stepped transformer. Cohn used the Chebyshev polynomial approach to optimize the transformer [2]. Results showed that the Chebyshev transformer had an improved response, for equal number of sections. Butterworth polynomials have the advantage of a maximally flat response, but in general such approach yields the bandwidth smaller compared to the one obtained by the Chebyshev polynomials.

The Chebyshev polynomial optimization method provides maximum bandwidth for a given VSWR, or minimum VSWR for a given bandwidth. This method treats the terms in such a manner that the resulted VSWR has the characteristics equal to a rippled response of a Chebyshev approximation. It is simple to implement such an algorithm on a stepped transformer with N sections. Given two of the following maximum VSWR, and bandwidth or number of sections; one can determine the characteristic impedance of each section.

There are finite number of elements in a multisection power divider. Since in the equivalent circuit for an odd mode, the termination is an short circuit, therefore the impedances in reflection and transmission coefficients can be expressed in terms of s, where [2]

$$s = - j \cot \phi \tag{2.15}$$

where ϕ is the equivalent electrical length of the individual section.

Hence, the problem can be reduced to an algebraic equation, with real positive input impedance functions, of the complex variable s. The even mode circuit is a quarter-wave stepped transformer, with conductance values varying from 1 to 0.5. There are already tables and formulas available to obtain the optimum values for Y_1 to Y_N [5,13]. The isolation resistors G_1 to G_N, need to be calculated with Γ_2, Γ_3 and T_{23} at optimum. It is, however, easier to determine G_1 to G_N such that Γ_o is optimized. The higher order reflections coefficients are complicated and difficult to evaluate, but are necessary to be included

to yield Chebyshev response. An approximate modified method is chosen to simplify the calculations [2]. In this method, when Γ_e and Γ_o were at optimum, Γ_2, Γ_3 and T_{23} were determined close to optimum.

The synthesis gets more difficult for $N \geq 3$. The $|\Gamma_o|$ vs ϕ is symmetrical about $\phi = 90^\circ$ and it also has a maximum ripple at $\phi = 90^\circ$ for N even. From equation (2.15), note that the even powers of s are real and odd powers of s are imaginary. Figure 7 shows a general equal ripple response for N=2. The band edges are at ϕ_1 and ϕ_2, and because of symmetry $\phi_2 = 180 - \phi_1$. The zero points are ϕ_3 and ϕ_4, defining that the port is perfectly matched.

One can equate for $\Gamma_o = 0$, and obtain two equations, one real and the other imaginary. Setting each equation to zero one can attempt to solve for the isolation resistors. If $N \geq 3$, the calculations tend to become very tedious. The formula relating ϕ_1 to ϕ_3 is obtained form the relation $T_N(x) \alpha |\Gamma_o|$. Cohn gives two possible values for x [2]

$$x = \frac{(90^\circ - \phi)}{(90 - \phi_1)} \quad \text{or} \quad x = \frac{\cos \phi}{\cos \phi_1} \tag{2.16}$$

stating that the first equation gives better results. The above procedure was followed in the code in Appendix A. The bandwidth is determined from f_1 to f_2, and the bandwidth ratio is defined as f_2/f_1 and the fractional bandwidth W

$$W = \frac{2\left[\frac{f_2}{f_1} - 1\right]}{\left[\frac{f_2}{f} + 1\right]} \tag{2.17}$$

The number of zeros ($\Gamma = 0$) shows the number of sections present in the multisection power divider. This is shown in Figure 7.

There are discontinuities between the quarter-wave transformer sections. These produce reactive effects, usually can be taken into account by an equivalent shunt capacitance. By reducing the length of the quarter-wave transformer a few percent also helps to compensate for such reactive effects. Practically, a lot depends on the fabrication process and on the resistors tolerances.

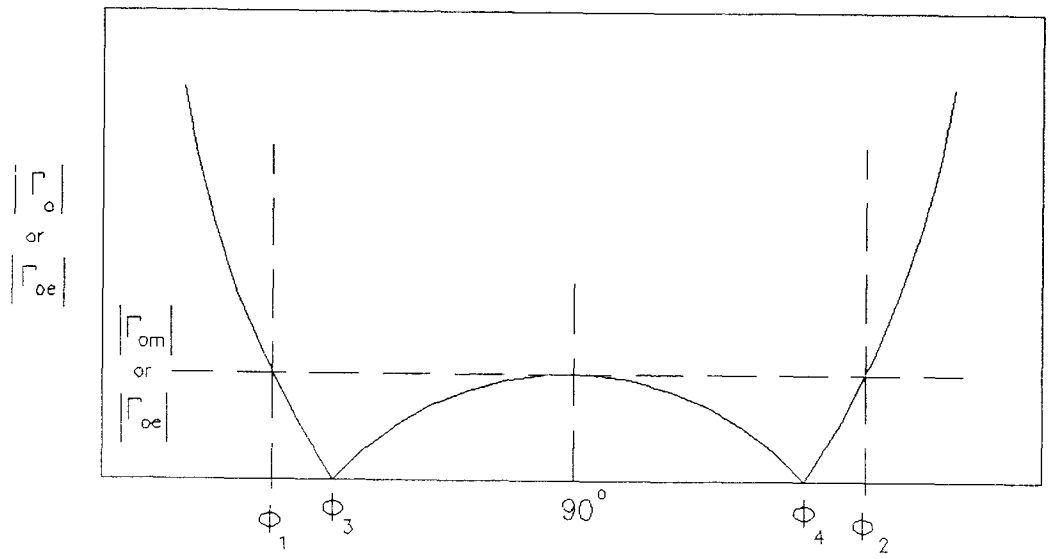


Figure 7. General equal-ripple behavior of $|\Gamma_o|$ and $|\Gamma_e|$ functions vs ϕ for N = 2.

2.5 Microstrip Transmission line

The power divider design described in previous sections is implemented on the microstrip medium. The lowest order mode propagation along the microstrip line has quasi-TEM character. The range of realizable impedances in a microstrip structure extend from 20Ω to 125Ω. The relative permittivity varies as

$$\frac{1}{2}\left(\varepsilon_r + 1 \right) \leq \varepsilon_{eff} \leq \varepsilon_r \qquad (2.18)$$

where $\varepsilon_{eff} = \varepsilon_r$ when the strip width is very wide, therefore all the field is confined within the substrate [6]. When the strip width is very narrow, the field is shared between the substrate and the air.

There are two basic methods to solve this structure, quasi-static approach and full wave approach [7]. In the quasi-static approach, the equations are simple but they have limited range of validity. It is suitable if the strip width and substrate are much smaller than λ in the dielectric material [16]. The full wave approach yields the

results which are exact, but require very rigorous procedure. Using numerical methods, the characterization of microstrip lines require extensive computation, but in practice closed form expression are necessary for Z_0 and ε_r, which is difficult to obtain from rigorous procedures.

The microstrip geometry involves the following parameters [17] (all appropriate units are in mils) -

ε_r - dielectric constant
H - height of substrate
h - height of cover from substrate
W - width of a conducting strip
w - width of substrate
T - conductor thickness

The characteristic impedance of the microstrip

$$Z_0 = f\left(\frac{W}{H}, \text{substrate material}\right) \qquad (2.19)$$

The Figure 8 below illustrates the cross section of the microstrip line.

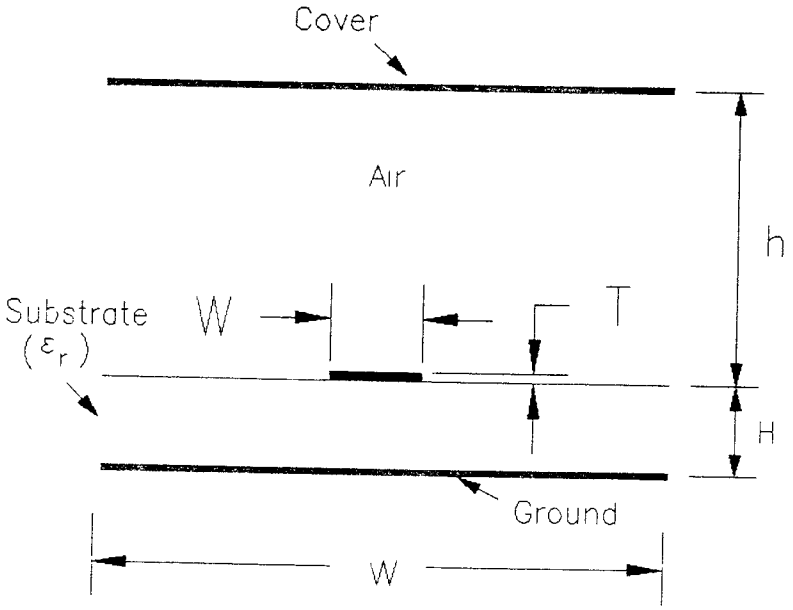


Figure 8 Cross sectional view of microstrip structure.

Advantages of a microstrip geometry over a classical waveguide or a coaxial line is that it has a wider bandwidth, good miniaturization, weight reduction, satisfactory thermal characteristics, reasonable RF power handling capacity and ease of component integration, as well as

lower cost.

The following recommendations are followed in practice to achieve better performance. Let the value h, between the substrate and the metallic cover has to be chosen at least 10 times the substrate thickness, to avoid higher order propagating modes ($h \geq 10H$). The physical width of the housing has to be less than half of the free space wavelength at operating frequency ($w \leq 0.5\lambda_0$) [16].

2.6 Microstrip Analysis and Synthesis Equations

Analysis expressions based on quasi-TEM mode were reported by Wheeler and Schneider [7,16]. These formulae are for analysis, and there is another set for synthesis. For analysis the W/H and ε_r are given, in case of synthesis Z_0 and ε_r are given. The formulae relevant to the design of power divider are only outlined below and full version is presented elsewhere [16-17].

For $\frac{W}{H} < 1$

$$Z_0 = \frac{\eta_0}{2\pi \sqrt{\varepsilon_{eff}}} \ln \left[\frac{8H}{W_e} + \frac{W_e}{4H} \right] \tag{2.20}$$

where $\eta_0 = 120\pi\Omega$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \left[\left[1 + \frac{12H}{W_e} \right]^{-0.5} + 0.04 \left[1 - \frac{W_e}{H} \right]^2 \right] \tag{2.21}$$

where the effective strip width is

$$W_e = W + \frac{T}{\pi} \left[\ln \frac{2H_e}{T} + 1 \right] \tag{2.22}$$

and the effective thickness of substrate is

$$H_e = H - (2T) \tag{2.23}$$

Similarly, the synthesis formulae are,

$$\frac{W}{H} = \frac{8}{P}\left[\frac{(7 + 4/\varepsilon_r)P}{11.0} + \frac{1 + 1/\varepsilon_r}{0.81}\right]^{1/2} \quad (2.24)$$

$$P = \exp\left[\frac{Z_0}{84.8}(\varepsilon_r + 1)^{1/2}\right] - 1 \quad (2.25)$$

The wavelength for the microstrip line is [6,17]

$$\lambda_g = \frac{V_p}{f} = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}} = \frac{C}{f\sqrt{\varepsilon_{eff}}} = \frac{2\pi\ell}{\theta} \quad (2.26)$$

where
λ_g = wavelength in the microstrip
λ_0 = electrical wavelength in the free space
$C = 3 \times 10^8$ m/s
ℓ = physical length
θ = electrical length

2.7 Coupled Microstrips Line

The strips can either be edge coupled or broadside coupled. The implementation in the power divider application requires them to be edge coupled. Figure 9 shows such edge coupled lines on a microstrip structure.

The sample design expressions [1] are outlined below but the versions built in Microwave Design System were utilized in final results.

$$\left[\frac{W}{H}\right]_{odd} = \frac{2}{\pi}\cosh^{-1}\left[\frac{(G + 1)F - 2}{(G - 1)}\right] \quad (2.27)$$

$$+ r\cosh^{-1}\left[\frac{\cosh^{-1}\frac{1}{2}\left[(G + 1)F + (G - 1)\right]}{\cosh^{-1} G}\right] \quad (2.28)$$

where $$F = \cosh \tfrac{1}{2} \pi \left[\frac{W}{H} \right]_{even} \tag{2.29}$$

$$r = \frac{1}{\pi} \qquad \varepsilon_r \geq 6 \tag{2.30}$$

$$r = \frac{8}{\pi(\varepsilon_r + 1)} \tag{2.31}$$

where the value of G that satisfies equation (2.27) is obtained numerically.

The width and separation of the coupled strip lines are

$$\frac{W}{H} = \frac{1}{\pi} \left[\cosh^{-1} H - \cosh^{-1} G \right] \tag{2.32}$$

$$\frac{S}{H} = \frac{2}{\pi} \left[\cosh^{-1} G \right] \tag{2.33}$$

where $$H = \tfrac{1}{2}\left(G + 1 \right)F + \tfrac{1}{2}\left(G - 1 \right)F \tag{2.34}$$

The above equations are not the most accurate ones, since they are based on quasi-TEM equations.

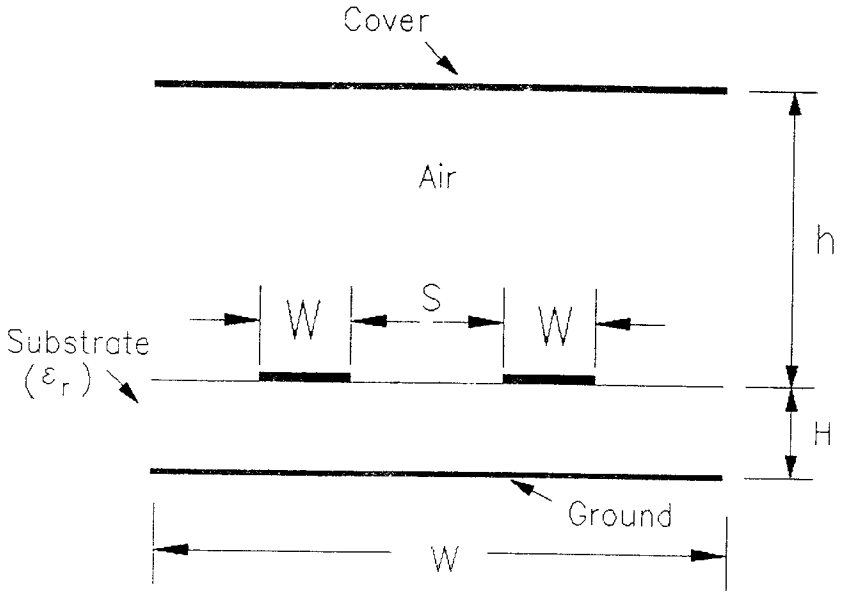


Figure 9 Cross sectional view of edge coupled microstrip lines.

2.8 Microstrip Discontinuity

The maximum frequency in microstrip applications is limited by discontinuity effects, fabrication tolerances, higher order mode losses, and low Q due to radiation of discontinuities. At higher frequencies losses are due to radiation of higher order modes and also fabrication gets exceedingly difficult [6]. All microstrip configurations are dispersive and the lower limit of the effective permittivity is $\varepsilon_{eff}(0)$, and the permittivity changes continuously in a nonlinear way to ε_r as frequency increases, as shown in equation (2.35). The maximum thickness is limited by coupling losses (open ends, gaps, step in width, bends) incurred in the microstrip. In coupled lines there can be two different modes of propagation. Since the structure is non-homogeneous and the field can be different, ε_{eff} and V_p are not equal for such two modes.

The microstrip is dispersive above f_t , where f_t is the critical frequency as another mode starts to contribute significantly.

$$f_t = 2.413 \left[\frac{Z_o}{H \sqrt{\varepsilon_r - 1}} \right]^{1/2} \text{ in GHz} \qquad (2.35)$$

and the effective permittivity can be approximated as

$$\varepsilon_{eff}(f) = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{eff}(0)}{1 + (f/f_T)^2} \qquad (2.36)$$

with

$$f_T = \left[\frac{\varepsilon_r}{\varepsilon_{eff}(0)} \right]^{1/2} \frac{Z_0 \, 10^5}{5.08 \, \mu_0 \, H} \qquad (2.37)$$

where the above equation is valid for (fH) < 39 GHz.mm. This expression for effective permittivity gives more accurate results at higher frequencies.

The effect of the discontinuities on circuit performance are a

frequency shift in narrow band circuits, a degradation in the VSWR at the relative ports, and higher ripple in gain flatness of broadband IC's. Note also that as frequency increases the effect of discontinuity increases. Most of the microstrip discontinuities are modeled by excessive capacitances. There are few compensation techniques to reduce such discontinuity effects. For the step in width the discontinuity can be compensated by gradual decrease of the wider strip. For a tee junction, this can be realized by cutting an isosceles triangle with $\theta = 30^{\circ}$ from the flat side of the tee [7]. At corners, this compensation is done by cutting the 90° angle to create a miter-bend of two $\pm 45^{\circ}$ angles with a small distance between them [6].

The effect of the metallic enclosure provides, mechanical strength, electromagnetic shielding, connector mounting and ease of handling. The presence of walls lowers the characteristic impedance and the effective permittivity of the microstrip [17].

$$Z_0(\text{shielded} = Z_0(\text{unshielded}) - 270 \left\{ 1 - \tanh\left[0.28 + 1.2 \sqrt{\frac{h}{H}} \right] \right\} \tag{2.38}$$

In the industry the trend is to use uncoupled lines since the design process gets a lot complicated if coupling is taken into account. Also to make sure that there is no coupling and to make the device shorter. The strips are curved in a wiggly shape so that the strips are only close together to connect the resistor across them. Figure 10 below illustrates such a design.

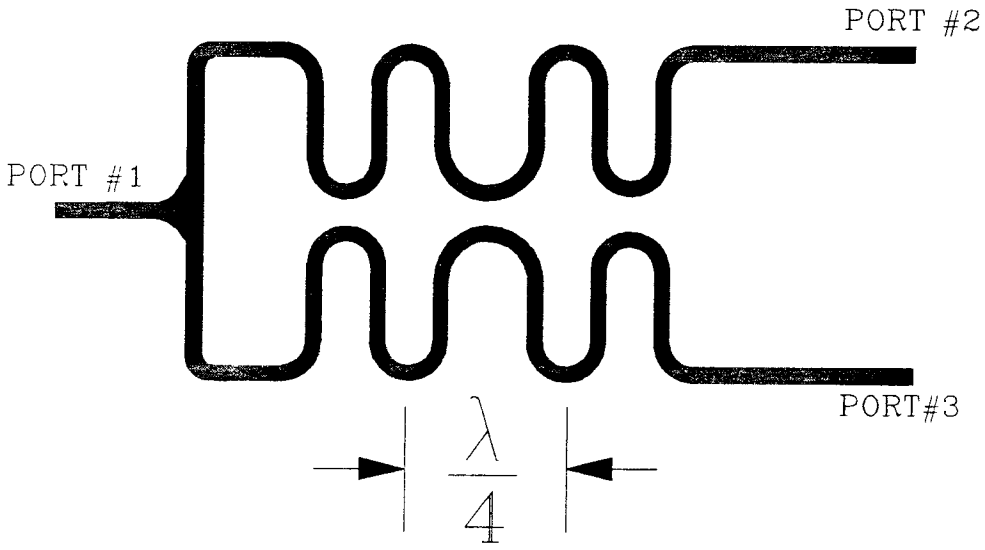


Figure 10 Layout of a practical power divider.

CHAPTER 3
NUMERICAL SIMULATORS

The wide band power divider including coupling addressed in this thesis requires extensive formulation and numerical evaluations, Though the available CAD packages for microwave applications are limited in there performance, it is still practical to utilize them if they yield valid results.

3.1 Background

CAD packages in microwave engineering evolved from simple algorithms to more complex ones. There are different levels of computations, where higher levels address problems of more complicated nature. The simplest level treats Smith chart and related equations. The next higher level uses matrices, especially ABCD matrix representation to combine various circuit elements. Then S parameters are used to determine attenuation, phase shift and reflection coefficients. Usually matrix operations are suitable for evaluations using computers. The higher level algorithms are further used to combine S parameter matrices directly and address much more complex problems.This is the level to which current microwave simulators have reached. These simulators allow engineers to design systems in more efficient way in both time and money. They also give the engineer precisely characterized and performance based models on such simulations and optimizations. This is desired, since in microwave integrated circuits, the engineer does not have an option to tune the circuit after fabrication. Usage of CAD tools helps to reduce the time interval from the first design to the final production because, the engineer does not have to built and test the circuit at every stage. It should be noted however that computers cannot replace engineers, good knowledge and solid principles of microwave design are still an absolute necessity.

3.2 CAD in Microwave Engineering

As a first step, the engineer has to define the required circuit specifications. Then a preliminary block diagram and an equivalent circuit have to be developed. The circuit is then modeled on a CAD program with the aid of the extensive library of devices. These libraries in a package include S parameters of active devices, passive devices and also user defined models. The CAD program converts the components described by the user into numerical models and evaluates based on predetermined specifications. For optimization, the results of the analysis are compared to given specifications. If the results are not satisfactory, then certain parameters specified by the user can be changed in a systematic manner within the given range. After achieved satisfactory simulations, the circuit fabrication and experimental measurements will follow.

3.2.1 Optimization Methods used by CAD

In a general optimization problem, an error function is defined as the difference between the designed circuit performance and given specifications. Then the error function is minimized using approaches such as gradient method or random method. The gradient method uses information about the derivatives of the performance functions to arrive at the modified set of parameters. Random optimization, as the name suggests is based on a random number which is selected within a specified range and then seeks for a global minimum.

3.2.2 Errors within CAD

The CAD approach can only produce accurate results for the system in consideration based on the validity and accuracy involved in each individual element. The user should exercise caution that such limits are not exceeded within specified range of values and frequencies. The numerical results should not be taken for granted but only have to be accepted after all possible validations.

3.3 Microwave Design Systems (MDS)

The CAD simulator used in this thesis is the Microwave Design System from Hewlett-Packard Company. The HP 9000 series platforms using Microwave Design Systems, has the most features compared to other platforms. One can do circuit simulation, run on X11 windows, run on diskless clusters, test instrument I/O, Microwave Linear Simulator (MLS) icon and Microwave Nonlinear Simulator (MNS). The most significant difference between MLS and MNS is that in MNS the analysis and optimization is controlled entirely by the circuit page where the other does not. The user has access to a mouse and menus, which makes MDS a user friendly system. Also it has on-line help on a wide group of functions.

3.3.1 Circuit Analysis and Optimization on MDS

First open a file and insert the following icons, design, presentation, dataset, MLS, and layout into the file. Enter the schematic of the circuit design into the circuit page of the design icon. Setup the MLS icon to analyze the circuit, with parameters such as frequency range, dataset name and circuit name. Setup involves the kind of results one would want to see, such as Smith chart, rectangular, log, polar, or tables. When the performance of the circuit has been analyzed, the layout can be obtained in the layout icon.

The components are obtained from the microwave library or from user-defined, user-configured libraries when the circuit is built. They could also be circuits already designed using components from the microwave library. Data for a component can also be obtained from a network analyzer. MDS can check the circuit schematic for open wire ends and unconnected pins. With each component, there is an attribute with all the parameters that define the element. Like for a microstrip transmission line the parameters are width and length. Parameters can also expressed as equations of other variables. A circuit can be made up of subcircuits. MLS simulates the electrical performance of the

circuit. Optimization can also be done. The MLS icon is made up of different pages, frequency, optimization variable, optimization goals, analysis and optimization. In the frequency page, the user can enter a list of frequencies, linear by number of points, linear by step size, exponential by number of points, and exponential by step size. Different bands of frequencies are allowed. In the analysis page the following information is needed, name of design icon, name of frequencies page, name of dataset where results would be stored. In the nature of analysis to be done, the choices are S-parameters, voltage and currents at points indicated by probes on the schematic, noise analysis, and group delay.

For optimization of the variable parameters, using the goals, the user enters into the optimization goal page in the MLS icon. The outcome of the optimization depends on the optimization method, number of frequencies chosen, the separation of good and bad values, the termination criteria and the circuit parameters that are varied. The goals that are set can be very complex, as long as, they are defined using MDS mathematical functions and circuit parameters. The three different methods that are used in MDS optimization are the, gradient method, the random method and the hybrid method. In the hybrid method, many gradient methods are repeated to find the local minimum. Then a new set of initial conditions is chosen randomly and the gradient process begins again. This methods takes a very long time and the error function is not necessary decreasing, but the best values are those with the lowest error function during the whole optimization. In practice few guidelines are to be followed to obtain effective results. The minimum value for number of iterations per update should be set to five times the number of optimization variables. The other factor, total number of iterations should be set to ten times the number of optimization variables squared.

3.3.2 Layout and printing on MDS

The layout of the circuit can be obtained at any time after the circuit schematic has been entered, if necessary even before the analysis . The layout can be edited and also the user can enter the

box and the drill holes for the screws as well as the connectors that can be inserted. Since there is a lot of information, it is all stored in layers. So the user should only show the layers that are currently being used, to keep the efficiency high. Using layers, keeps the layout easy to edit. One layer can be used only for the metalization, another for the substrate, another for lumped circuit elements, another for connectors, another for drilling targets and alignments.

Before plotting or printing, the item that would be plotted can be inserted into a view and then re-inserted into the document icon. A form can be generated in the form icon and inserted into the document icon so that the plots look standardized, there could be a box with the company logo and also the device number and so on. The user can then customize the page and print it out. The graphs, the circuit schematic and the layout can be plotted. The information is updated automatically. For instance if the marker in a graph is moved it is also moved in the document. For the MDS to perform efficiently, the user should have only necessary icons open, avoid overlapping windows, close unused icons and windows, run memory management occasionally. Also to shorten the process of going through the menus there are user defined keys, so keyboard can be used. Other features are eight different choices of fonts, menus wrap and scroll at the window borders, in the circuit page the unused pins, connectors and wire ends can be highlighted. Data can be read or written to an instrument from the dataset. Also the data can be read or written in a Touchtone format.

CHAPTER 4
NUMERICAL RESULTS AND CONSIDERATIONS

4.1 Design

The broadband power divider was designed on the microstrip media. The initial design procedure is based on earlier work [2] which was based for any transmission line media.

The microstrip substrate is chosen according to commercially available samples having the following parameters:

ε_r = 9.6 (or 10.8)	relative dielectric constant
H = 10 (or 50) mils	height of substrate
T = 0.001	dielectric loss tangent

and the chosen metalization is copper.

The design procedure [2] required finite number of quarter-wave steps, increasing in number depending on the chosen bandwidth. The computer program in C++ language is written to obtain the characteristic impedance and terminating isolation resistor at each stage for any number N upto N_{max} = 7. In the following sections results for N = 3, 5 and 7 will be presented for different parameters.

There are limitations in approximating microstrip within this program since not all conditions were taken into account. The program uses equations from Wheeler and Schneider [17] for the condition W/H < 1. These results are not valid for higher frequencies. The main purpose of this program is to obtain preliminary results that could be further optimized on a microwave simulator. The program is included in Appendix A and requests the user to enter design specifications: the dielectric constant of the substrate material, substrate height, conductor thickness, number of stages, input impedance, output impedance (the two impedances that you want to match), the bandwidth ratio, and the low end frequency. The output of this program consists of repetition of the input specifications for verification and furthermore yields the maximum VSWR and minimum isolation. The remaining output parameters are characteristic impedance (actual and normalized) of each stage, width of the strip, the terminating

isolation resistors that follow each stage. The numerical results obtained from this program were validated with the published data [2]. The preliminary results form this code in Appendix A were fed into the Microwave Design System and was subjected to optimization for various parameters such as insertion loss, isolation and low VSWR at all ports. Hence, the optimized parameters were characteristic impedance and isolation resistor for each individual stage. Other conditions that were kept variable in the complete design were, the number of quarterwave sections and the substrate material. Additional cases were based on the presence or absence of coupling between the two arms of output ports. If coupling was considered then, the distance between two arms became an optimized parameter.

4.2 Numerical Data

The designed microwave broadband power divider was realized on a substrate with $\varepsilon_r = 9.6$ and the height of $H = 10$ mils. The output of the program in Appendix A for 3-quarterwave sections and load impedance of 100Ω for bandwidth ratio of 3 is presented in Table 1(a). The other alternative substrate parameters are $\varepsilon_r = 10.8$ and $H = 50$ mils. For the chosen bandwidth ratio of 2, preliminary numerical results are given in Table 1(b). Similarly numerical results for the 5 and 7 stage models are attached in Tables 1(c) and 1(d). One obvious observation from the above tables is that the bandwidth ratio is proportional to the number of quarterwave sections, it increases with higher number of such stages. The matching conditions and maximum isolation is achieved if narrow bandwidth is tolerated.

It is observed that the characteristic impedance values increased monotonically from the output ports towards the junction. However, monotonic change in values of terminating isolation resistors remained until $N = 4$ and beyond that monotonic behavior disappeared.

For Substrate parameters are -
er = 9.6, H = 10, T =0.001

Other parameters of the design -

Number of stages	N =	3
Input impedance	z0 =	50
Load impedance	zl =	100
Bandwidth ratio	bw =	3.00
Low end frequency	f1 =	0.50
high end frequency	f2 =	1.50
center frequency	f0 =	1.00
fractional bandwidth	fbw =	1.00
low end phase	p1 =	45.00
high end phase	p2 =	135.00
width of microstrip	W =	9.96
quarter wave length	L =	1159.02
VSWR max. port 1	S1 =	1.098
VSWR max. port 2 &3	S23 =	1.020
Isolation max.	I23 =	27.59 dB

impedance [0]	= 50.00	normalized	= 1.0000	width	= 9.956
impedance [1]	= 57.43	normalized	= 1.1487	width	= 7.387
impedance [2]	= 70.71	normalized	= 1.4142	width	= 4.389
impedance [3]	= 87.06	normalized	= 1.7411	width	= 2.333
impedance [4]	= 100.00	normalized	= 2.0000	width	= 1.418

Resistor [1]	= 386.25	normalized	= 7.7250
Resistor [2]	= 204.51	normalized	= 4.0902
Resistor [3]	= 97.79	normalized	= 1.9559

Table 1(a) Preliminary data for a 3-stage power divider model obtained form a code in Appendix A.

For Substrate parameters are -
er = 10.8, H = 50, T =0.001

Other parameters of the design -

Number of stages	N =	3
Input impedance	z0 =	50
Load impedance	zl =	100
Bandwidth ratio	bw =	2.00
Low end frequency	f1 =	2.00
high end frequency	f2 =	4.00
center frequency	f0 =	3.00
fractional bandwidth	fbw =	0.67
low end phase	p1 =	60.00
high end phase	p2 =	120.00
width of microstrip	W =	44.37
quarter wave length	L =	367.11
VSWR max. port 1	S1 =	1.027
VSWR max. port 2 &3	S23 =	1.005
Isolation max.	I23 =	38.90 dB

impedance [0]	=	50.00	normalized =	1.0000	width = 44.369
impedance [1]	=	55.63	normalized =	1.1125	width = 35.016
impedance [2]	=	70.71	normalized =	1.4142	width = 18.804
impedance [3]	=	89.89	normalized =	1.7977	width = 8.617
impedance [4]	=	100.00	normalized =	2.0000	width = 5.717

Resistor [1]	=	494.32	normalized =	9.8864
Resistor [2]	=	190.88	normalized =	3.8177
Resistor [3]	=	165.13	normalized =	3.3026

Table 1(b) Preliminary data for a 3-stage power divider model obtained form a code in Appendix A.

For Substrate parameters are -
er = 10.8, H = 50, T =0.001

Other parameters of the design -

Number of stages	N =	5
Input impedance	z0 =	50
Load impedance	zl =	100
Bandwidth ratio	bw =	4.00
Low end frequency	f1 =	1.00
high end frequency	f2 =	4.00
center frequency	f0 =	2.50
fractional bandwidth	fbw =	1.20
low end phase	p1 =	36.00
high end phase	p2 =	144.00
width of microstrip	W =	44.37
quarter wave length	L =	440.53
VSWR max. port 1	S1 =	1.048
VSWR max. port 2 &3	S23 =	1.010
Isolation max.	I23 =	33.88 dB

impedance [0]	=	50.00	normalized =	1.0000	width = 44.369
impedance [1]	=	53.55	normalized =	1.0710	width = 38.195
impedance [2]	=	60.29	normalized =	1.2058	width = 28.852
impedance [3]	=	70.71	normalized =	1.4142	width = 18.804
impedance [4]	=	82.93	normalized =	1.6587	width = 11.427
impedance [5]	=	93.37	normalized =	1.8674	width = 7.480
impedance [6]	=	100.00	normalized =	2.0000	width = 5.717

Resistor [1]	=	754.10	normalized =	15.0820
Resistor [2]	=	391.35	normalized =	7.8270
Resistor [3]	=	225.57	normalized =	4.5114
Resistor [4]	=	135.00	normalized =	2.7000
Resistor [5]	=	248.40	normalized =	4.9680

Table 1(c) Preliminary data for a 5-stage power divider model obtained form a code in Appendix A.

For Substrate parameters are -
er = 9.6, H = 10, T =0.001

Other parameters of the design -

Number of stages	N =	7
Input impedance	z0 =	50
Load impedance	zl =	100
Bandwidth ratio	bw =	10.00
Low end frequency	f1 =	1.00
high end frequency	f2 =	10.00
center frequency	f0 =	5.50
fractional bandwidth	fbw =	1.64
low end phase	p1 =	16.36
high end phase	p2 =	163.64
width of microstrip	W =	9.96
quarter wave length	L =	210.73
VSWR max. port 1	S1 =	1.180
VSWR max. port 2 &3	S23 =	1.036
Isolation max.	I23 =	22.34 dB

impedance [0]	=	50.00	normalized =	1.0000	width = 9.956
impedance [1]	=	56.37	normalized =	1.1274	width = 7.706
impedance [2]	=	60.25	normalized =	1.2050	width = 6.608
impedance [3]	=	65.09	normalized =	1.3017	width = 5.465
impedance [4]	=	70.71	normalized =	1.4142	width = 4.389
impedance [5]	=	76.82	normalized =	1.5364	width = 3.463
impedance [6]	=	82.99	normalized =	1.6597	width = 2.730
impedance [7]	=	88.70	normalized =	1.7740	width = 2.190
impedance [8]	=	100.00	normalized =	2.0000	width = 1.418

Resistor [1]	=	442.56	normalized =	8.8512
Resistor [2]	=	616.62	normalized =	12.3323
Resistor [3]	=	446.08	normalized =	8.9216
Resistor [4]	=	319.88	normalized =	6.3976
Resistor [5]	=	217.43	normalized =	4.3485
Resistor [6]	=	129.71	normalized =	2.5942
Resistor [7]	=	286.02	normalized =	5.7205

Table 1(d) Preliminary data for a 7-stage power divider model obtained form a code in Appendix A.

Parameter	A	B	C
w21 (mils)	2.322	2.322	2.383
w22 (mils)	4.355	4.355	4.713
w23 (mils)	7.324	7.324	8.010
w10 (mils)	9.901	9.901	9.901
len (mils)	952.99	716.04	895.31
R21 (Ω)	107.18	107.18	88.26
R22 (Ω)	211.46	211.46	177.28
R23 (Ω)	400.00	400.00	542.67
S21 (mils)		35.	40.
S22 (mils)		31.75	40.
S23 (mils)		35.	35.05
Isolation	27.75	26.14	33.46
VSWR_1	1.107	1.112	1.076
VSWR_2	1.022	1.019	1.033
BW	2.95	3.02	2.31

where VSWR_1 = S_1 (max) VSWR_2 = $S_{2,3}$ (max)

Isolation = I (min) dB = $-S_{23}$ dB

Column A: uncoupled output arms

Column B: Coupled output arms, optimized parameters are length of each section, and separation distance between two output arms.

Column C: Same as (Column B) except widths of strips in each stage and isolation resistor.

Table 2(a) 3-stage power divider model subjected to optimization. For substrate parameters ε_r=9.6 and H=10 mils.

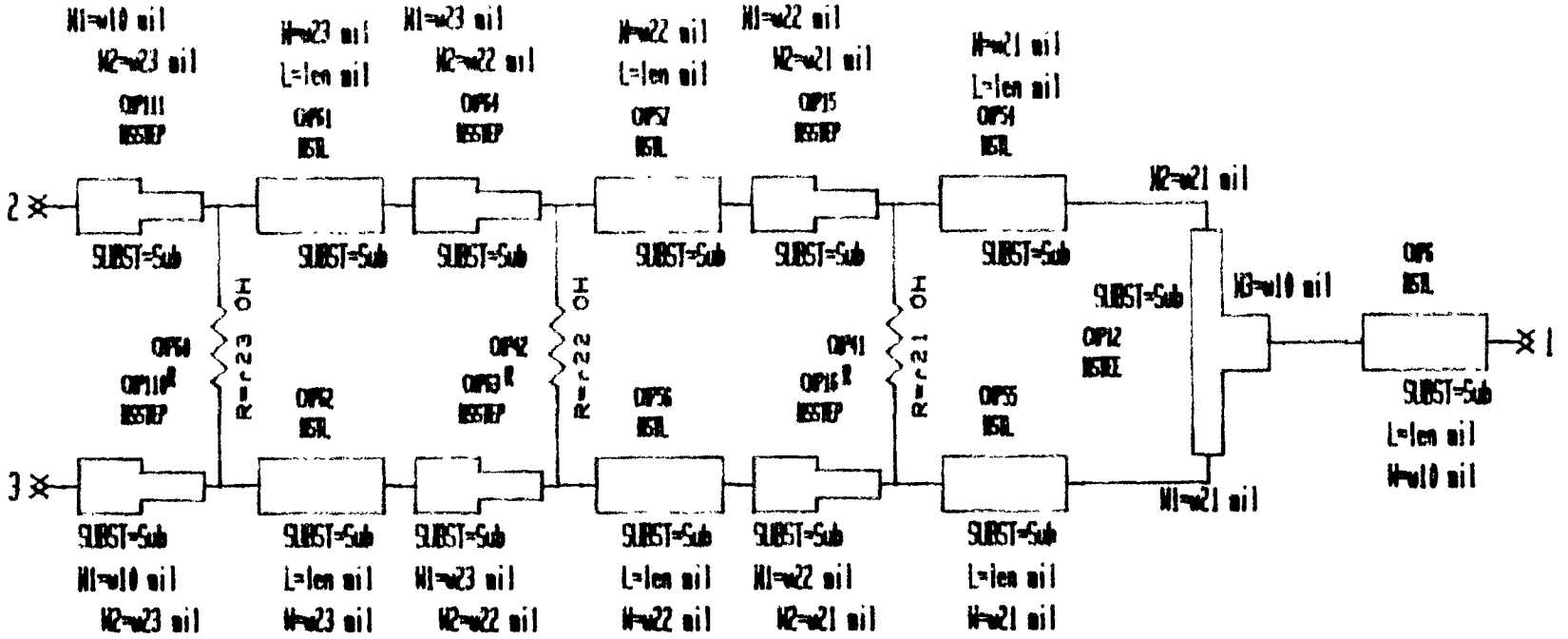


Figure 11(a) Schematic of a three section uncoupled power divider model of Table 2(a), Column A.

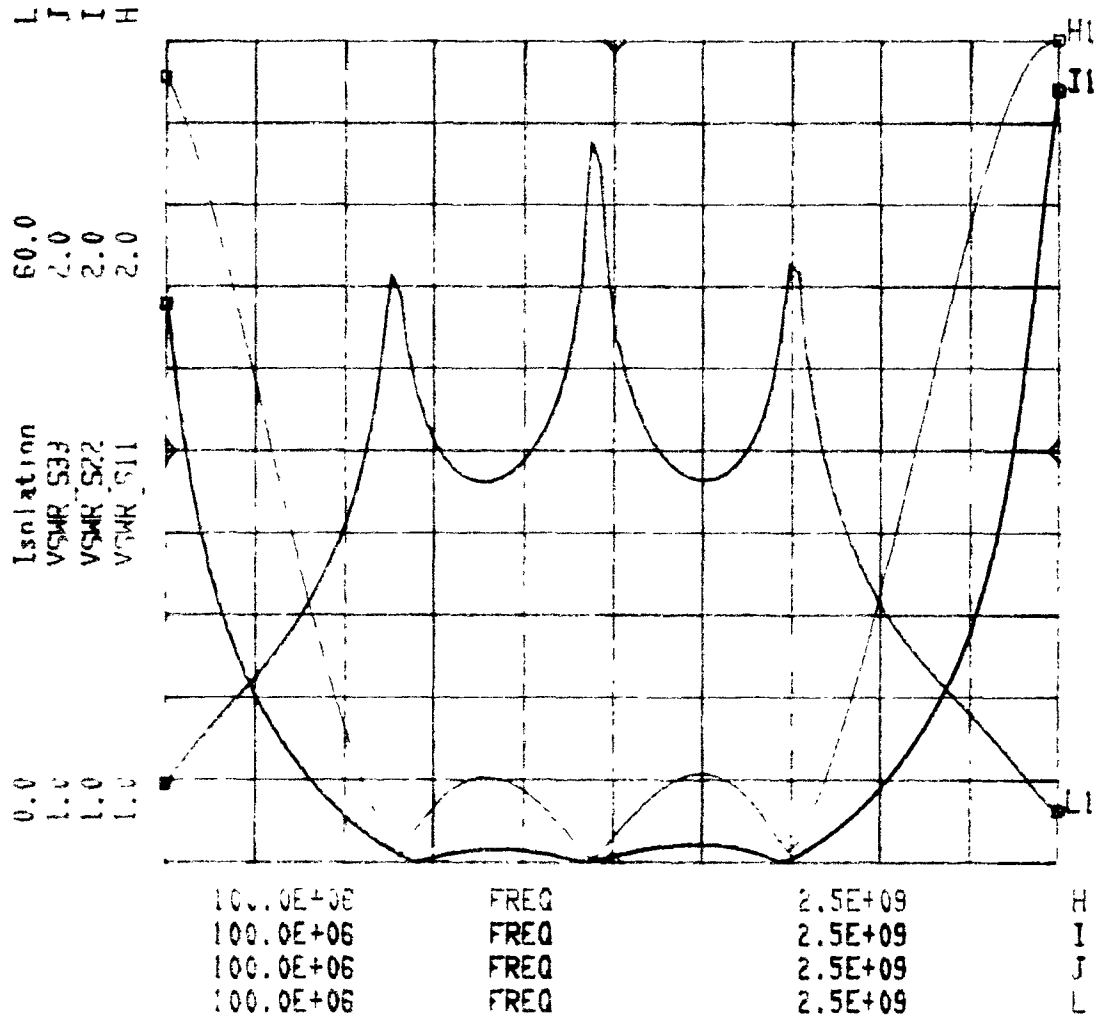


Figure 11(b) Frequency response of a 3-section uncoupled power divider model of Table 2(a), Column A.

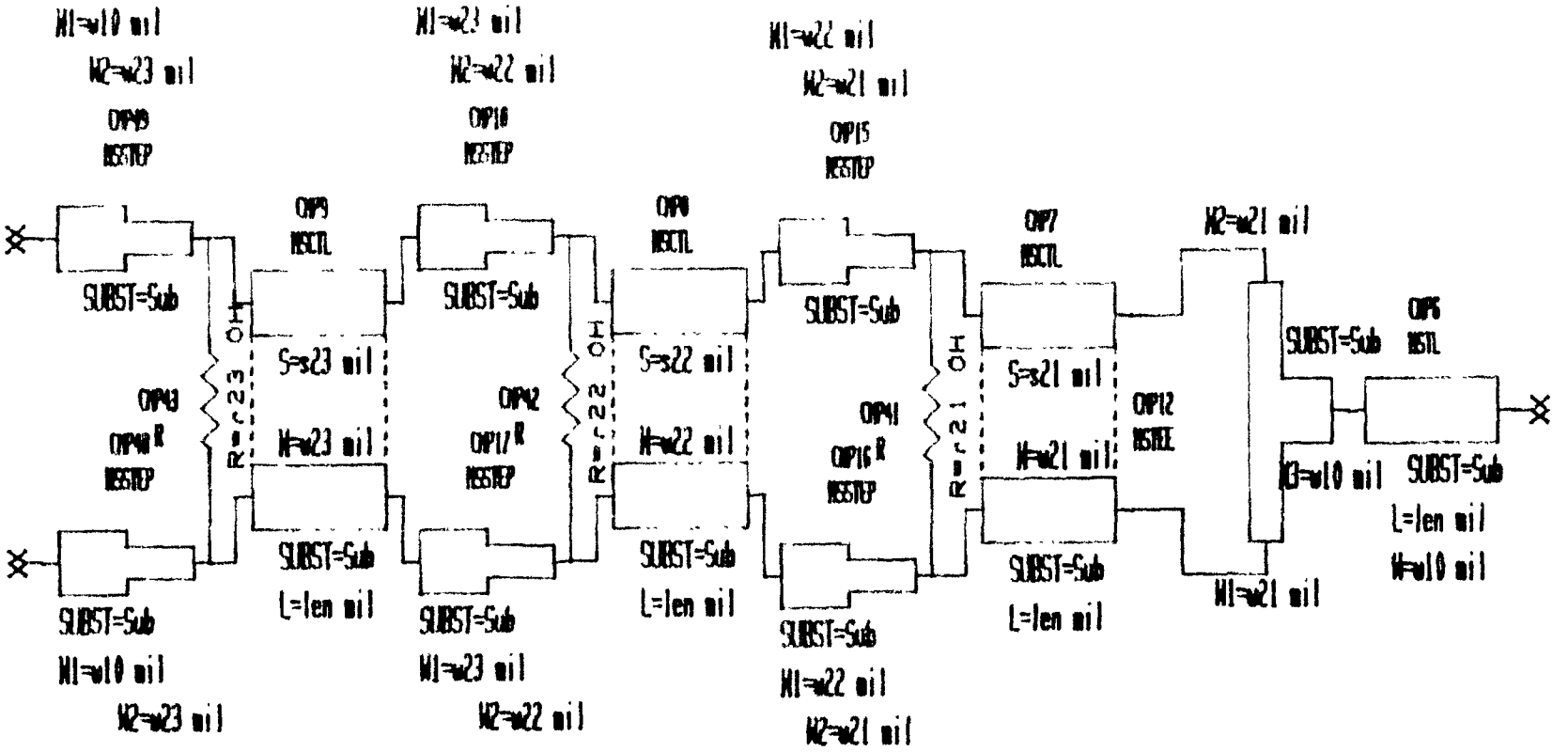


Figure 12(a) Schematic of a three section coupled power divider model of Table 2(a), Column C.

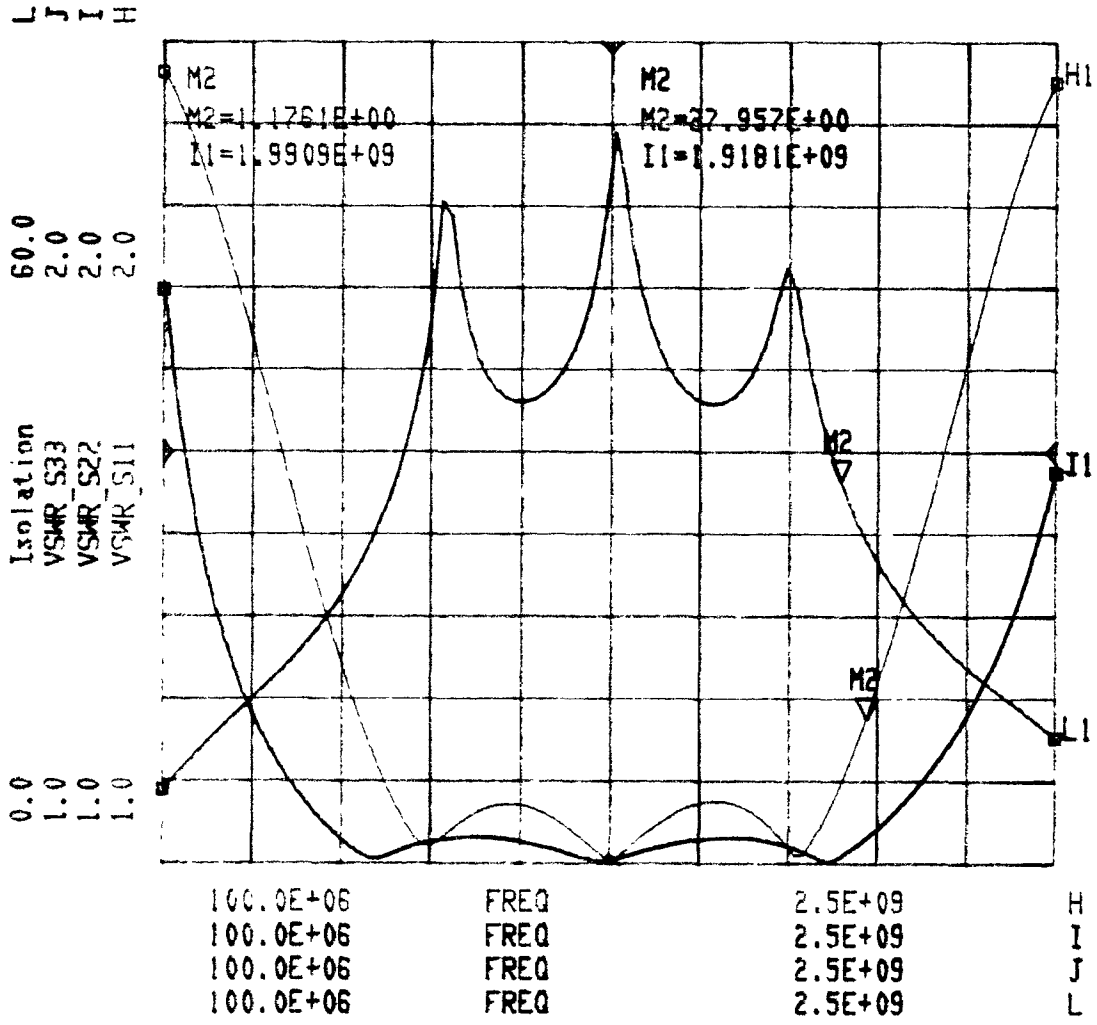


Figure 12(b) Frequency response of a 3-section coupled power divider model of Table 2(a), Column C.

The numerical results based on the code in Appendix A were entered into Microwave Design System and were subjected to further optimization. Table 2(a) depict results for 3-stage model on a 10 mils high substrate. Based on minimum isolation in the passband the uncoupled model between two arms yielded 27.75 dB (Column A). However if coupling is considered, the isolation remained constant for optimized values of the separation between coupled lines (Column B). If the width of the strip in each individual stage is subjected to optimization, results in higher isolation of 33.46 dB in the pass band. The schematic diagrams and the frequency behavior of the model in Columns A and C are given in Figures 11(a),(b) and 12(a),(b) respectively.

The schematic model for an uncoupled three section power divider is shown in Figure 11(a). The microstrip transmission line is represented with three attributes, substrate name, length of a line and width of a line. Tee junction has attributes which define the width of the strip at each of the three ports. In a resistor the value of the resistance is the only attribute. A step discontinuity is also modeled with attributes of the substrate name and the width of each of the two ports. Note that the last step discontinuity was placed before the output ports in an attempt to model the mismatch between the impedance of the last section and the load. In the coupled case, Figure 12(a), is very similar to the uncoupled case, except the transmission line model is replaced by the coupled model. The attributes for the coupled lines are the name of substrate, length of a line, width of a line and separation distance between the two lines.

The length variable is 'len' and the width variables are 'w10' for the line between port 1 and the T-junction, and 'w21' for the strip adjacent to the T-junction. The numbers keep increasing as each section is placed further away from the T-junction, until '2N' where N is the number of sections. Each section consists of a transmission line or coupled transmission line, a resistor and a step discontinuity. The optimization goals, for all the cases are, $S_{1max}=1.05$, $S_{2,3max}=1.03$ and isolation, $I_{min}=40$ dB over a specified frequency range.

	A	B	C	D
VSWR_1	1.105	1.098	1.107	1.076
VSWR_2	1.038	1.020	1.022	1.033
Isolation	27.9	27.59	27.75	33.46
Z1	1.1497	1.1487	1.1496	1.1048
Z2	1.4142	1.4142	1.4142	1.3736
Z3	1.7396	1.7411	1.7396	1.7260
R1	8.0	7.7250	8.0	10.8534
R2	4.2292	4.0902	4.2292	3.5456
R3	2.1436	1.9559	2.1436	1.7652

where VSWR_1 = S_1 (max) VSWR_2 = $S_{2,3}$ (max)

Isolation = I (min) dB = $-S_{23}$ dB

Column A: Theoretical results from [2]

Column B: Numerical results from program in Appendix A

Column C: Uncoupled output arms

Column D: Coupled output arms

Table 2(b) Comparison of results for a 3-stage power divider model with preliminary numerical data for substrate parameters ε_r = 9.6, H = 10 mils, and T =0.001 mils

	A	B	C	D
VSWR_1	1.105	1.027	1.054	1.052
VSWR_2	1.038	1.005	1.041	1.041
Isolation	27.9	38.9	39.47	36.63
Z1	1.1497	1.1125	1.0874	0.9672
Z2	1.4142	1.4142	1.4046	1.1394
Z3	1.7396	1.7977	1.8524	1.5146
R1	8.0	9.8864	10.0	80.0
R2	4.2292	3.8177	3.5138	2.5294
R3	2.1436	3.3026	1.8202	0.9875

where VSWR_1 = S_1 (max) VSWR_2 = $S_{2,3}$ (max)

Isolation = I (min) dB = $-S_{23}$ dB

Column A: Theoretical results from [2]

Column B: Numerical results from program in Appendix A

Column C: Uncoupled output arms

Column D: Coupled output arms

Table 2(c) Comparison of results for a 3-stage power divider model with preliminary numerical data for substrate parameters ε_r = 10.8, H = 50 mils, and T =0.001 mils

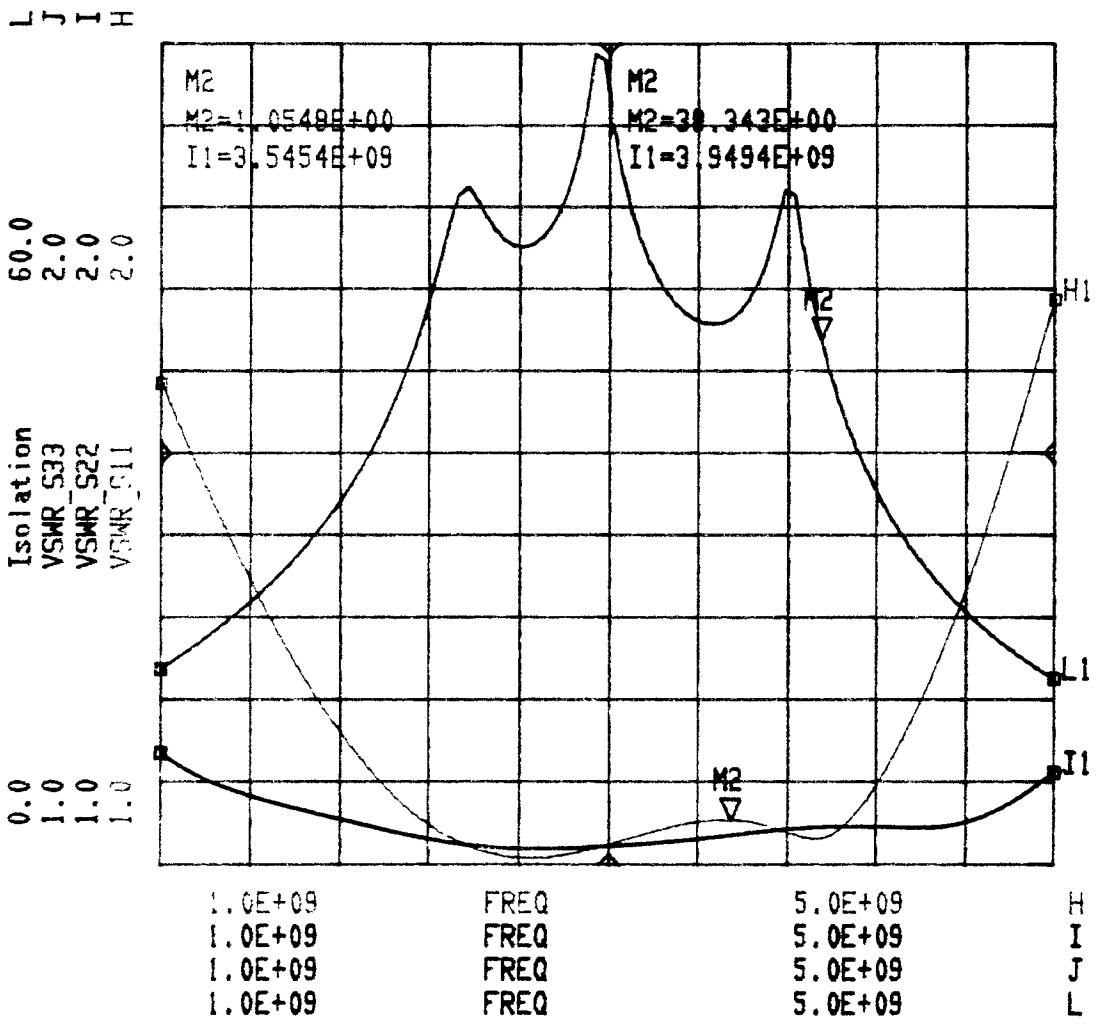


Figure 13(a) Frequency response of a 3-section uncoupled power divider model of Table 2(c), Column C.

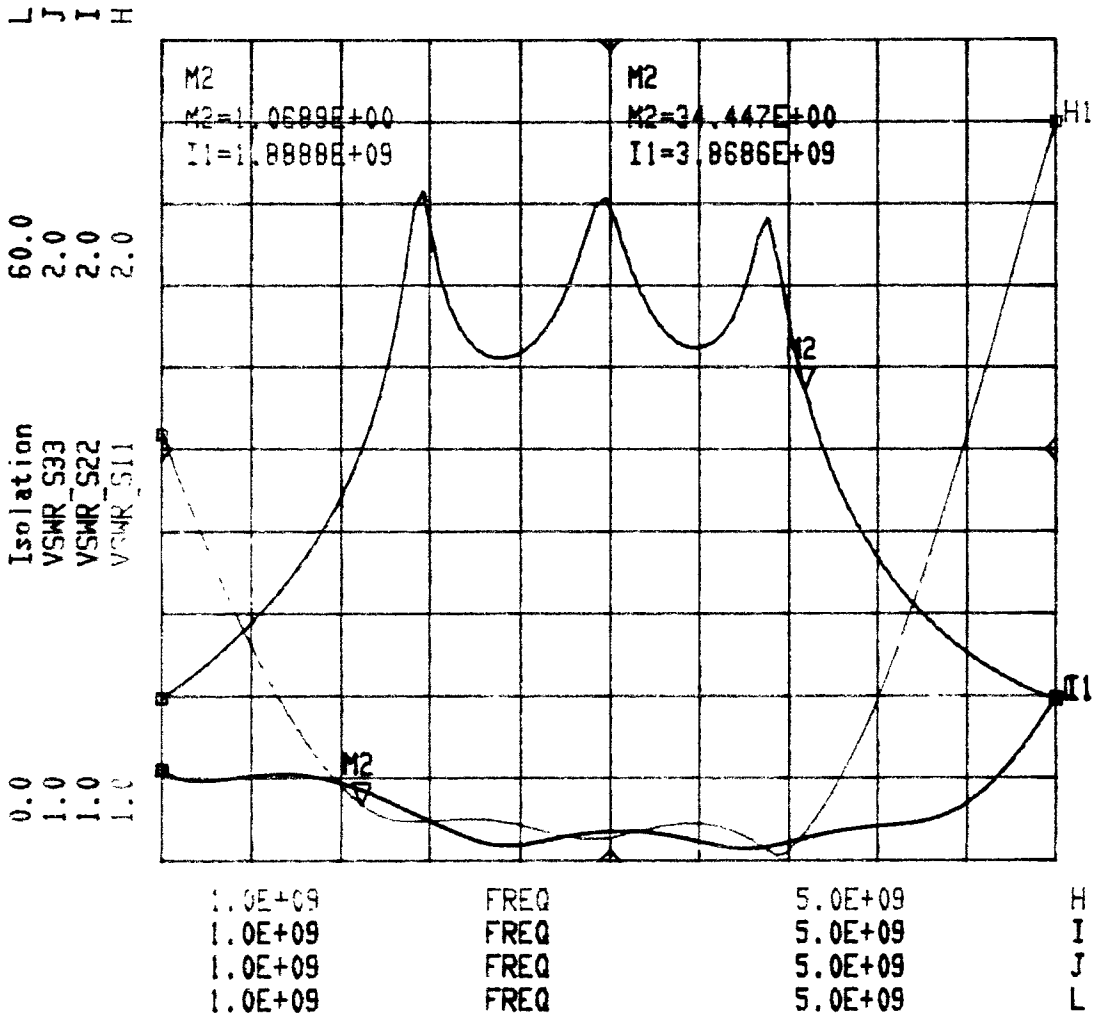


Figure 13(b) Frequency response of a 3-section coupled power divider model of Table 2(c), Column D.

The optimized results of Table 2(a) were further compared to the theoretical ones [2] and the numerical data obtained from the code in Appendix A in Table 2(b). One obvious conclusion is that isolation in the passband is maximum when coupling between two lines occurs. Additionally coupling consideration leads to higher values for isolation resistors. Table 2(c) demonstrates various comparisons between analytical and optimized results for ε_r = 10.8, H = 50 mils 3-stage model. Frequency response of the model in Table 2(c) for uncoupled (Column C) and coupled (Column D) are given in Figures 13(a) and 13(b), respectively. Note that optimized values for separation between two coupled lines of Table 2(c) (Column D) for individual stages are 38.51, 31.04 and 50.0 mils. Comparison of Figure 13(a) and 13(b) shows not too much improvement is introduced due to coupling effects.

For the five section power divider model, the substrate parameters are ε_r = 10.8 and H = 50 mils. Table 3 has the optimized values obtained for the uncoupled and coupled cases with $R_{max}=4000\Omega$ and $R_{max}=600\Omega$. The optimized values for the separation between the strips do not show monotonic variation. The value of the width of the last strip for $R_{max}=4000\Omega$ is 50 mils, where the 50Ω line has a width of 44.095 mils, also the length of each section is doubled compared to the uncoupled case. The resistor values for the first and second sections turned out to be same, of 40Ω. Similarly for $R_{max}=600\Omega$, the last two sections before the output ports have identical resistance values of 600Ω. In Table 3, Columns A and B have monotonic isolation resistor values, whereas (Column C) does not follow this monotonic behavior. Figure 14(a) shows the uncoupled case, the bandwidth is calculated with the last lobe of the curve being ignored since the isolation value is 23.46 dB and the VSWR at port 1 is 1.34. Hence, it results in the bandwidth of 4.45 and $I_{min}=27.31$ dB, $S_{1max}=1.15$ and $S_{2,3max}=1.1$. The first coupled case with $R_{max}=4000\Omega$ shows higher isolation and is almost uniform in the passband, and the values of the VSWR are about 1.05. With $R_{max}=600\Omega$, the coupled five section power divider behaves as if it has two sections, because there are only two zeros in the isolation curve and VSWR curves. This results in $I_{min}=28.69$ dB, $S_{1max}=1.08$ and $S_{2,3max}=1.05$ with a bandwidth of 1.85.

Parameter	A	B	C
w21 (mils)	7.329	9.456	13.545
w22 (mils)	13.677	16.514	21.376
w23 (mils)	19.143	25.923	33.462
w24 (mils)	27.791	42.167	37.453
w25 (mils)	36.688	50.0	43.073
w10 (mils)	44.095	44.095	44.095
len (mils)	292.16	419.22	188.88
R21 (Ω)	118.66	40.0	361.47
R22 (Ω)	174.12	40.0	68.71
R23 (Ω)	295.32	71.82	433.32
R24 (Ω)	394.60	173.32	600.0
R25 (Ω)	600.0	4000.0	600.0
S21 (mils)		44.592	40.911
S22 (mils)		30.795	25.508
S23 (mils)		39.012	14.506
S24 (mils)		32.825	50.0
S25 (mils)		50.0	50.0
Isolation	27.31	31.14	28.69
VSWR_1	1.15	1.06	1.08
VSWR_2	1.09	1.04	1.05
BW	4.45	2.92	1.85

where VSWR_1 = S_1 (max) VSWR_2 = $S_{2,3}$ (max)

Isolation = I (min) dB = $-S_{23}$ dB

Column A: uncoupled output arms

Column B: Coupled output arms, with $R_{max} = 4000\Omega$

Column C: Coupled output arms, with $R_{max} = 600\Omega$

Table 3 5-stage power divider model subjected to optimization. Substrate parameters are $\varepsilon_r = 10.8$ and H = 50 mils

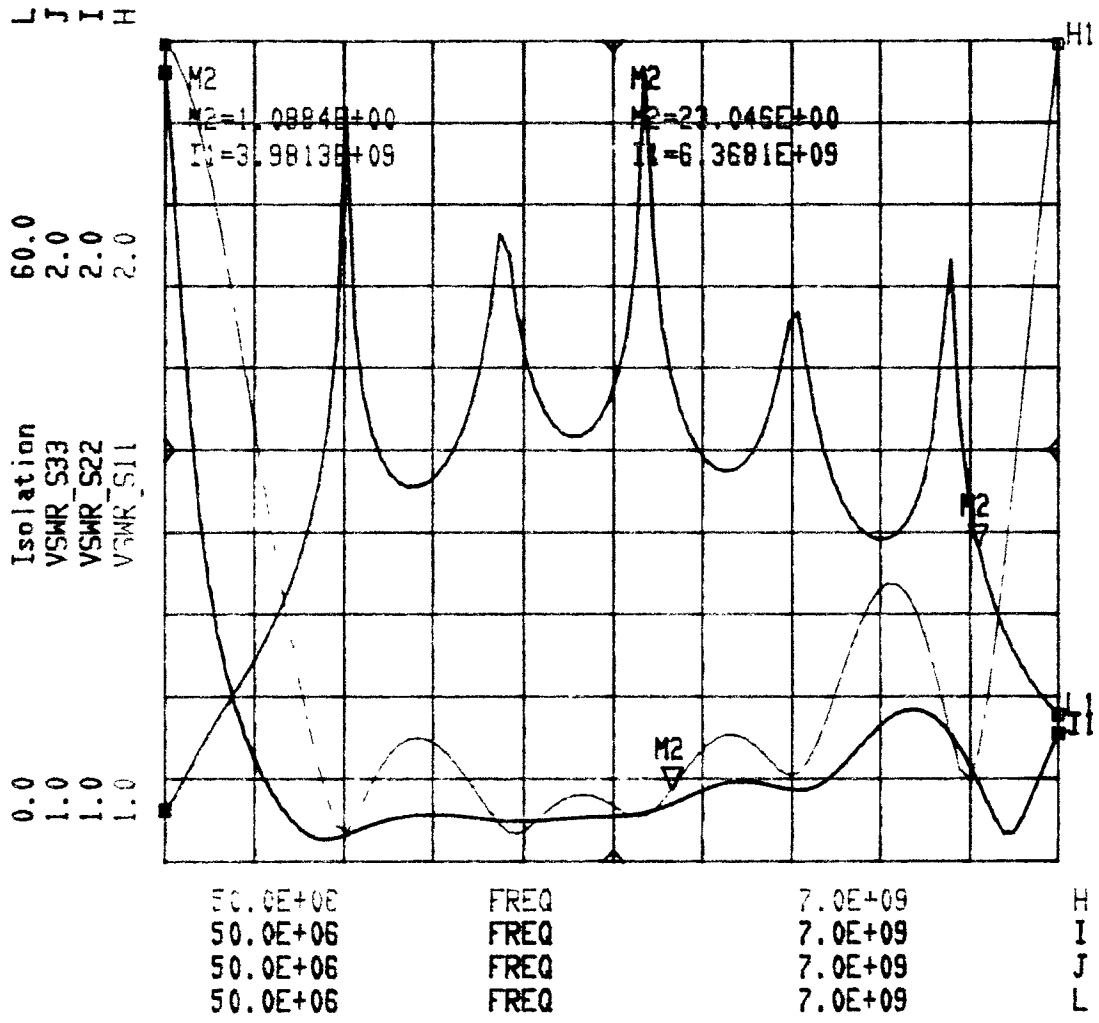


Figure 14(a) Frequency response of a 5-section uncoupled power divider model of Table 3, Column A.

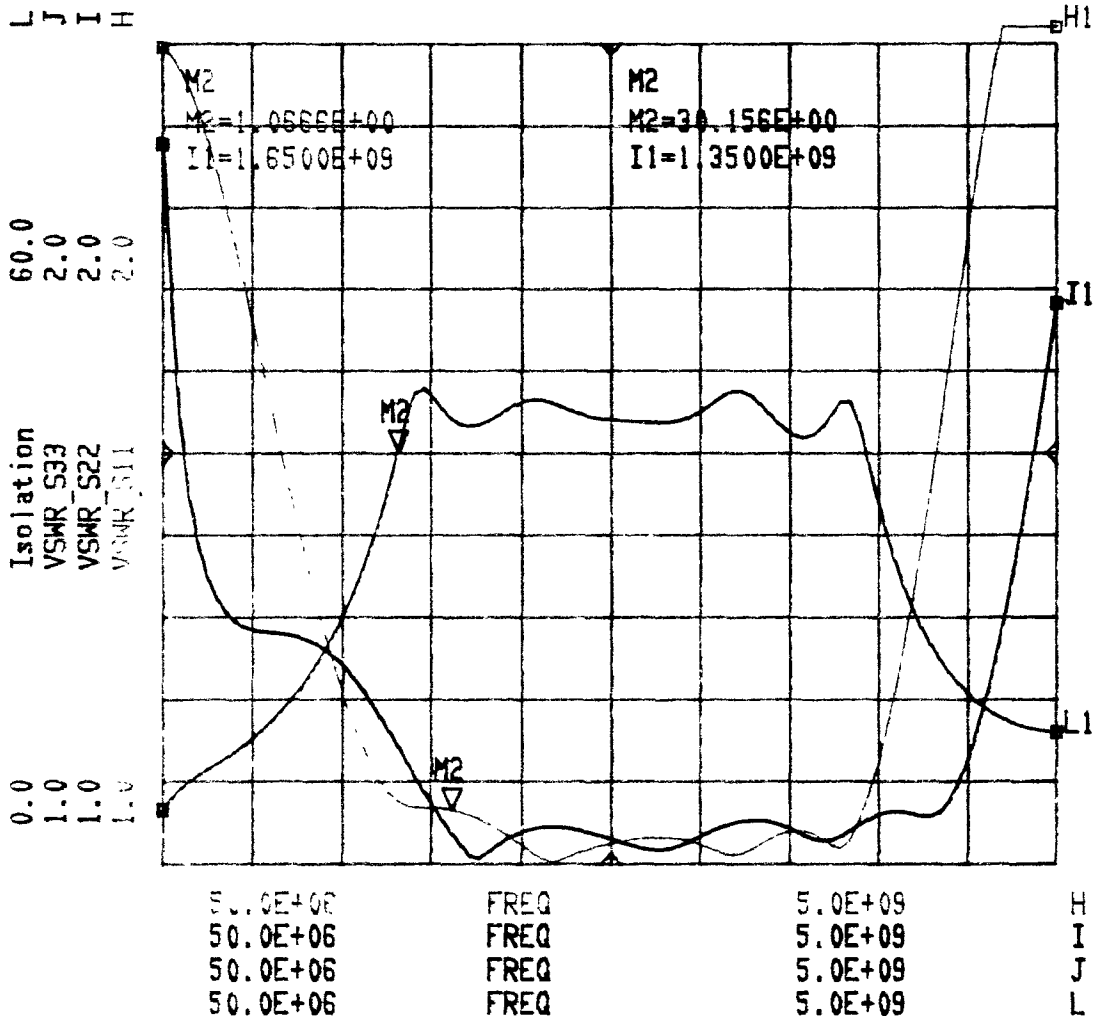


Figure 14(b) Frequency response of a 5-section coupled power divider model of Table 3, Column B.

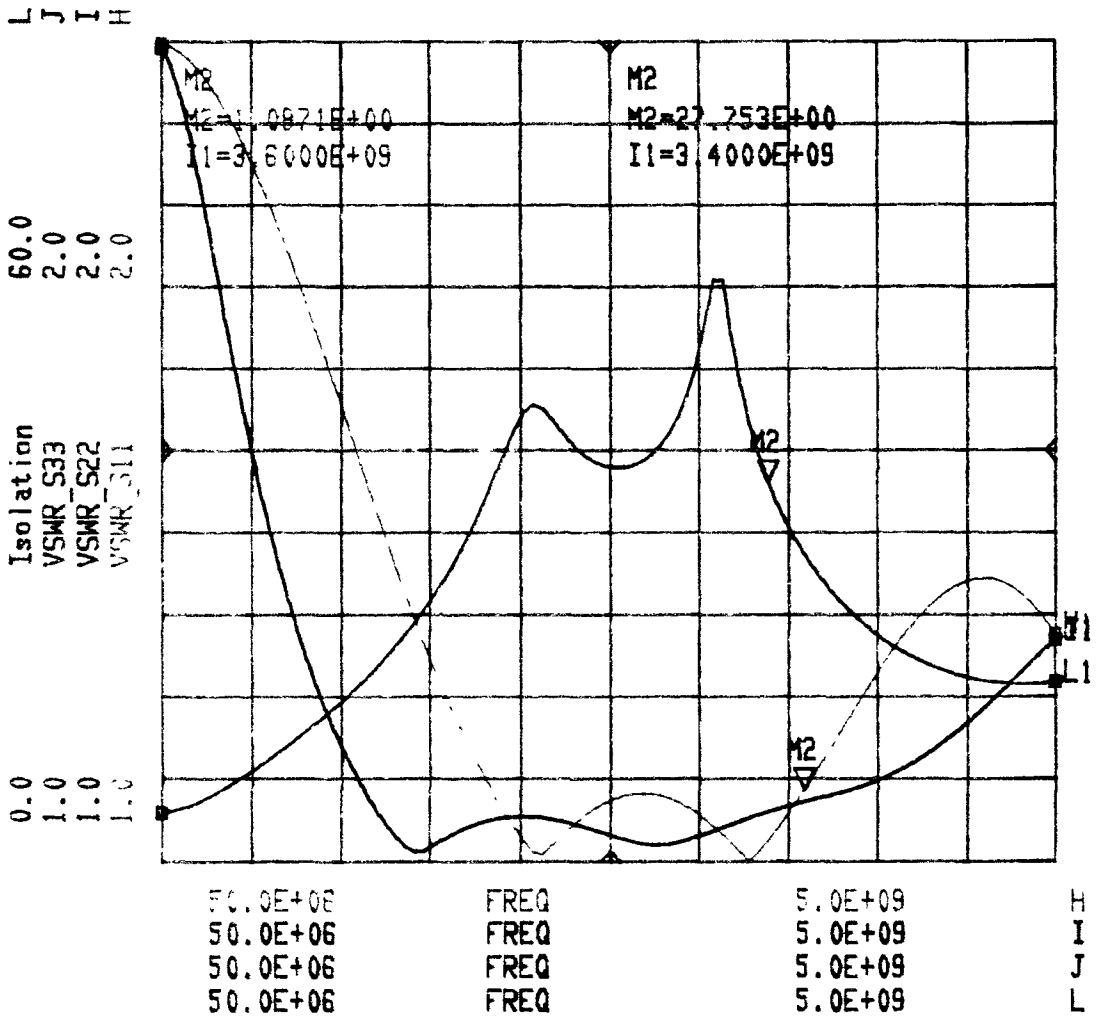


Figure 14(c) Frequency response of a 5-section coupled power divider model of Table 3, Column C.

Parameter	Uncoupled	Coupled
w21 (mils)	2.173	2.533
w22 (mils)	2.709	3.342
w23 (mils)	3.436	3.385
w24 (mils)	4.355	6.077
w25 (mils)	5.426	5.964
w26 (mils)	6.562	7.389
w27 (mils)	7.657	8.784
w10 (mils)	9.901	9.901
len (mils)	233.61	210.89
R21 (Ω)	248.26	89.63
R22 (Ω)	129.62	234.45
R23 (Ω)	217.58	169.27
R24 (Ω)	319.90	1043.67
R25 (Ω)	446.23	485.19
R26 (Ω)	616.15	715.25
R27 (Ω)	422.48	3709.56
S21 (mils)		11.49
S22 (mils)		10.68
S23 (mils)		24.89
S24 (mils)		10.14
S25 (mils)		39.81
S26 (mils)		35.0
S27 (mils)		32.83
Isolation	21.67	33.5
VSWR_1	1.22	1.10
VSWR_2	1.09	1.07
BW	9.29	6.84

where VSWR_1 = S_1 (max) VSWR_2 = $S_{2,3}$ (max)

Isolation = I (min) dB = $-S_{23}$ dB

Table 4 7-stage power divider model subjected to optimization. Substrate parameters ε_r=9.6 and H=10 mils

In the case of a seven section power divider model, the parameters are ε_r = 9.6 and H = 10 mils. For the uncoupled case, results are tabulated in Table 4 and are shown in Figure 15(a) and 15(b). The performance limits are I_{min}=21.67 dB, S_{1max}=1.22 and $S_{2,3max}$=1.09 for a bandwidth of 9.29:1. Cohn achieved I_{min}=19.4 dB, S_{1max}=1.206 and $S_{2,3max}$=1.098 for a 10:1 bandwidth. In the coupled case the I_{min}=35.15 dB, S_{1max}=1.09 and $S_{2,3max}$=1.08 and a bandwidth of 7.15:1. One can observe that there is a good improvement in the performance limits due to optimization. The resistor values for the uncoupled case do not show monotonic change, but in the coupled case they are monotonic with a wider range of values. The VSWR for the coupled case yields lower values than the uncoupled case approximately by a factor of 0.1.

The substrate with ε_r = 9.6 and H = 10 mils was chosen finally because alumina is a popular substrate material. The simulator having limits to the built-in equations, forced the height to be chosen as 10 mils so the design of the power divider would be more accurate.

An alternative substrate was also chosen which is more suitable for fabrication of the design of the power divider. The specifications of this duriod substrate are ε_r = 10.8 and H = 50 mils, and the practical maximum resistor value was chosen as 600Ω due to availability numerically. The restrictions in the simulator MDS required that the built-in equations were used up to about f = 5 GHz for a substrate height of 50 mils, and resulted in inaccurate response beyond 5 GHz.

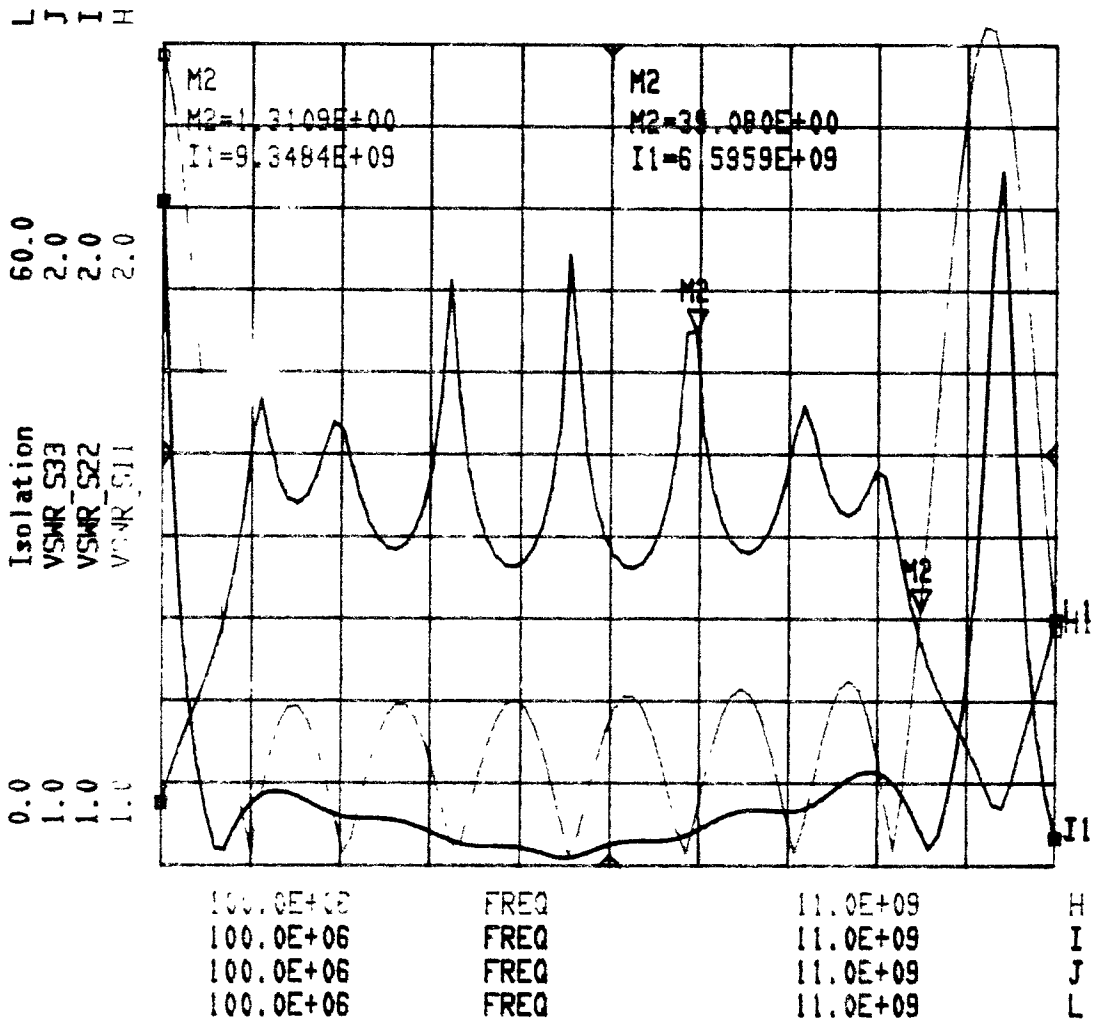


Figure 15(a) Frequency response of a 7-section uncoupled power divider model of Table 4, Column A.

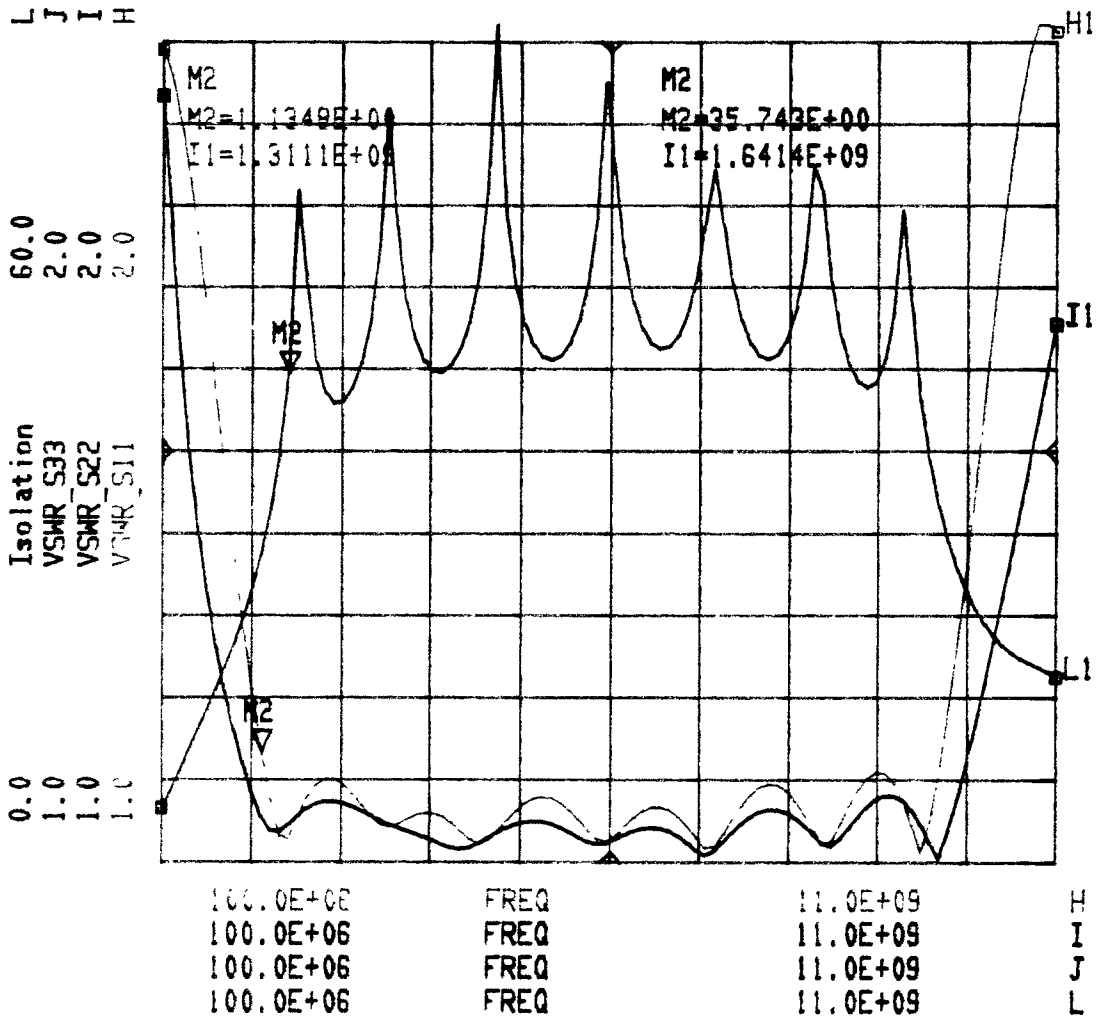


Figure 15(b) Frequency response of a 7-section coupled power divider model of Table 4, Column B.

CHAPTER 5
CONCLUSIONS

The conventional technique used to design wide band power divider uses multisection quarterwave transmission lines based on the Chebyshev polynomial approximation. To improve isolation and matching, isolation resistors are placed following each stage. In this thesis, results based on this approach were further extended to improve the performance. These results were used as a starting solution in a microwave simulator and were subject to further optimization for preset goals in performance. Furthermore, coupling between adjacent lines was taken into account, which has not been previously reported in the open literature for wide band microwave power divider design. The overall performance for coupled and uncoupled lines in the power divider design were compared. It is observed that optimization and coupling results in a better performance compared to conventional approach. Currently, the designed components are being fabricated to verify the validity of the design approach introduced in this thesis.

APPENDIX A

C++ Program

```
/* PDIV.C */
/* To analyze a power divider using odd and even mode analysis. */
/* To calculate the "Optimum Design of Stepped Transmission-Line
    Transformer" from S. Cohn. */
#include <stdio.h>
#include <math.h>
#include <complex.h>

#define PI 3.14159265358979323 83
#define C (3E+8*1E+5/2.54)
#define max_N 21
/*
float er = 10.8;
int H = 50;
float T = 0.001;
float res = 1.673; /* metal CU - units micro.ohm.cm */
*/
float p = 90;

int N,z0,zl,H = 0;
float   bw,f1,p1,er,T;

/* To get information from the user */
void  getinfo  ()
{
  printf ("                          For a power divider - ");
  printf ("       For Substrate parameters are - ");
  printf ("                          Enter dielectric constant er   ");
  scanf("%f",&er);
  printf ("                    height of substrate  H (mils)   ");
  scanf("%d",&H);
  printf ("              thickness of metalization  T (mils)   ");
  scanf("%f",&T);
  printf ("                       Enter number of stages  N   ");
  scanf("%d",&N);
  printf ("                     input impedance  z0  (ohms)   ");
  scanf("%d",&z0);
  printf ("                      load impedance  zl  (ohms)   ");
  scanf("%d",&zl);
  printf ("                  bandwidth ratio   bw = (f2/f1)   ");
  scanf("%f",&bw);
  printf ("                    low end frequency  f1  (GHz)   ");
  scanf("%f",&f1);
  printf ("     er = %5.1f,   H = %2d,   T =%5.3f ",er,H,T);
  printf ("      Other parameters of the design - ");
  printf ("      Number of stages          N = %3d ",N);
  printf ("      Input impedance           z0 = %3d ",z0);
  printf ("      Load impedance             zl = %3d ", zl);
```

```
  printf ("      Bandwidth ratio          bw = %6.2f ",bw);
  printf ("      Low end frequency        f1 = %6.2f ",f1);
}

/* Function - to calculate the Chebyshev polynomial */
float calcheb (int M, float x)
{
 int  i;
 float Tx[max_N];
 /* printf ("      Chebyshev polynomial "); */
 Tx[0] = 1;
 Tx[1] = x;
 for (i=2; i <=M; i++)
 {
  Tx[i] = 2*x*Tx[i-1] - Tx[i-2];
 }
 /* printf (" T[%d] = %6.2f ",M,Tx[M]); */
 return Tx[M];
}

/* Function - calculate all other small variables */
void calcinfo ()
{
  float    f2,f0,fbw,p2,L,XA,XW,wl0,S1,S23,I23,eeff,he,We,cheb,temp;
  f2 = bw*f1;
  f0 = (f1+f2)/2;
  fbw = 2*((f2-f1)/(f1+f2));
  p1 = 180/(1+bw);
  p2 = 180-p1;
  printf ("      high end frequency       f2 = %6.2f ",f2);
  printf ("      center frequency         f0 = %6.2f ",f0);
  printf ("      fractional bandwidth   fbw = %6.2f ",fbw);
  printf ("      low end phase            p1 = %6.2f ",p1);
  printf ("      high end phase           p2 = %6.2f ",p2);
  temp = (0.4516+0.2416/er);
  XA = z0*sqrt(2*(er+1))/119.9 + (er-1)/(2*(er+1))*temp;
  XW = H*(8/(exp(XA)-2*exp(-XA)));
  he = H - (2*T);
  We = XW + (T/PI*(log(2*he/T)+1));
  temp = pow((1+12*H/We),-.5);
  eeff = (er+1)/2 + ((er-1)/2*(temp+0.04*pow((1-We/H),2)));
  wl0 = C/(f0*1E+9*pow(eeff,.5));
  L = wl0/4;
  cheb  =  calcheb((N-1),(1/(cos(p1*PI/180))));
  S1 = 1 + log(zl/z0)/cheb;
  S23 = 1 + 0.2*(S1 - 1);
  I23 = 20*log10(2.35/(S1-1));
  printf ("      width of microstrip      W = %6.2f ",XW);
  printf ("      quarter wave length      L = %6.2f ",L);
  printf ("      VSWR max. port 1        S1 = %6.3f ",S1);
  printf ("      VSWR max. port 2 &3    S23 = %6.3f ",S23);
  printf ("      Isolation max.         I23 = %6.2f dB",I23);
}
```

```
/* Function - calculate am (appendix II) */
void am_func (ae)
float   *ae;
{
  int  i,  j;
  float zam[max_N][max_N],temp;
  /* to clear the array */
  for (i=1; i<=N; i++)
   for (j=1; j<=N+1; j++)
     zam[i][j]  =  0;
  zam[1][1]  =  2;
  zam[2][2]  =  1/cos(p1*PI/180);
  for (i=3; i<=N; i++)
  {
    zam[i][1]  =  (zam[i-1][2]*  2*zam[2][2]  -  zam[i-2][1]);
    for (j=2; j<=i; j++)
    {
      temp  =  (zam[i-1][j-1]+zam[i-1][j+1]);
      zam[i][j]  =  (temp*zam[2][2]  -  zam[i-2][j]);
    }
  }
  i= 1;
  for (j=N; j>=1; j-=2)
  {
   ae[i]  =  ae[N+1-i]  =  zam[N][j]/zam[N][N];
   i += 1;
  }
}

/* Function - to calculate the reflection coefficient */
void  calref  (ae)
float   *ae;
{
 int   i;
 float    ref[max_N],refl;
refl  =  0;
 for (i=1; i<=N; i++)
 {
   ref[i]    =    2*ae[i]*cos(2*(i-1)*p*PI/180);
   refl  +=  ref[i];
   if (N % 2 == 0)
     refl  +=  2*ae[N/2]*cos(p*PI/180);
   else
     refl  +=  ae[(N+1)/2];
 }
}

/* Function - to calculate the impedances */
void  calimp  (ay,ae)
float   *ay,*ae;
{
 int   i;
 float xz[max_N],sum,zln[max_N],xw[max_N],XA,temp;
```

```
 sum = 0;
 for (i=1; i<=N; i++)
   sum += ae[i];
 for (i=1; i<=N; i++)
   zln[i]    =    ae[i]*(log(zl/z0))/sum;
 xz[0] = z0;
 for (i=1; i<=N; i++)
   xz[i]    =    xz[i-1]*exp(zln[i]);
 for (i=0; i<=N; i++)
 {
   temp = (er - 1)*(0.4516+0.2416/er);
   XA = xz[i]*sqrt(2*(er+1))/119.9 + temp/(2*(er+1));
   xw[i] = H*(8/(exp(XA)-2*exp(-XA)));
   printf ("      impedance [%d]   = %6.2f",i,xz[i]);
   printf ("       normalized = %6.4f ",xz[i]/z0);
   printf ("      width = %6.3f ",xw[i]);
 }
 ay[0] = 1;
 for (i=1; i<=N; i++)
   ay[i]   =   1/(xz[i]/z0);
}

/* Function for even mode analysis */
void caleven (ey)
float  *ey;
{
 int  i;
 float     eref[max_N],erefl,et[max_N],tot;
 erefl = 0;
 for (i=1; i<=N; i++)
 {
  eref[i]  =  (ey[i-1]  -  ey[i])/(ey[i-1]  +  ey[i]);
  et[i]    =     (4*ey[i-1]*ey[i])/pow((ey[i-1]+ey[i]),2);
  if (i == 1)
    tot = 1;
  else
    tot  *=  et[i-1];
  erefl   +=   2*eref[i]*tot*cos(2*(i-1)*p*PI/180);
 }
 eref[N+1] = (ey[N]-0.5) / (ey[N]+0.5);
 erefl += eref[N+1];
}

/* Function - odd mode analysis */
void calodd (oy)
float  *oy;
{
 int  i;
 float G[max_N],oref[max_N],ot[max_N],g[max_N];
 float     tot,cheb1,cheb2,eS,temp;
 complex   phase,orefl;
 orefl = 0;
 for (i=0; i<=N; i++)
   G[i] = 0;
```

```
 G[1]  =  (1-oy[1]);
 for (i=1; i<=N; i++)
 {
  if (i == 1)
    tot = 1;
  else
    tot *= ot[i-1];
  temp    =    oy[i-1]*tot*(oy[i-1]+oy[i])+2*(oy[i-1]-oy[i]);
  ot[i]   =    (4*pow(tot,2)*oy[i]*pow(oy[i-1],3))/pow(temp,2);
  phase   =  (0,2*(i-1)*p*PI/180);
  orefl   +=   oref[i]*tot*(exp(phase));
  if (i>1)
    G[i]    =     (oy[i-1]-oy[i])/(oy[i-1]*tot);
  oref[i]    =     (oy[i-1]-oy[i]-2*G[i])/(oy[i-1]+oy[i]+2*G[i]);
 }
 cheb1  =  calcheb  (N-1,((PI/2  -  p)/(PI/2-p1)));
 cheb2  =  calcheb  (N-1,cos(p1*PI/180));
 eS  =  1  +  log(zl/z0)*cheb1/cheb2;
 g[1]  =  -2*G[2]  +  (pow(oy[1],2)/(-2*G[1]  +  1  +  0.7*(eS  -  1)));
 for (i=2; i<=N-2; i++)
  g[i]  =   -2*G[i+1]  +  pow(oy[i],2)/g[i-1];
 G[N]  =  fabs(0.5*pow(oy[N-1],2)/g[N-2]);
 oref[N+1] = -1;
 orefl += oref[N+1];
 printf  ("");
 for (i=1; i<=N; i++)
 {
   printf ("      Resistor [%d]     =  %7.2f ",i,z0*1/G[i]);
   printf ("    normalized  =  %8.4f ",1/G[i]);
 }
}

main()
{
  int  i;
  float  a[max_N],y[max_N];
  getinfo  ();
  N +=1;
  calcinfo  ();
  am_func (&a);
  calref  (&a);
  calimp  (&y,&a);
  N -=1;
  caleven  (&y);
  calodd  (&y);
  printf ("                                                    ");
  printf ("              Finally  Done  ...");
  return  0;
}
```

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