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# A transistor delay model based on charge conservation

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# A Transistor Delay Model
# Based on Charge Conservation

by

**Bharatsingh K. Bisen**

Submitted to the Departement of Electrical Engineering of the New Jersey Institute of Technology in partial fulfillment of the requirement for the degree of Master of Science in Electrical Engineering.

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# Abstract

Delay information of a circuit is often used in the areas of timing verification, timing analysis, race detection and circuit optimization. Given a circuit its delay can be estimated by various simulation techniques. SPICE is one of the simulation techniques, but it is seen that with the increase in the complexity of the circuit the SPICE circuit simulation technique to obtain delay information become cumbersome and computationally too expensive. So as to overcome the above disadvantages of the circuit simulation technique to obtain delay information various timing delay models were developed. However general survey of most of these timing delay model show that they suffer from the problem of accuracy while estimating the delay of a given circuit.

The previous model used to work with linear RC-approach method treating the transistor as a device represented by a fixed resistance and capacitance with a scale factor, without considering the effect of input waveform and non-linearities of MOS on delay. The error in delay estimation is roughly ranging from 30% to 40%.

The main objective of the thesis is to develop a timing delay model which has higher accuracy and precisely resembles the circuit simulation techniques. The Timing delay model, based on charge conservation principle is used for estimating accurately the delay in a circuit. The basic principle of charge conservation, i.e the time taken by the capacitor to discharge (fall time estimation) and the time taken by the capacitor to charge (rise time estimation).

After a large number of simulation on the model for various conditions of the capacitive load and input waveform effect, the timing delay model gave fairly accurate results, with an error ranging from 2% to 8% as compared to 30% to 40% of earlier models, and takes less CPU time for calculation of delay.

# ACKNOWLEDGEMENT

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# Chapter 1

# INTRODUCTION

Given a circuit and the shape of the input waveform, the output of the circuit can be predicted, depending on the circuit configuration. One of the main objectives of the circuit designers, is to ensure that the circuit meets the application requirements. It means for a given input to the circuit, the designers need to know accurately when the output is available, hence when dealing with the aspect of speed in VLSI circuits which plays a major role, it becomes essential to determine the delay in propagation which is a main measure of speed.

Delay information of a circuit is often used in the areas of timing verification, timing analysis, and circuit optimization. The purpose of timing analyzer is to predict the operating speed of a VLSI chip before it is fabricated. The speed of a circuit is a function of many factors, one of which is the manufacturing process. Over- and under etching, oxide growth rates, and ion-implantation level, all these affect the electrical characteristics of the resulting circuit. In particular they affect transistor sizes, threshold voltages, resistance and capacitances. Accuracy of delay

information of a functional block, affects very much the performance of the final product.

There are various circuit simulation techniques which are used to simulate the circuit performance, among them SPICE is one of the well known circuit simulation techniques, but it is seen that the circuit level simulators, such as SPICE, while very accurate are prohibitive for all but small circuits, due to their expensive computation time. The logic level simulators perform very little transient analysis, and hence to compromise between computation time and accuracy, various transistor modeling techniques have been proposed in the past.

There has been enormous demand in the VLSI design community to find a solution for fast and accurate timing analysis methodology. Numerous efforts have been made for developing the timing models for CMOS circuits which shall accurately compute the delay of the circuit. Some of them employs rigorous mathematical models which gives fairly good results but it does not have any distinct advantage over the circuit simulation techniques, and also has large deviation in the accuracy. While others have developed models that spend less computational time to calculate the delay of the circuit, but they end up with a over-simplified model which does not take care of various parameters, such as input waveform effect and etc.

Most transistor level analysis use RC (resistor capacitor) delay models, which deviates from the SPICE results by 30% to 40%. These inaccuracies in RC delay results from neglecting the non-linearities of the MOS transistors and from difficulties in including input waveform effects, which are very carefully looked upon in this thesis.

The objective of this thesis is to overcome the inaccuracy problem for calculating the delay in CMOS circuits faced by the existing RC models, by taking a

completely different approach and working on the principle of charge conservation theory in addition to the RC model.

The basic principle behind the approach can be explained by taking a specific case of inverters, where the fall time i.e (the time taken for the output voltage to decrease from supply potential to ground potential) is basically the time taken by the charge stored in the capacitor to discharge entirely and hence making the output voltage to go upto ground potential, similarly the rise time i.e (the time taken by the output to rise from ground potential to supply potential) is basically the time taken by the capacitor to charge to supply potential. We follow the above , basic charge conservation principle to calculate the timing delay in CMOS circuits.

The charge storage in MOSFET consists of capacitance associated with parasitic and intrinsic devices, the parasitic consists of the overlap capacitances of the gate with respect to other three terminals and the capacitance of the junction diodes, bottom and sidewall (periphery), of bulk source and bulk drain junction diodes.

The entire thesis is divided into five chapters where the Chapter2 gives an entire review on the past work done to handle the problem of delay estimation and minimization with their merits and demerits as compared to the developed model.

Chapter3 gives the basic operational details of the CMOS inverter circuit for which the delay model was developed, and related definitions. It describes about the developed model, the basic principle behind the analysis with the explicit numerical approach to achieve the best solution for the above stated problem.

Chapter4 basically discusses about the simulation results and model results, it even describes about the basis behind the various assumptions made at different stages while developing the model, it also mentions about the accuracy feature of the approach followed.

Chapter5 is the last phase of the thesis which concludes the above work describing about the merits, demerits and applications of the above model and the approach, with the scope for future work.

# Chapter 2

# REVIEW OF THE EMPIRICAL MODELS FOR TIMING ANALYSIS

## 2.1 Introduction

The primary aim of the thesis is to present a simplified timing delay model for the CMOS circuits with best possible accuracy, hence it is seen that various concepts and related models were developed where most of them concentrated on arranging capacitive and resistive elements in different fashions according to the theory of analysis to determine the delay of the circuit.

For optimizing high-speed integrated circuits, accurate modeling of signal path delays in the circuit is of special importance. Although device level simulators such as SPICE produce accurate and detailed delay information, analytical delay models are required in general, since computation time for SPICE simulation increase rapidly with the number of transistors in the circuit.

Numerous efforts and results have been reported and contributed to the evolution of this linear RC approach. Rubinstein[11], Penfield[11], and Horowitz[24] derived simple formulas for finding upper and lower bounds of the delay. Wyatt[21] and Yu[21] made extensions to include resistor loops in the network, and also tight-

ened the bounds. Lin[25] and Mead[25] redefined Elmore's[22] delay to properly handle the effect from initial charges in the network. Chu[24] and Horowitz[10] presented a two-pole-one-zero model to improve the accuracy of circuits with charge sharing operations, as a result from these remarkable contributions, timing simulators and analyzers based on the linear RC model have a computational speed close to that of switch-level logic simulators.

However, this method generally suffers from one major drawbacks; namely, the over simplified linear resistance model on the nonlinear MOS transistor cannot guarantee reliable accuracy as compared with the more complicated circuit simulators . Moreover, the above results are derived by assuming a step-input waveform while the propagation signal always exhibits a finite-slope waveform in practice. Attempts to extend the applicability of the linear RC delay model have been reported. Horowitz[24] introduced a simple transformation of variables to convert the nonlinear MOS circuit into a psuedo linear network such that the techniques developed for linear RC networks are still applicable while taking into account the nonlinear MOSFET characteristic.

The nonlinear model, however, becomes quite complicated especially when the input waveform effect is included. In the timing verifier Crystal , Ousterhout[23] used an effective resistance based on the rise-time ratio to include the effect of the finite-slope input waveform. However substantial inaccuracies still exist.

On the other hand, an alternative approach based on the empirical delay models for fixed gate structures has been reported . Reliable accuracy and extremely efficient speed can be achieved as the delay values are directly estimated, with very minor computations, from the library if the delay characteristic of the gate has been pre-characterized. This approach nevertheless suffers from several drawbacks.

- In order to cover a wide range of different parameters such as transistor sizes, node capacitances, and input waveform shapes, numerous delay data respect to various combinations of such parameters need to be generated and the pre-characterization process is quite time consuming.
- It is not guaranteed, and in fact is impossible, to construct empirical models for all possible logic gates.
- The timing delay is a high dimensional and nonlinear function of the forementioned parameters and is difficult to be represented by a simple delay model directly in terms of these parameters. A variable reduction technique has been reported to reduce the number of parameters in the empirical model. The dimension of the parameter space, however, still grows in more complicated subcircuit, such as those containing transmission gates.

While there are many timing verifiers in use today most do not address the problem of parameter uncertainty, a few however provide a partial solutions to this problem. In particular, this timing verifier for digital circuits use bounds on the delay of each circuit macro-component (AND gates, OR gates, FLIP FLOP, ETC) to compute bounds on the performance of the entire circuit, but none of them discusses how these components delays are derived initially.

The most widely used approach for modeling parameter uncertainty within existing simulation systems is the "Monte Carlo" methods or the "Methods of Statistical Trials", with this techniques analysis is repeated for random combinations of values chosen from within acceptable range of each parameters. Unfortunately, accurately determining bounds on the behavior of a circuit requires a large number of trails, thus while Monte Carlo[32] simulation can be effective it is also very

time-consuming, the goal is to achieve similar accuracy in less time.

There are two basic approaches which are usually taken to acquire the transient information and yet maintain a fast computation time. One of these approaches use extremely simplified RC model and treats each MOS transistor as a linear resistor from the drain to the source and a diffusion cap acitance to the ground. Tools such as RSM, CRYSTAL[17], TV, and SCALD systems are widely used and they fit into this category and fall at the far end from SPICE on the speed-accuracy trades-off curve.

On the other hand switch timing approach calibrates certain type of primitive components using a circuit level simulator and stores these primitive delay values in a multi-dimensional space. The higher level circuit elements are first broken down and mapped into the primitive components and than than the delay values are looked up from the tables. Time optimizers such as LSS and TILOS[27] are employed to tune both hand and machined generated designs.

Minimizing the delay in a circuit path is a problem of global optimization which becomes very difficult when path consists of multiple input gates, because the delay also depends on the input pattern. The necessity of global optimization can be explained better with an example, let us assume that we want to minimize the delay of an inverter chain given the value of output load and the size of the first gate, Increasing the width of the device in the second stage decreases the delay of the second gate but, at the same time, this increases the output capacitance seen by the first gate. We decrease the delay in the second stage and we increase the delay in the first stage:is the net result a shorter delay? To find this out global optimization becomes necessary.

## 2.2 Delay analysis using RC method

There are various techniques which are based on the RC-approach, where the basic concept is of using a resistive and a capacitive element. But the entire analysis changes depending on the arrangement of these elements. Also it depends on inclusion and exclusion of some important factors. In the subsequent section various important approaches based on the RC-analysis are discussed.

### 2.2.1 RC-tree approximation method

The RC-tree approximation method presents a new intuitive formulation of the problem, making explicit use of the RC-tree delay modeling. When the optimizer is applied to a signal path traced by the critical path analyzer, each transistor on the path is treated as a fixed resistor driving some output capacitances. In the following analysis it is assumed that resistance per square of each transistor remains constant as the width changes. Load capacitances includes interconnect as well as gate and channel capacitances.

Delay through a path is given by

$$T = \sum_{i=1}^{N} t_i \tag{2.1}$$

where the delay $t_i$ over each transistor is assumed to be the RC delay.

$$t_i = R_i C_i \tag{2.2}$$

where the resistance $R_i$ depends only on the type and width $W_i$ of the transistor, and is fixed otherwise;

$$R_i = \frac{r_i}{W_i} \tag{2.3}$$

where for the sake of simplicity, length of the transistor and some other fixed parameters have been absorbed in $r_i$.

The output capacitance for each transistor is calculated based on the RC-tree approximation. In this approximation, the effective load of each transistor is the sum of all capacitances down stream on the same diffusion path. It is convenient to separate the effective capacitance into two components

$$C_i = C_{0i} + \sum_{j=i}^{N} f_{ij} W j \tag{2.4}$$

where the summation runs over all transistors which are downstream on the signal path, and on the same diffusion path as the first transistor. The term $C_{oi}$ does not depends on the width of the transistors, and remains fixed as they are changed. This term is made up of the wiring capacitances. The second component depends only on the widths of the transistor source/drain.

$$f_{ij} = 2C_{jsw} + C_j(dsextend) \tag{2.5}$$

where $C_{jsw}$ and $C_j$ are the sidewall junction, and junction capacitance respectively, is the extension of source/drain region.

The other terms can also be related to the primitive capacitances; if a transistor is preceded by another with a channel connection, capacitances at the source as well as at the drain of the transistor should be included.

This yields

$$f_{ij} = 2f_{jj} \tag{2.6}$$

for$i \geq j$ which is the loading of the transistor j on transistor i up stream on the path. In the case where the connection to the predecessor is through a gate,

the loading coefficient is given by

$$f_{ij} = L_j C_g \tag{2.7}$$

for $i \geq j$ where $C_g$ is the gate capacitance, and $L_j$ is the length of the transistor

In the above RC- tree approximation method the results show that the deviation from the SPICE results is in the range of 30% to 40%, even the resistor of the device is assumed to be fixed and is assumed to be linear having a scale factor to take care of rise time and fall time delay estimation, which shall further enhance the deviation from actual results. The one major positive point is the simplicity of the model, which shall be usefull for optimization of a circuit and delay calculation.

### 2.2.2 RC analysis in crystal

We begin with a brief review of the PR-Slope delay model used in Crystal[23]. The purpose of the delay modeler in Crystal is to compute the signal delay through a stage or chain of transistors. Each stage represents a path through the circuit originating at a strong signal source (Vdd or Gnd) and terminating at an output node or transistor gate (called the target). A stage is enabled by the last transistor in the path to switch on. This transistor is called the trigger of the stage. Given a stage description consisting of the sizes and types of the transistors in the stage, the parasitic resistances and capacitances of the nodes, the trigger transistor, and the waveform at the gate of the trigger transistor, the delay modeler generates the resulting waveform at the target of the stage.

To estimate delay, the PR-Slope model begins by calculating a resistance and capacitance for each node and transistor along the stage. In Crystal, a transistor is modeled as a perfect switch in series with a resistor. This resistance is fixed

for non-trigger transistors and is determined by a table lookup on the transistor type and signal value. This factor is then multiplied by the length/width ratio of the transistor to generate an estimate of its effective resistance. The effective capacitance of all transistors is similarly computed.

The effective resistance of the trigger transistor is more accurately modeled. This resistance is not a constant, but a function of the input waveform at the gate of the transistor. In particular, the timing analyzer combines the rise time at the transistor gate, the load being driven, and the transistor size into a single ratio (called the rise time ratio). It then consults a table indexed by these rise time ratios to find the resistance factor of the trigger transistor. This factor is multiplied by the aspect ratio of the transistor to determine its resistance. All transistor characterization tables used in these computations are generated by running SPICE simulations on sample circuits and compiling the results.

Having calculated the resistances and capacitances of each node and transistor in the path, Crystal uses these values to compute the total delay of the stage. The PR-Slope model employs the RC equations presented by Penfield and Rubinstein in [11]. Since a Crystal stage is just an RC line, these delay equations simplify to the following sum: where Rs,i is the sum of the resistance along the path from the signal source to element i and Ci is the capacitance at element i.

But this methodoloy though using PR-slope model is still unable to match the results of SPICE and has a deviation of 30% to 35%, and even the non-linear characteristics of the MOSFET is overlooked giving the error on higher side.

### 2.2.3 Transistor level modeling technique

This is an another approach used to compute the delay of a given circuit by RC-approach.

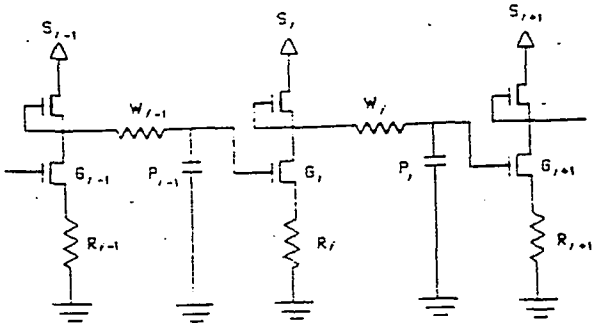


Figure 2.1: Transistor model

This approach uses another method were the optimizer, is used to identify and analyze the set of critical and near-critical paths in a circuit. On any one critical path, a single gate input triggers a change in the gate output. All other gate inputs are assumed to be constant all inputs in series with the trigger input are modeled as a single resistance. Ri as shown in figure(2.1), each gate is modeled as an input capacitor plus a fixed resistor whose value depends on gate topology, device characteristics and whether the output ofthe gate is 0 or 1.

The transistor sizing algorithm EO[18] associates with each gate a scale factor, $S_i$, that determines the transistors sizes within the gate. Transistor sizes scale up or down according to the scale factor, the length of the pullup is inversely proportional to $S_i$ while the width of the pulldown is directly proprtional to Si (pullup width and pulldown length are fixed). Thus changing the scale factor will leave

the impedance ratio of the gate unchanged, but the current supplied or the current sunk by the gate will increase in direct proportions to $S_i$. Increasing $S_i$ decreases the output delay of gate i but increases the capacitive load on gate i-1.

The delay of gate i Figure 2.1 is simply the product of the resistance times the capacitive load.

$$t_i = \frac{R_{ieff}}{S_i + W_i}(S_{i+1}G_{i+1} + P_{i+1}) \tag{2.8}$$

The capacitive load on the output is the sum of the parasitic wire capacitance between gate i and i+1, $P_{i+1}$, and the input capacitance of the gate i+1. Since the width of the pull-down transistors is proportional to the gate scale factor, the input capacitance of gate i+1 is $S_{i+1}G_{i+1}$ where $G_{i+1}$ is the gate capacitance of the original unoptimized circuit. $W_i$ is the parasitic wire resistance, and $R_{ieff}$ is the effective resistance of gate i

$$R_{ieff} = R_{pui} \tag{2.9}$$

if output is 1

$$R_{ieff} = R_{pdi} + R_i \tag{2.10}$$

if output is 0

Where $R_{pui}$ and $R_{pdi}$ are the effective resistance of a single pullup and pull-down transistor respectively.

The total path delay is simply the sum of the individual gate delays.

$$T = \sum_{i=0}^{N} t_i \tag{2.11}$$

The intial results were far away from the actual results, the simplified circuit model allow the circuit delays to be computed very rapidly. Initial estimates indicate the accuracy to often be within 30% of the delays calculated with SPICE simulations. The greatly simplified transistor models allow the vector of optimum transistor sizes to be formulated as a relatively simple set of tridiagonal, nonlinear equations. These can be analytically solved with high computational efficiency. Simulators such as SPICE require iterative computation of delays. This requires two to three orders of magnitude more computation time making the optimization problem prohibitively costly.

A theoretical overview of the linear RC circuit model wass presented in the previous section, where two delay models of different complexities were derived, namely, the simpler STC (single time constant) model and the more accurate TTC (two-time-constant) model. The STC model usually provides a reasonable estimation but, in quite a few cases, may greatly deviate from the real delay values. The TTC model gives much better estimation but consumes CPU time. An accuracy measure on the STC model is derived in section which decides whether using the more accurate TTC model.

The accuracy performance of the STC model has been discussed. Where the STC prediction closely matches the real waveform in one example, but has a large deviation in another example. The TTC model was proposed in and to handle this accuracy problem. since the more complicated TTC model inevitably takes more computations, an interesting problem thus arises, namely, under what circumstances, the STC model is to suffer from the poor accuracy and the TTC model should be applied.

In addition to the error caused by the nonlinear MOSFET characteristic , the linear RC delay also suffers from some inaccuracies due to the STC approximation

the multiple-time constant network function of the linear RC network.

Despite larger errors in some cases, the STC model still provides decent predictions in most cases.

## 2.3 Macromodeling technique

Delay models can be defined on different levels. There are transistor level models using RC-tree formulas, and there are macromodels, where different types of subcells are considered to be the building blocks of the circuits instead of individual devices. The general idea of macromodeling is to characterize the delay contribution of each type of subcell in the circuit with a single or few design parameters in order to obtain a low dimensional optimization problem, and hence, to reduce the computational effort. In the simplest case a scale factor is introduced for each gate in the circuit.

### 2.3.1 Signal delay modeling

This is an different approach for calculating the delay of a circuit, it uses MOGLO, which stands for multiobjective gate-level optimization, which uses posynomial gate level macro-model for signal delay in CMOS logic gates combined with efficient multiobjective optimization techniques.

According to [29], there are two contributions to the signal delay T of a long-channel inverter triggered by an input voltage ramp, the step response delay, $t_d^s$ and an input dependent delay, $t_d^{in}$.

$$T = t_d^s + t_d^{in} \tag{2.12}$$

$t_d^s$ is given for rising (falling) input signals by

$$t_d^s = \frac{C_L}{W_{n(p)}} \tag{2.13}$$

$t_d^{in}$ is given by

$$t_d^{in} = \frac{1}{16} t_{sub}^{r(f)} (1 + \frac{2V_{tn}}{Vdd}) \tag{2.14}$$

where $t_{subr(f)}$ denotes the input signal rise(fall) time The proportionality constant in above equation depends on the supply voltage $V_{dd}$, the threshold voltage $V_T$, and other technology dependent parameters. $W_{n(p)}$ denotes the width of the n- or p-device, respectively. The channel length L of the MOS transistor is chosen to be minimal in the following. $C_L$ is the output load capacitance of the inverter.

To replace Wn and Wp by an integral scaling variable we note that in typical signal paths the probability of rising and falling input signals is equal. Hence, it is advantageous to design the inverter "symmetrical", i.e.. for a fixed but technology dependent ratio $\frac{Wn}{Wp}$ , $t_d^s$ can then be considered to be proportional to $\frac{CL}{(Wn+Wp)} = \frac{C_L}{W}$. Note that the switching threshold of a symmetrical inverter is near the mid-level voltage, which guarantees for high noise immunity.

To include short-channel effects and to correct for certain approximations in the derivation of above equation considered is the proportionality constant in $t_d^s$ as a free parameter $t_d^s = \frac{1}{G}\frac{CL}{W}$, where G can be regarded as a specific transconductance. Parasitic output capacitance increasing the total load CL are incorporated by introducing a second free parameter $G_{s/d}$ for the specific source/drain capacitance. In order to improve the accuracy of the fits. The method replaces the proportionality factor (1/6) in the long-channel solution fror $t_{in}^d$ by third free parameter T. T is found in the interval $1/6 \leq T \leq 1/5$ depending on technology. $V_T$ might also be considered as a fitting constant for $t_d^{in}$ . However, excellent fitting to SPICE delay times were obtained with the threshold voltages from the SPICE parameter sets.

$$\mathrm{T} = (C_L + W * C_{s/d}/(G * *W) + T * T_{subr(f)} * (1 + 2V_T/V_{dd})$$

The fitting reproduce the simulation data accurately with the exception of

very slow input ramps. In particular , the model has a wider applicability than was expected from long-channel analysis . Originally the above equation were derived for "fast" input ramps reaching their final value before the conducting device leaves the saturation regime. Hedenstierna and Jeppson give a criterion : $t_{subr}C_L$ ...$6V_T$ /$\beta n(p)$Vdd(1-VT)3.$\beta n(p)$ is the n(p)-transistor gain factor. In the present case, it is convenient to replace $\beta$ and to recast the inequality in terms of $t_d^s$.

$t_{sub}^{r(f)} \leq 1.1v \quad t_d^{in}$ , (VT = 0.8V);

Equation corresponds to the dotted line in fig.1 which separates fast (right) and slow(left) input ramps. Linear behavior persists far beyond this boundary until input ramps are extremely slow. This extended length of validity of the model for a 1-uM technology results from the extended saturation region of short -channel devices due to carrier velocity saturation. In regions where model is not valid, it is still a strict upper bound for gate delay. Hence, if we use that model for circuit optimization, transistors in gates triggered by extremely slow input signals will be sized somewhat larger than necessary and timing requirement will not be violated.

## 2.4 Mapping technique for Timing models

This is new technique used for delay calculation for both simple and complex static logic gates. Unlike the previous delay models which assume the worst case scenario, this delay model handles the different input switching conditions. In the delay analysis of a circuit, failing to take into account the position of the transistor that is switching can result in a delay value which is by a margin of 100% or more from actual delay value. This new modeling technique has been implemented in LISP on a TI explorer II Lisp Machine as a part of DROID design environment.

The circuit elements at higher level are first broken down and mapped into

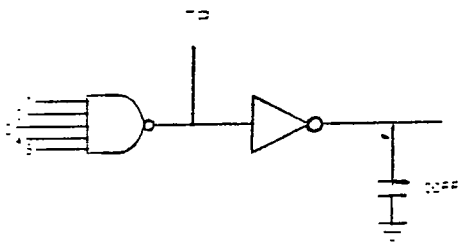

Figure 2.2: NAND5 test circuit configuration[6]

primitive components such as inverter and then the delay values for these components are looked up from the tables. Despite the routine use, little mapping issue have been addressed before: the worst case scenario has normally been assumed where the delay value can be off by 100% or more, from the actual. As can be seen in Figure 2.2 NAND5 gate cascaded to an inverter with a 100Ff capacitive load has been simulated with SPICE Figure 2.2 shows two delay waveforms at a TP; solid curve represents the case when the first input of the NAND gate is switching and rest are tied to high and the dashed curve represents the case where the bottom-most transistor is switching. It can be observed that solid line and the dashed line temporally differ by more than 100%. Obviously, the worst case analysis is inadequate for todays high performance IC's. A new mapping technique which can handle different input switching situations for static gates is presented in this paper.

### 2.4.1 Mapping Technique

Figure 2.3 shows a NAND circuit, with N input signals arranged in such an order that the smallest number is closest to the output node. Only one transistor K is assumed to be switching at any particular time. This is an assumption, as in the critical path identification, only one signal per gate will be activated. Following

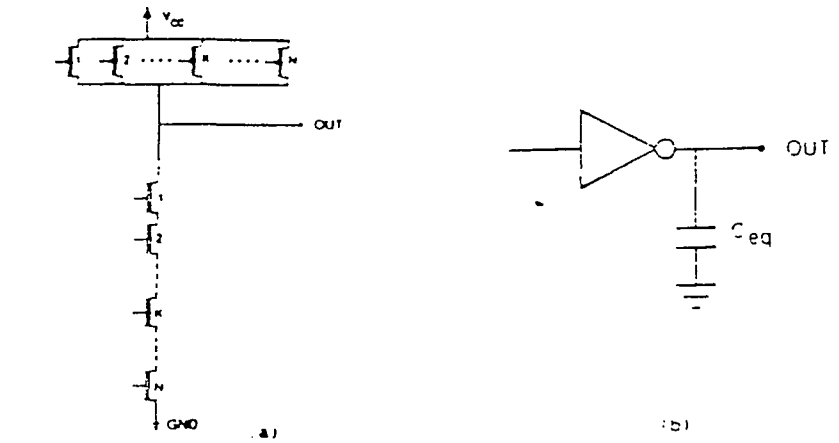


Figure 2.3: A NAND circuit with N input

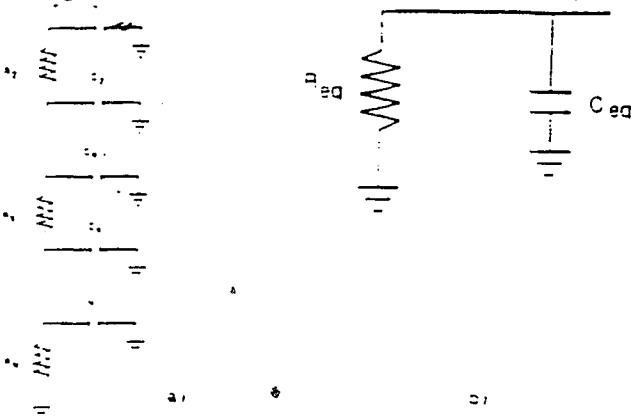


Figure 2.4: RC model for N input NAND

our mapping technique. this circuit will be mapped to an equivalent inverter of the Figure 2.3 such that both circuits have equal first-order time constants Figure 2.4 show the RC models for the n-portion of the NAND and the inverter circuits respectively. The first-order moment of the impulse response or the Elmore time constant of the Figure 2.4 is

$$T_C = (R_1 + R_2 + R_3 + .... + R_N)C_0 + (R_2 + R_3 + .... + R_N)C_1 \tag{2.15}$$

$$T_C = \sum_{j=1}^{N} \sum_{i=1}^{N} R_j C_i \tag{2.16}$$

where $R_j$ and $C_i$ are the equivalent resistance and the equivalent capacitance

respectively for the transistor Ti. The mapping technique is thus to find an inverter circuit with the correct width which will represent an equivalent resistance of value Req and also to find the correct capacitive load to the inverter output node.

### 2.4.2 Width Consideration

Usually, the effect due to the backgate bias may raise concern for a large number of transistor connected in series.

For the NAND type circuits, all the N-channel devices will be in the conducting state, except for the device K, which will switch either from low to high or high to low. In other words, the device K will change its state either from cutt-off to fully-turned-on or vice-versa. In either case, its average current driving capability is only half of the other devices, i.e, its effective transistor size is only half of the others. Based on the perception, the equivalent transistor sizes are determined as per the following equations

$$W_{peq} = W_{pk}$$

$$\frac{1}{W_{neq}} = \frac{1}{W_{nk}} + \sum_{i=1}^{M} \frac{1}{2W_{ni}}$$

where

M= N —- if Tk switching high M= (k-1)—- if Tk switching low

Only the transistor up to the one switching are considered if the input signal is switching low, because the path is blocked beyond this device.

### 2.4.3 Capacitance Mapping

Because the first-order time constants are to be preserved and the sizes of the transistors other than the one switching are made twice as big or the equivalent

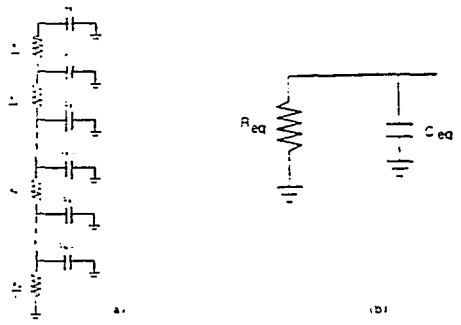


Figure 2.5: Modified RC model for n-input NAND

resistances are reduced by half. the RC models of the circuits in Figure 2.4 are transformed to those in Figure 2.5 and equation can be recast as

$$R_{eq}C_{eq}) = (\frac{R_1}{2} + \frac{R_2}{2} + \frac{R_3}{2} + \frac{R_4}{2})C_0 + (\frac{R_2}{2} + \frac{R_3}{2} + .... + \frac{R_N}{2})C_1....$$

Since the transistor width is inversely proportional to its resistance can be rewritten as

$$\frac{C_{eq}}{W_{eq}} = (\frac{1}{2W_1} + \frac{1}{2W_2} + .... - \frac{1}{2W_n})C_0 + (\frac{1}{2W_2} + .... + \frac{1}{2W_2} + .... + \frac{1}{W_n})C_1 + ....$$

The capacitance consists of diffusion capacitance and gate capacitance respectively, for the above NAND gate the extracted equivalent mapping capacitance, Ceq, is the sum of Cneq (the equivalent capacitance for the serial n-channel transist or) and Cpeq (the equivalent capacitance for the parallel p-channel transistor).

Optimizing scale factor in the gate level algorithms might induce a certain suboptimality in the resulting set of transistor sizes, since transistors cannot be sized individually according to their position in the pull-up or pull-down branch of logic gate. In contrast, transistor level optimization algorithms allow for position dependent sizing, which has been quoted to be important for high performance circuits. However, most transistor level optimization algorithms use RC-tree delay models, which deviate from SPICE simulation by 10 to 20 percent. These inaccuracies might yield suboptimal sets of transistor sizes as well. Inaccuracies in RC- delay result from neglecting non-linearities of the MOS-transistors and from difficulties in including input waveform effects.

Since last response times can be expected for gate level algorithms, we decided to use gate level models for the optimizer MOGLO[33]. Macromodels for MOS logic gates were presented by Matson[33]. Although these models are easy to compute and quite accurate, they exhibit discontinuities in first derivatives. This complicates the numerical part of transistor size optimization. Hence, we derived a precise gate level delay model with well behaved analytical properties. This model is based on the analytical solutions recently published by Hedenstierna[29] and Jeppon[29] for the delay of long channel CMOS inverters driven by input voltage ramps. Since SPICE simulation indicates that the same functional dependence of gate delay on device geometries and input signal slope is found for NAND- and NOR- gates as well, we used the results of to derive a gate level delay model for general static CMOS logic gates. Short-channel effects and different driving capabilities of the various gate types are incorporated by introducing technology dependent fitting parameters for each type of logic gate. These model parameters are determined from SPICE simulations.

# Chapter 3

# A TIMING MODEL BASED ON CHARGE CONSERVATION

## 3.1 Introduction

The main objective of this work is to improve the accuracy of delay estimation in CMOS circuits using the charge conservation principle. As seen in the previous chapter that the models based on linear RC approach are simple, consuming less computation time, but has large deviation from the actual result. Hence we follow an entirely different approach to solve the above problem. We use the principle of charge conservation. Taking a specific case of an inverter and a specific case of fall time delay estimation it can be explained as follows, it is the time taken by the charge stored in the capacitor to discharge to ground potential. In case of the rise time delay estimation it is the time taken by the capacitor to charge to the supply potential. So basically the entire delay of the circuit is a function of the charge present in the load capacitor. Taking a specific case of fall time delay estimation, the discharging of the stored capacitor is goverened by two different current equations, the saturation current and the linear current in two different intervals. Since the current is a non-linear function of time, we have basically taken

care of the non-linear MOSFET characteristics.

Model describes the device behavior which resembles the circuit simulation program. This is done by expressing the current and the charge associated with device terminals interms of nodel equations.

The basic reason for using this approach is becuase of the following merits.

- It avoids time consuming numerical integrations or differential equation in the circuit or timing simulation.
- It realistically captures the switch nature of the CMOS inverter and properly models the novel MOS circuit structure such as the precharged logic, pass transistor buses, static and dynamic storage cells [24].

## 3.2 Delay Analysis of an Inverter

This chapter discusses the basic concept about the functioning and delay analysis in an CMOS inverter circuit, similarly an analysis can be carried out for the other standard gates.

A complementary CMOS inverter is realized by the series connection of a p- and n- device shown in the Figure 3.1 [30].In order to derive the D.C transfer characteristic of the inverter (Output voltage $V_o$ as a function of the input voltage $V_{in}$), we start with Figure 3.2 which outlines various regions of operations for the n- and p- transistors. In this table $V_{tn}$, is the threshold voltage of the n-channel device and $V_{tp}$ is the threshold voltage of p-channel device. The objective is to find the variation in output voltage ($V_o$) for changes in the input voltage ($V_{in}$).

The operation of the CMOS inverter can be divided into five regions shown in the Figure 3.2 .

**Region.A :**

This region is defined by the variation of the input voltage in the range $0.0 \leq Vin \leq Vtn$ in which the n-device is in cuttoff ($I_{dsn}$=0) and the p-device is in linear region.

**Region.B :**

This region is characterized by the change in the input voltage from $Vtn \leq 0.5Vdd$ in which p-device is in linear region while the n-device is in saturation.The equivalent circuit of the inverter in this region can be represented by a resistor for the p-transistor as shown in the figure.

**Region.C :**

In this region both n- and p-device are in saturation region and hence during this period the maximum current is flowing in the circuit. The significant factor to be noted is that in region C we have two current sources in series, which is unstable condition. Thus a small input voltage has a large effect at the output which is responsible for making the transition very steep, and the region C happens to be an important region.

**Region.D :**

This region is described by the variation of the input voltage in the range $0.5Vdd \leq Vin \leq Vdd - Vtn$ in this region the p-device is in saturation and the n-device is in linear region. This condition is represented by the equivalent circuit diagram shown.

**Region.E :**

This region is defined by the input conditions $Vin \leq Vdd - Vtp$ in which

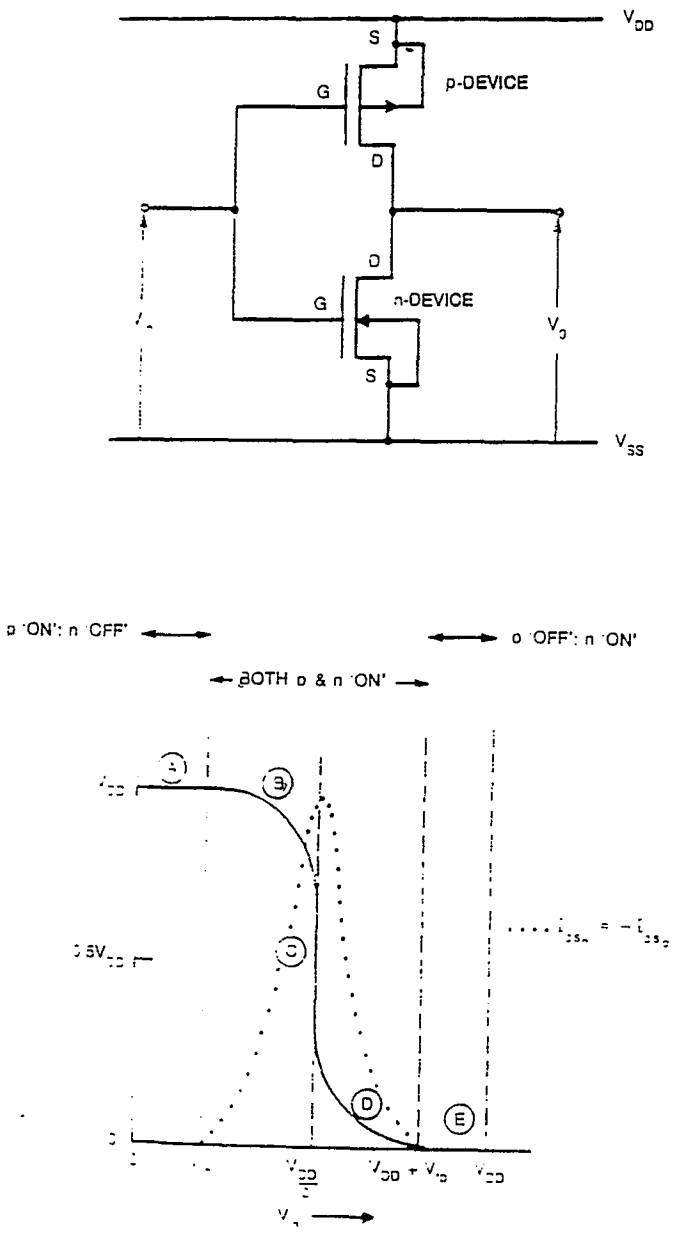


Figure 3.1: Inverter circuit with its D.C Transfer characteristics [30]

| | CUTOFF | LINEAR | SATURATION |
|---|---|---|---|
| p-device | $V_{gs_p} > V_{t_p}$ ; <br> $V_{in} > V_{t_p} - V_{DD}$ | $V_{gs_p} < V_{t_p}$ ; <br> $V_{in} < V_{t_p} - V_{DD}$ | $V_{gs_p} < V_{t_p}$ ; <br> $V_{in} < V_{t_p} - V_{DD}$ |
| | | $V_{gd_p} < V_{t_p}$ ; <br> $V_{in} - V_{out} < V_{t_p}$ | $V_{gd_p} > V_{t_p}$ ; <br> $V_{in} - V_{out} > V_{t_p}$ |
| n-device | $V_{gs_n} < V_{t_n}$ ; <br> $V_{in} < V_{t_n}$ | $V_{gs_n} > V_{t_n}$ ; <br> $V_{in} > V_{t_n}$ | $V_{gs_n} > V_{t_n}$ ; <br> $V_{in} > V_{t_n}$ |
| | | $V_{gd_n} > V_{t_n}$ ; <br> $V_{in} - V_{out} > V_{t_n}$ | $V_{gd_n} < V_{t_n}$ ; <br> $V_{in} - V_{out} < V_{t_n}$ |

Figure 3.2: Operational details of the CMOS inverter [30]

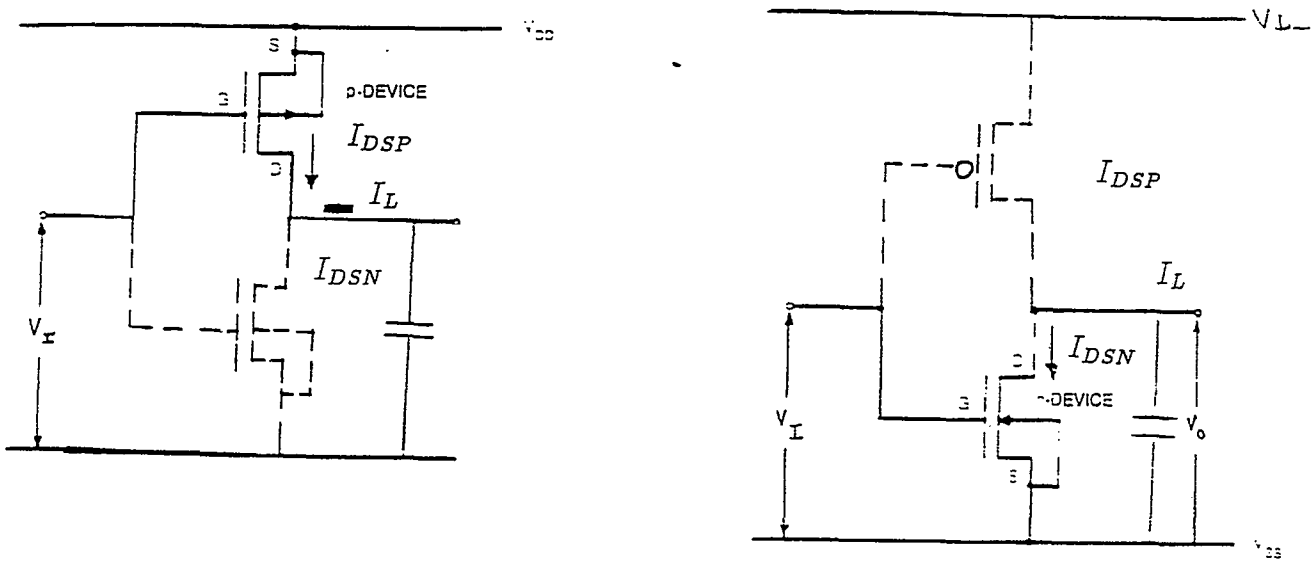


Figure 3.3: Capacitance charging through p-device and discharging through n-type of device [1]

the p-device is cutoff (Idsp=0) and the n-device is in linear mode operation.

The above gives the basic idea of the circuit behavior under various cases of the input voltage and even it shows the behavior of the current flow in the circuit from where we roughly get the idea of the delay in the circuit.

The switching speed of a CMOS gate is limited by the time taken to charge and discharge the load capacitance $C_l$ as shown in Figure 3.3 . An input transition results in an output transition that either charges $C_l$ towards $V_{dd}$ or discharges $C_l$ towards $V_{ss}$. The main idea here is to develop simple timing model that describes the switching characteristics of a CMOS inverter and similarly it can be modified to fit for various CMOS gates.

### 3.2.1 Basic Definition

Before proceeding further, we need to define some terms referring to the Figure 3.4

**Risetime** :Tr:

It is the time for a waveform to rise from 10 percent to 90 percent of its steady state value.

**Falltime** : Tf:

It is the time for a waveform to fall from 90 percent to 10 percent of its steady state value.

**Delaytime** : Td:

It is the time taken by the capacitor to discharge to make the output voltage to goto $0.1_{Vdd}$, or as seen in the Figure 3.4 it is the area under the curve and mathematically it is given as T3-T1. Where T3 is the instant of time when the output voltage comes to $0.1V_{dd}$. T1 is the instant of time when the output voltage is $0.9V_{dd}$ or is the instant of time when the n-device starts conducting.

## 3.3 Detailed Description of the Developed Model

This chapter basically gives an inside picture of the work done on the timing analysis of the CMOS gate. Considering a specific case of a CMOS inverter we proceed as follows. We know that the basic function of the inverter is to give an inverted output for the given input voltage. This means if an step input is applied at the input the output received is an inverted step. The output is avialable after some an delay which occurs due to charging and discharging phenomena occuring due to the presence of the load capacitance and device resistance. A typical load capacitance consists of the input gate capacitance of the following transistor and the sidewall

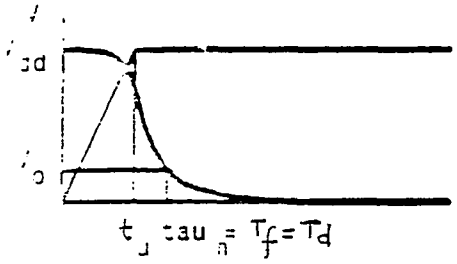

Figure 3.4: Fall time, rise time and delay of the CMOS inverter[1]

junction capacitance.

This section aims to present an accurate model for the fall time and the rise time of an CMOS circuit (inverter) when driving an capacitive load. In order to compute the output voltage and hence the delay, itis necessary to know the load current ($I_l$). From the kirchoff's current law we have the relationship.

$$i_L(t) = -i_{dsn}(t) - i_{dsp}(t). \tag{3.1}$$

Where

$i_{ds(n)}$ = the drain to source current of the n-channel device

$i_{ds(p)}$ = the drain to source current of p-channel device

Unfortunately such approach becomes cumbersome given the complexity of

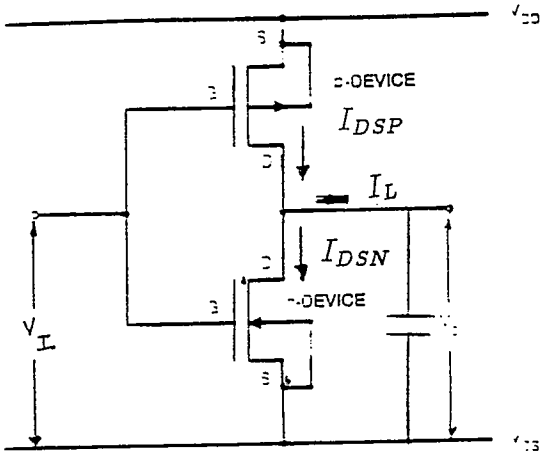


Figure 3.5: Current paths in an inverter[30]

the equations that model the two drain to source current and even simplified equations lead to integrals that are hard to solve analytically. However an important simplification is possible if we look at the dynamic behaviour of a CMOS inverter as shown in the Figure 3.6 and Figure 3.7. The output curves refer to the different load capacitances and it shows that the current flowing through the n-channel device $I_{ds(n)}$ and $I_l(t)$ when the load capacitance is moderately high are almost identical in absolute value that $I_l(t) = I_{ds(n/p)}$.

Here we choose $I_{dsn}(t)$ when calculating fall time and $I_{dsp}(t)$ when calculating rise time. The output response of a CMOS inverter depends on many parameters, most of them are fabrication process parameters such as thin oxide thickness, substrate doping concentration, etc or physical constant such as Sio2 dielectric constant while others can be considered constants, at least in first order approximation, e.g(majority carrier mobility, thin oxide capacitance per unit area, etc).

## 3.4 Fall Time Delay Estimation

Note that the output response of a CMOS inverter depends on the dynamic characteristics of the input waveform, since we know the two classical equations for an CMOS inverter as,

$$i_{ds(sat)} = \frac{\beta_{n(p)}}{2}(V_{in} - V_{tn(p)})^2 \tag{3.2}$$

(saturation region equation).

$$i_{ds(linear)} = \beta_{n(p)}((V_{in} - V_{tn(p)})V_o - \frac{V_o^2}{2}) \tag{3.3}$$

(Linear region equation).

Where

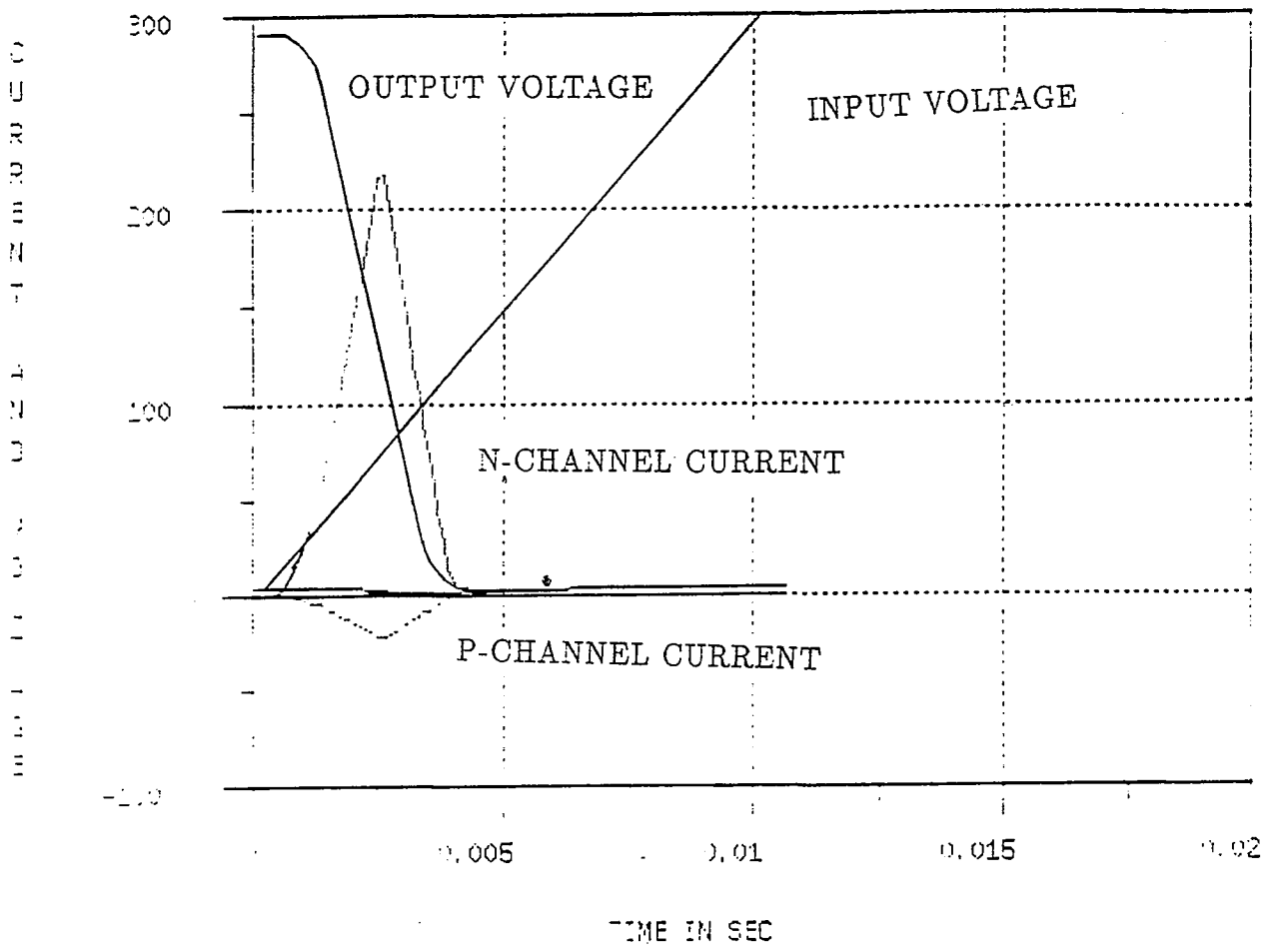


Figure 3.6: Input and output voltage with the current in two devices.

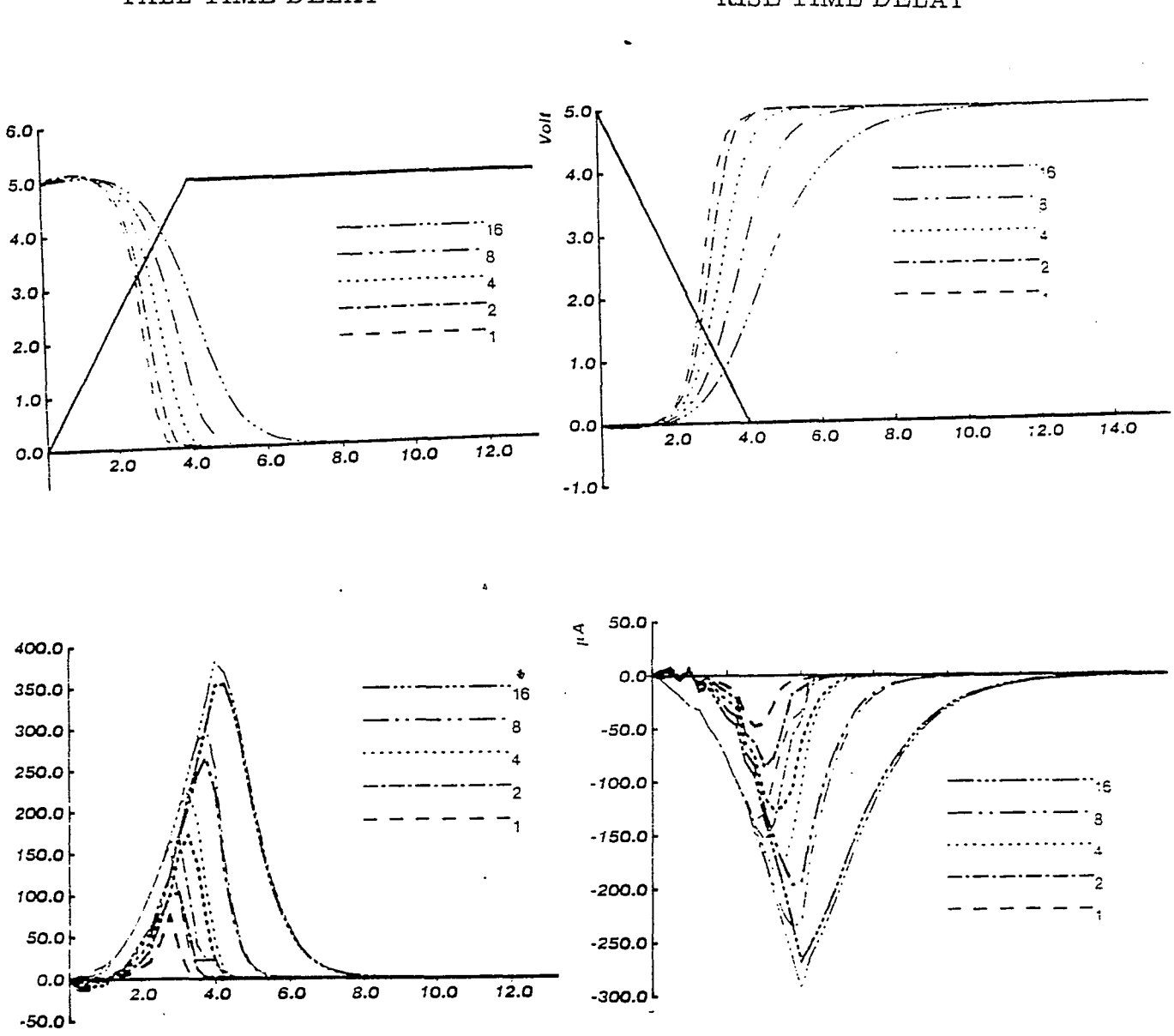


Figure 3.7: Load current during rise time and fall time delay estimation[1]

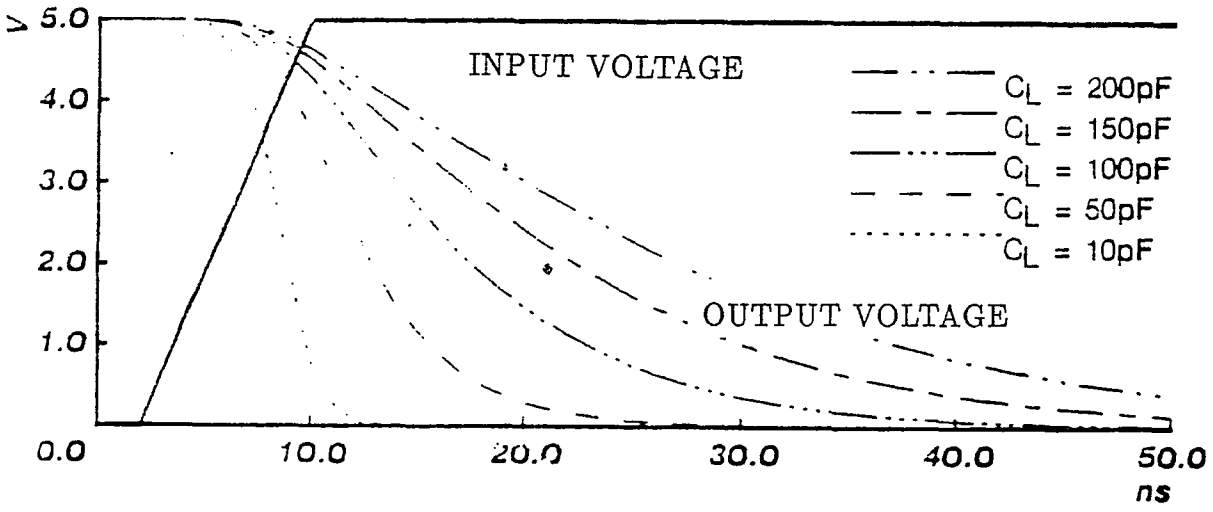


Figure 3.8:

Output voltage for various values of load capacitance.[1]

$\beta_n$ = transistor gain factor of n-device

$\beta_p$ = transistor gain factor of p-device

$V_{in}$ = input voltage to the inverter

$V_o$ = output voltage of the inverter

$V_{tn}$ = threshold voltage of the n-device

$V_{tp}$ = threshold voltage of the p-device

With the above two well known equations for the saturation region of the device and the linear region of the device we proceed as follows. The fall time (rise time) delay $T_f(T_r)$ can be computed by solving the equations appearing in the subsequent sections.

### 3.4.1 Theory Behind the Analysis

The transient solution is determined computaionally by dividing the time interval (0,T) in to discrete time points (0,t1,t2,t3——T), at each point numerical integration is employed to transform the differential model equations of energy storage elements in to equivalent algebraic equations. So we proceed further on the basis of the charge storage.

Charge storage in MOSFET consists of capacitances associated with parasitic and intrinsic device. The parasitic capacitance consists of the overlap capacitances of the gate with respect to other three terminals and the capacitance of the junction diodes, bottom and sidewall(periphery), of bulk source and bulk drain junctions.

For the MOS transistor, gate, bulk, source and drain charges Qg, Qb, Qs , Qd as function of time is difficult, requiring solution of nonlinear partial differential device equations. A solution which is valid at relatively low circuit speeds, i.e. speeds lower than the carrier transit time through the device may be obtained by invoking the quasi-static approximation. The transistor charges are calculated as a

function of terminal voltages under steady state conditions. It is then assumed that the resulting relationship holds even during transients. Thus the charging current are ignored and the MOS transistor is treated as a simple multiterminal capacitance.

$$Qa = \int idt = -C \int dV_o \tag{3.4}$$

To compute the fall-time delay $T_{(f)}$, the entire falling transition is divided into two regions, in the region1 from period T1 to T2 the n-channel device is in saturation wheras in region2 that is from T2 to T3 the n-channel device is in linear region and the total charge stored in the capacitor is equal to the area under the curve as shown in Figure 3.9 . The further calculation is done by following the analytical technique to be discussed in subsequent sections.

### 3.4.2 Region 1: n-channel Device in Saturation

In our case we have separated the entire timing analysis in to two parts. Referring to the Figure 3.9 the first region is from point T1 to the point T2, and from the basic inverter functioning we know that during this region the current flowing in the circuit is the saturation current since $(Vgs - Vtn) \leq (Vds)$. As we move towards the point T2 we observe that the current flowing is the circuit is maximum, because the n-device is in saturation and is on the verge of entering the linear region, wheras the p-device was is linear region and starts entering into the saturation region.

According to the charge conservation principle, the charge stored in the capacitor is given as follows

$$Qa = \int i_L dt = -\int C dV_o \tag{3.5}$$

hence,

$$C \int dV_o = -\int i_L dt \tag{3.6}$$

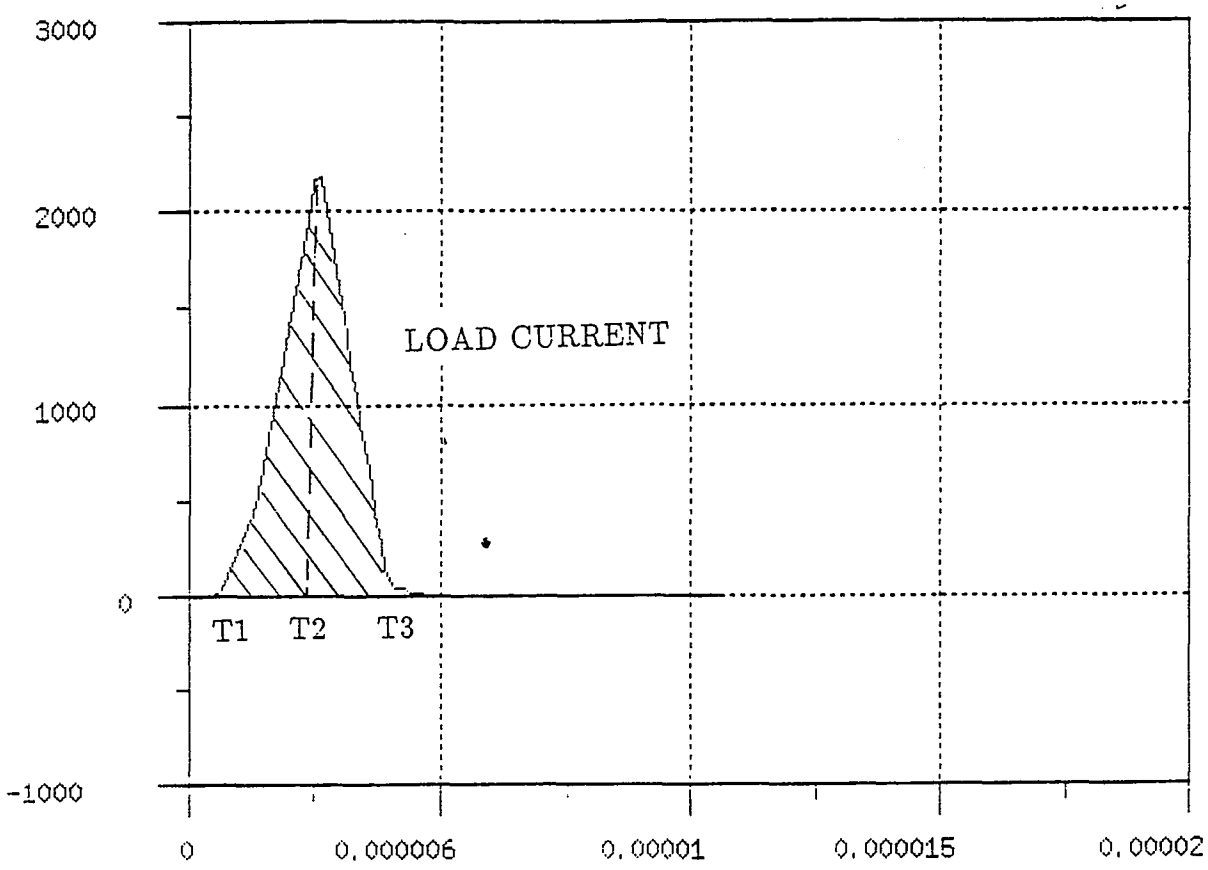


Figure 3.9: Different regions of timing analysis

Where,

$Q_a$ = total charge stored in the capacitor during the interval T1 to T2

C = the load capacitance

$i_L$ = the load current

The current flowing is the saturation current and it flows from the point of time T1 to the time T2. During this interval of time the output voltage changes from the voltage $V_{dd}$ to the voltage $V_x$. The voltage $V_x$ is termed here as the crossover voltage, the voltage at which the rising input voltage meets the falling output voltage as shown in Figure 3.10. After carefully analyzing the simualtion results for various range of capacitive load it is observed that the drain current in the n-device is maximum when the rising input voltage crosses or meets the falling output voltage. This was considered an important point while developing the model because after this point the state of the n-channel device changes, and it leaves saturation region and enters into linear region Hence the Equation 3.5 turns as,

$$C \int_{Vdd}^{Vx} dV_o = - \int_{T1}^{T2} i_L dt \tag{3.7}$$

Where

T1 = the instant of time at which the n-device starts conducting

T2 = it is the instant of time at which the current in the circuit is maximum

Since we know from the very basic current equation of the CMOS inverter that the saturation current is given by the following equation,

$$i_{dsn}(sat) = \frac{\beta_n (V_{gs} - V_{tn})^2}{2} \tag{3.8}$$

Where

$V_{gs}$ = Gate to source voltage applied to the transistor

$i_{dsn(sat)}$ = the saturation current of the n-device

After substituting the standard equation for saturation current depicted in Equation 3.8 in the Equation 3.7 we get the following,

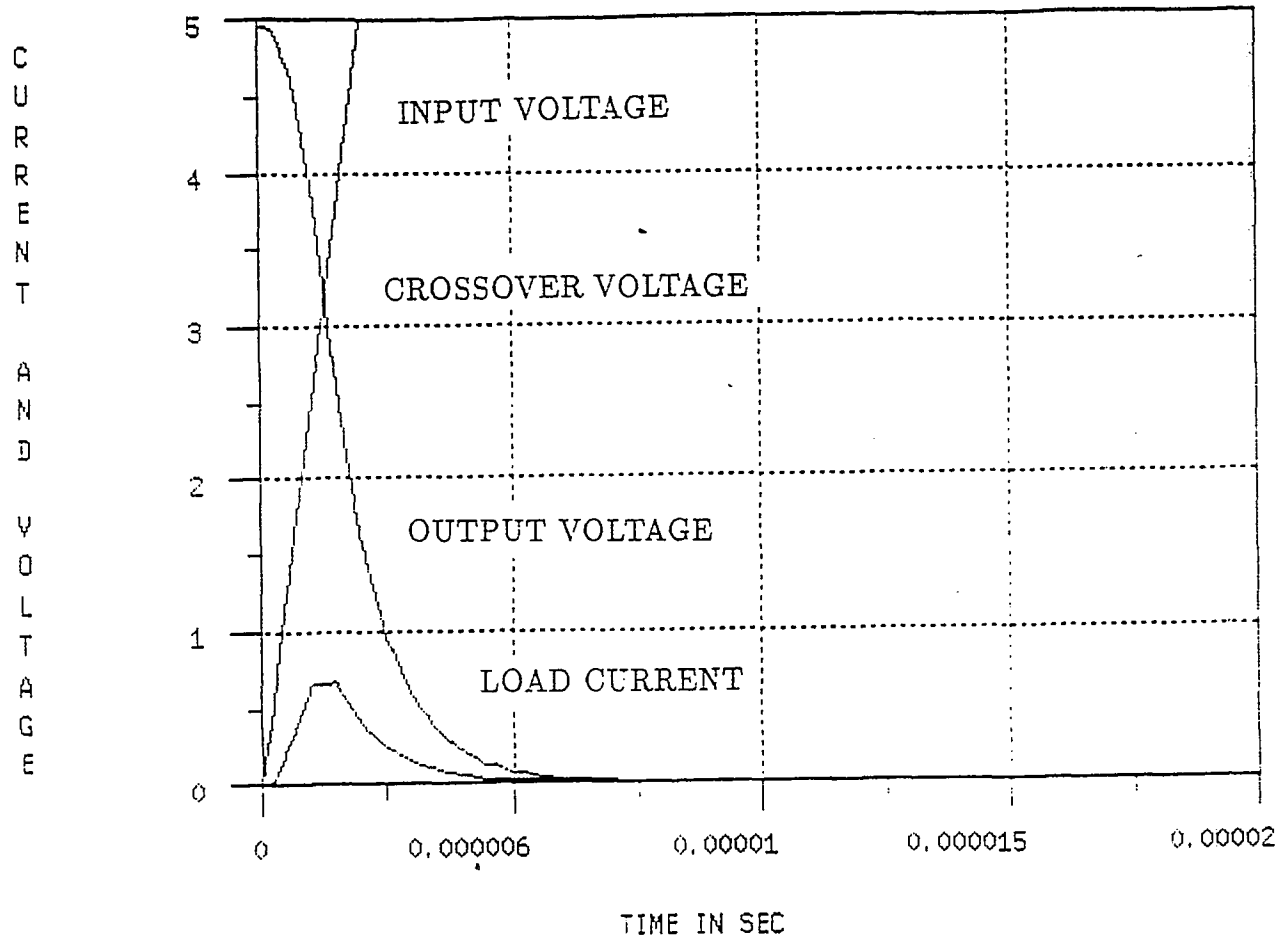


Figure 3.10: Input, output and cross-over voltage with load current

$i_{dsn(sat)}$ = the saturation current of the n-device

After substituting the standard equation for saturation current depicted in Equation 3.8 in the Equation 3.7 we get the following,

$$C \int_{V_{dd}}^{V_x} dV_o = - \int_{T1}^{T2} \frac{\beta_n (V_{gs} - V_{tn})^2}{2} dt \tag{3.9}$$

Simplifying the above Equation we get

$$C \int_{Vdd}^{Vx} dV_o = - \int_{T1}^{T2} \frac{\beta_n ({V_{gs}}^2 - 2V_{gs}V_t + {V_t}^2)}{2} dt \tag{3.10}$$

Carrying integration on left hand side of the above equation

$$C(V_{dd} - V_x) = \int_{T1}^{T2} \frac{\beta_n ({V_{gs}}^2 - 2V_{gs}V_{tn} + {V_{tn}}^2)}{2} dt \tag{3.11}$$

Since the input voltage is rising as the time increases we have an equation

$$V_{gs} = \frac{V_{dd}t}{t_{rise}} \tag{3.12}$$

Substituting the Equation 3.12 in Equation 3.11 we get

$$C[V_{dd} - V_x] = \frac{\beta_n}{2} \int_{T1}^{T2} (\frac{{V_{dd}}^2}{{t_{rise}}^2} t^2 - 2V_{tn}\frac{V_{dd}}{t_{rise}}t + {V_{tn}}^2)dt \tag{3.13}$$

For ease of mathematical representation we use a constant $S_L$ where

$$S_L = \frac{V_{dd}}{t_{rise}} \tag{3.14}$$

using Equation 3.14 in Equation 3.13

$$C[V_{dd} - V_x] = \frac{\beta_n}{2} \int_{T1}^{T2} [{S_L}^2 t^2 - 2V_{tn}S_L t + {V_{tn}}^2]dt \tag{3.15}$$

after integrating the right hand side we have

$$C[V_{dd} - V_x] = \frac{\beta_n}{2} [\frac{S_L^2 t^3}{3} - 2V_{tn}S_L\frac{t^2}{2} + V_{tn}t]_{T1}^{T2} \tag{3.16}$$

Proceeding on the assumption in the Equation 3.12 we now that at t=T1 $V_{gs} = V_{tn}$ for moderate value of rise-time. This is instant of time when the n-device just start conducting. After substituting the conditions mentioned above in equation(3.12) we get

$$V_{in} = \frac{V_{dd}t}{t_{rise}} \tag{3.17}$$

and as we know that the transistor shall start conducting at t=T1 when,

$$V_{in} = V_{tn} = \frac{V_{dd}T_1}{t_{rise}} \tag{3.18}$$

and hence the above equation becomes

$$V_{tn} = \frac{V_{dd}T_1}{t_{rise}} \tag{3.19}$$

solving the above algebraic equation, gives the required T1 in the standard form as follows

$$T_1 = \frac{V_{tn}}{S_L} \tag{3.20}$$

It is seen that for higher values of the input risetime the MOSFET starts conducting in the subthreshold region and hence the subthreshold current dominates during the input voltage change from $V_{off}$ to $V_{tn}$.

And hence we see that for moderate values of capacitive load with higher rise time the subthreshold condition comes into picture, where the above equation of $V_{in} = V_{tn}$ at t=T1 does not holds good, but instead of that the current starts flowing for a voltage less than $V_{tn}$ and that current is called the subthreshold current hence the assumption of the transistor conducting at t=T1 slightly changes for higher rise time and moderate capacitive load.

Substituting the Equation 3.20 in Equation 3.16 and after further simplifications we come to the conclusion that all the parameters of the above equations are known except T2 .

$$C[V_{dd} - V_x] = \frac{\beta_n}{2}[\frac{{S_L}^2{T_2}^3}{3} - V_{tn}S_L{T_2}^2 + V_tT_2 - K] \tag{3.21}$$

Here the parameter K is constant representing the given equation,

$$K = \frac{\beta_n}{2}[\frac{{S_L}^2{T_1}^3}{3} - V_{tn}S_L{T_1}^2 + V_{tn}T_1] \tag{3.22}$$

simplifying the above equation we get

$$C[V_{dd} - V_x] + K = \frac{\beta_n}{2}[\frac{{S_L}^2{T_2}^3}{3} - V_{tn}S_L{T_2}^2 + V_{tn}T_2] \tag{3.23}$$

simplification results in,

$$\frac{{S_L}^2{T_2}^3}{3} - V_{tn}S_L{T_2}^2 + V_{tn}T_2 = \frac{C[V_{dd} - V_x] + K}{\frac{\beta_n}{2}} \tag{3.24}$$

From the above we see that there are two ways to handle the Equation 3.24. In the first approach the above Equation 3.24 can be solved by the newton raphson method. The other approach is the approximation method which gives very accurate solution as compared to the newton raphson method and here for all the calculation we use the approximation method. The program was developed to solve the above equation which is attached in the Appendix.

The approximation method is an approach used for further simplification of the above equations, and to carry out computations more easily without loosing the accuracy feature. In this method , after a large number of simulation runs it is seen that in the above Equation 3.24 the first and the third parameters on the left hand side were having negligible effect, since the model and the simulation results show that these parameters hardly affect the required performance. After comparing the newton-raphson method with the approximation method, it is seen that almost similar results are obtained on substituting an empirical rise-time dependent constant parameter $N_3$ as shown in the Appendix B in Equation 3.24 to get a simplified result as compared to newton raphson method consuming less computation time.

Hence after proceeding by the approximation method we get the following results for T2.

$$T_2 = [\frac{C[V_{dd} - V_x] + K}{\frac{\beta_n}{2}V_{tn}S_LN_3}]^{1/2} \tag{3.25}$$

After analysing the above equations we see that all the unknown parameters in terms of T1 , T2 are being modeled and the only unknown that is left is T3. Before proceeding towards the calculation of T3 we see that we require the crossover voltage to be calculated as it is required in Equation 3.25.

For calculating the crossover voltage we proceed as follows. This basic assumption of the cross-over voltage has been made after carefully analyzing the behavior of the cross-over voltage with the change in the rise time or change in the capacitive load.

From the Figure 3.11 it is seen that with the increase in rise time the cross-over voltage reduces. When we plot the curve for the behavior of cross-over voltage with change in rise time it very well approximates the Equation 3.26 and hence confirming the assumption.

Hence we assume the following

$$V_x = V_{dd} \exp \frac{-t_{rise}}{NT_a} \tag{3.26}$$

Where

$t_{rise}$ = the rise time of the applied input voltage

N = is a constant dependent on the capacitive load

$T_a$ = is the RC dependent time constant

To standardize the assumption of the cross-over voltage ($V_x$) in Equation 3.26 for a wider range of capacitive load and rise times, the constant N is included.

After analysing the various simulation results and carefully observing the behavior of the cross-over voltage, with the change in rise time and change in capacitive load the behavior of N was confirmed as shown in the Figure 3.12 which strengthens the basis of assumption.

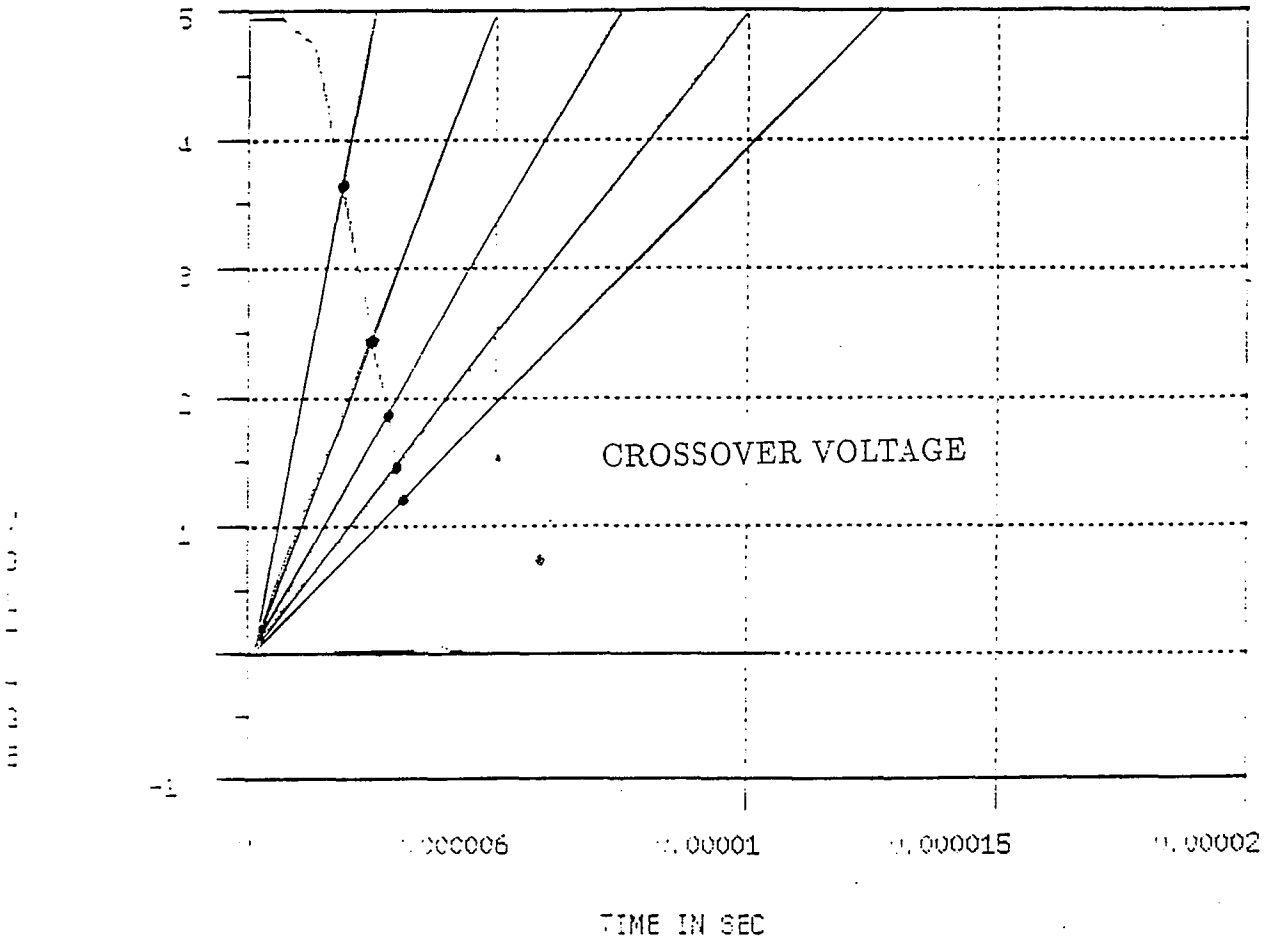


Figure 3.11: Behavior of cross-over voltage with change in rise-time

It is seen that for smaller load capacitance the discharging of the capacitance is fast as compared to the higher capacitive value, hence a constant factor is include to take care of the above and holding the assumption good.

Here $T_a$ is the time constant of the circuit. The time constant $T_a$ was deduced after analyzing the basic circuit of RC circuit, where the discharging voltage at any instant of time is given by the following equation $V_t = V_{peak} \exp \frac{-t}{T_c}$. Where $T_c$ is the circuit time constant dependent on the resistance and the capacitance of the circuit. So on the similar basis after a large number simulation runs the behavior of $T_a$ was derived.

After analyzing the nature of the time-constant from the Figure 3.13 it is seen that $T_a$ is given as follows

$$Ta = 0.95 * t_{rise} + K \tag{3.27}$$

where

$$K = R_l * C_l \tag{3.28}$$

and the value 0.95 in the above equation is the process dependent parameter, hence the above equation becomes as follows

$$Ta = 0.95 * t_{rise} + R_l C_l \tag{3.29}$$

Here we complete the calculation of the first part that is the time T1 and the time T2 and the only unknown parameter left for calculating the final time delay is T3, know we shall analyse the approach for handling T3.

### 3.4.3 Region2: n-channel Device in Linear Region

The above basic Equation 3.3 show that the current flowing through the n-device during the interval T2 to T3 is linear current. Since the gate to source voltage of the n-device is more than the drain to source voltage of the device. Whereas the p-device is in saturation, proceeding on the same grounds of the charge equation

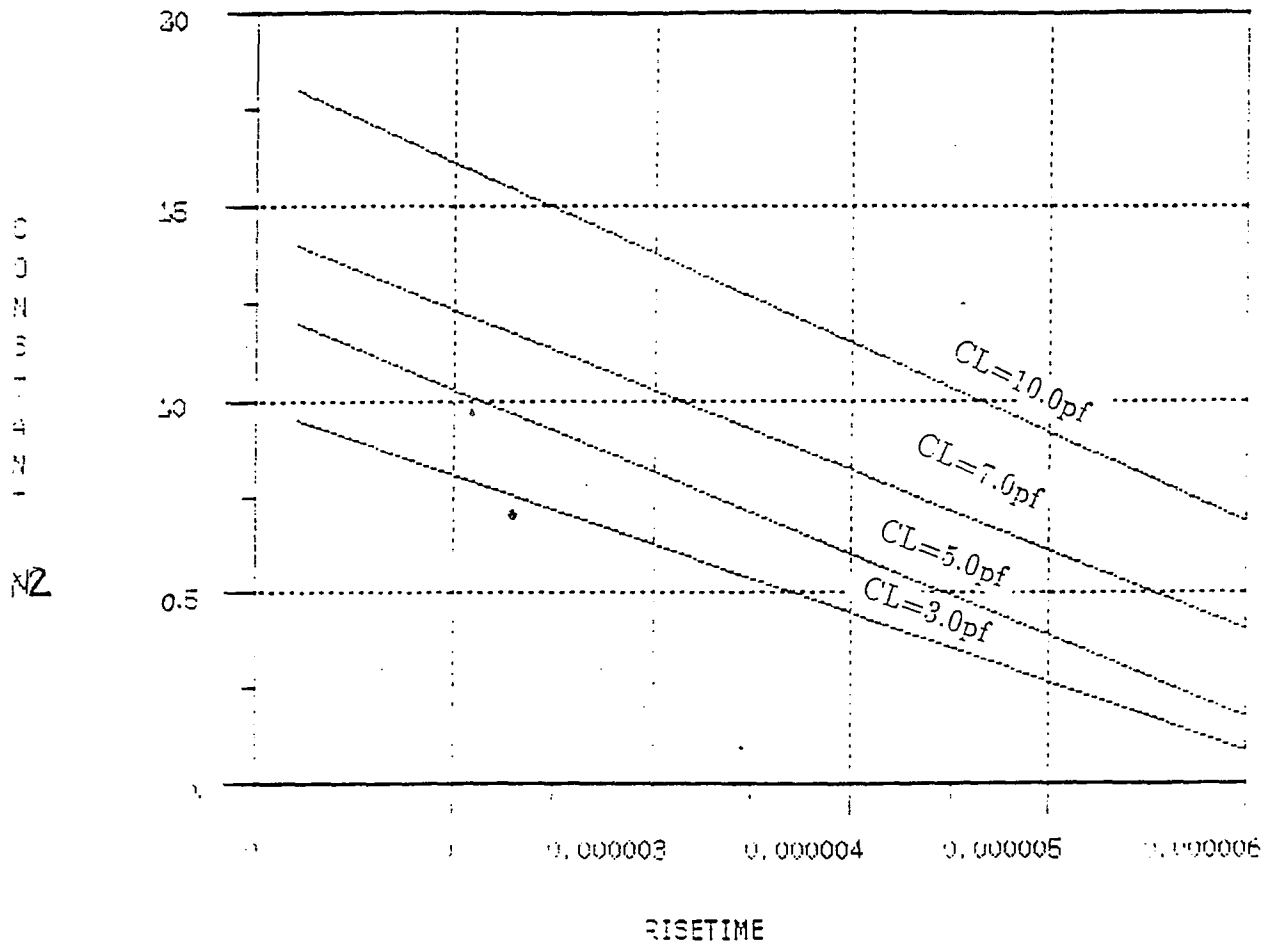


Figure 3.12: Behavior of constant N with respect to rise time

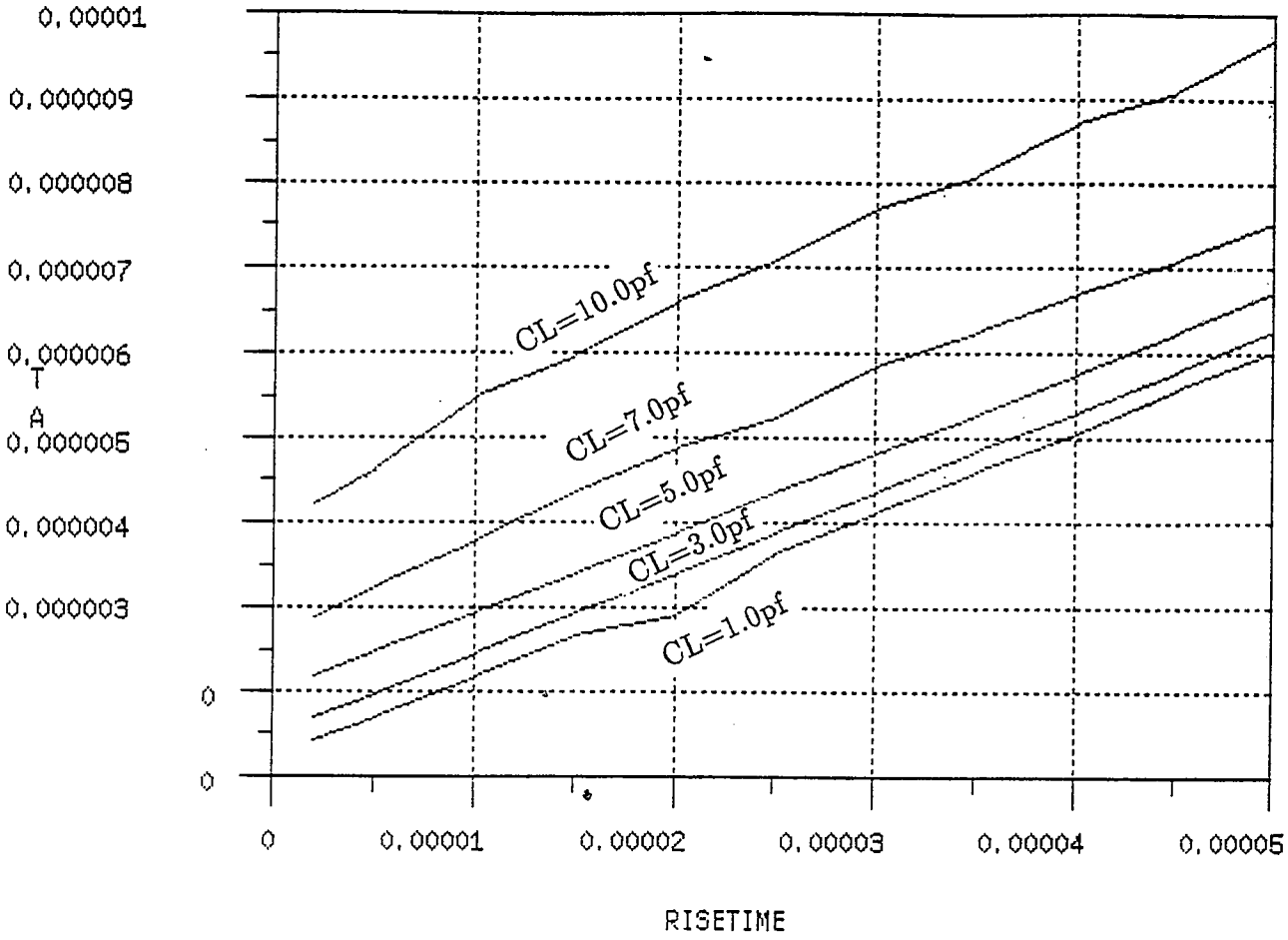


Figure 3.13:
Representation of Ta with respect to rise-time for various capacitive load

we get, the charge stored in the capacitor during the interval T2 to T3 is given by the equation

$$Q_b = \int i dt = -\int C dV_o \tag{3.30}$$

the above equation can be simplified in the form given below

$$i_l = -C\frac{d}{dt}V_o \tag{3.31}$$

at t=to

Since the fall time is the time taken by the output voltage to decay from 90 percent to 10 percent, (i.e from $0.9V_{dd}$ to $0.1V_{dd}$) hence in the case T3 is the point at which the output voltage is $0.1V_{dd}$, so the above equation appears as,

$$i_L = -C\frac{d}{dt}V_o \tag{3.32}$$

at t= T3

Analysing the simulation results for various set of capacitive load and rise-time we come to an conclusion that behavior of the output voltage with the increase in the rise time approximates an gaussian curve, which is seen and confirmed in the Figure 3.14 hence on the same criteria this model treats the behavior of the output voltage close to gaussian and proceeds

$$V_o = V_{dd} \exp \frac{-t^{3/2}}{2{T_x}^{3/2}} \tag{3.33}$$

substituting $V_o$ in the above Equation 3.32 we get,

$$i_L = -C\frac{d}{dt}[V_{dd} \exp \frac{-t^{3/2}}{{T_x}^{3/2}}] \tag{3.34}$$

In the above equation it is seen that $i_{ds(n)}$ is the linear current and is given as follows,

$$i_{dsn} = i_L = \beta_n[[V_{in} - V_{tn}]V_o - \frac{V_o^2}{2}] \tag{3.35}$$

but as per the above explanation it is seen that at instant of time T3 the output voltage is equal to $0.1V_{dd}$ and the input voltage in most of the cases is $V_{dd}$ we get,

$$i_{dsn} = i_L = \beta_n[[V_{in} - V_{tn}]0.1V_{dd} - \frac{0.1{V_{dd}}^2}{2}] \tag{3.36}$$

The time constant $T_x$ in Equation 3.34 is given as follows,

Since from the Figure 3.10 we know the voltage at an instant of time T2 is the cross-over voltage ($V_x$) when the current in circuit is maximim. Substituting the value of T2 and the voltage $V_x$ in Equation 3.33 we get the value of the time constant $T_x$,

$$V_x = V_{dd} \exp \frac{-{T_2}^{3/2}}{2{T_x}^{3/2}} \tag{3.37}$$

simplifying the above equation we get

$$T_x = [\frac{-{T_2}^{3/2}}{2ln\frac{V_x}{V_{dd}}}]^{2/3} \tag{3.38}$$

Hence substituting the above Equations 3.36 and 3.33 in 3.32 we get,

$$\beta_n[[V_{in} - V_{tn}]0.1V_{dd} - \frac{0.1{V_{dd}}^2}{2}] = -C_l\frac{d}{dt}V_{dd} \exp \frac{-t^{3/2}}{2{T_x}^{3/2}} \tag{3.39}$$

and hence we get

$$i_{dsn} = -C_L V_{dd}\frac{d}{dt} \exp \frac{-t^{3/2}}{2{T_x}^{3/2}} \tag{3.40}$$

on solving the differential equation we get

$$i_{dsn} = -C_L V_{dd}[\frac{3t^{1/2}\exp\frac{-t^{3/2}}{2T_x{}^{3/2}}}{4T_x{}^{3/2}}] \tag{3.41}$$

simplifying the above equation results in

$$i_{dsn} = \frac{C_L V_{dd} 3T_3^{1/2} \exp\frac{-T_3{}^{3/2}}{2T_x{}^{3/2}}}{4T_x{}^{3/2}} \tag{3.42}$$

simplifying the equation further

$$\frac{i_{dsn}4T_x{}^{3/2}}{3C_L V_{dd}} = T_3{}^{1/2} \exp\frac{-T_3{}^{3/2}}{2T_x{}^{3/2}} \tag{3.43}$$

to solve the exponential equation, we take logrithmic on both the sides

$$\ln\exp\frac{-T_3{}^{3/2}}{2T_x{}^{3/2}} = \ln\frac{i_{dsn}4T_x{}^{3/2}}{3C_L V_{dd} T_3{}^{1/2}} \tag{3.44}$$

algebraic simplification results in

$$\frac{-T_3{}^{3/2}}{2T_x{}^{3/2}} = \ln\frac{i_{dsn}4T_x{}^{3/2}}{3C_L V_{dd}} - \ln T_3{}^{1/2} \tag{3.45}$$

on simplification we get

$$\frac{-T_3{}^{3/2}}{2T_x{}^{3/2}} + \ln T_3{}^{1/2} = \ln\frac{i_{dsn}4T_x{}^{3/2}}{3C_L V_{dd}} \tag{3.46}$$

In the above equation all the parameters on the right hand side are known and hence solving the above equation by newton raphson method or the approximation method shall give the value of the T3, a program is attached in the Appendix B which solves the above equation and gives the value of T3 by the approximation method. After a large number of simulation runs it was obserevd that the middle parameter in Equation 3.46 had a negligble effect on the required performance but

for better accuracy a emiprical rise-time dependent constant $N_4$ refered in Appendix B is used to get the accurate solution with less computational time.

So all the necessary parameters such as T1, T2 and T3 for calculating the delay are known. The fall time delay is given as follows

So if we substitute the empirical constant $N_4$ in the Equation 3.46 we get

$$\frac{-{T_3}^{3/2}}{2{T_x}^{3/2}} N_4 = \ln \frac{i_{dsn} 4{T_x}^{3/2}}{3 C_l V_{dd}} \tag{3.47}$$

$$T_d = T_3 - T_1 \tag{3.48}$$

$$T_d = \frac{-{T_3}^{3/2}}{2{T_x}^{3/2}} + \ln {T_3}^{1/2} - \ln \frac{i_{dsn(sat)} 4{T_x}^{3/2}}{3 C_L V_{dd}} + \frac{V_{tn} t_{rise}}{V_{dd}} \tag{3.49}$$

## 3.5 Rise Time Delay Estimation

The results presented in the previous section can be used to compute the rise time of a CMOS inverter, by substituting all the (n) subscripts with (p). When using previous equations to compute the rise time delay, it is important to introduce the following changes.

[1] The threshold voltage of the p- channel, which has a negative value, must be included in the equation with opposite sign (i.e always positive).

[2] $V_o$ is the complement to $V_{dd}$, of the actual $V_o$ we need to compute. If for instance, we want to compute the rise-time delay to 4.0v, $V_o$ will be actually $V_{dd} - V_o$ =1.0v (for $V_{dd}$=5v).

Similarly an analysis can be carried out for the other standard gates and hence for a given circuit, we can precisely proceed towards the accurate timing analysis.

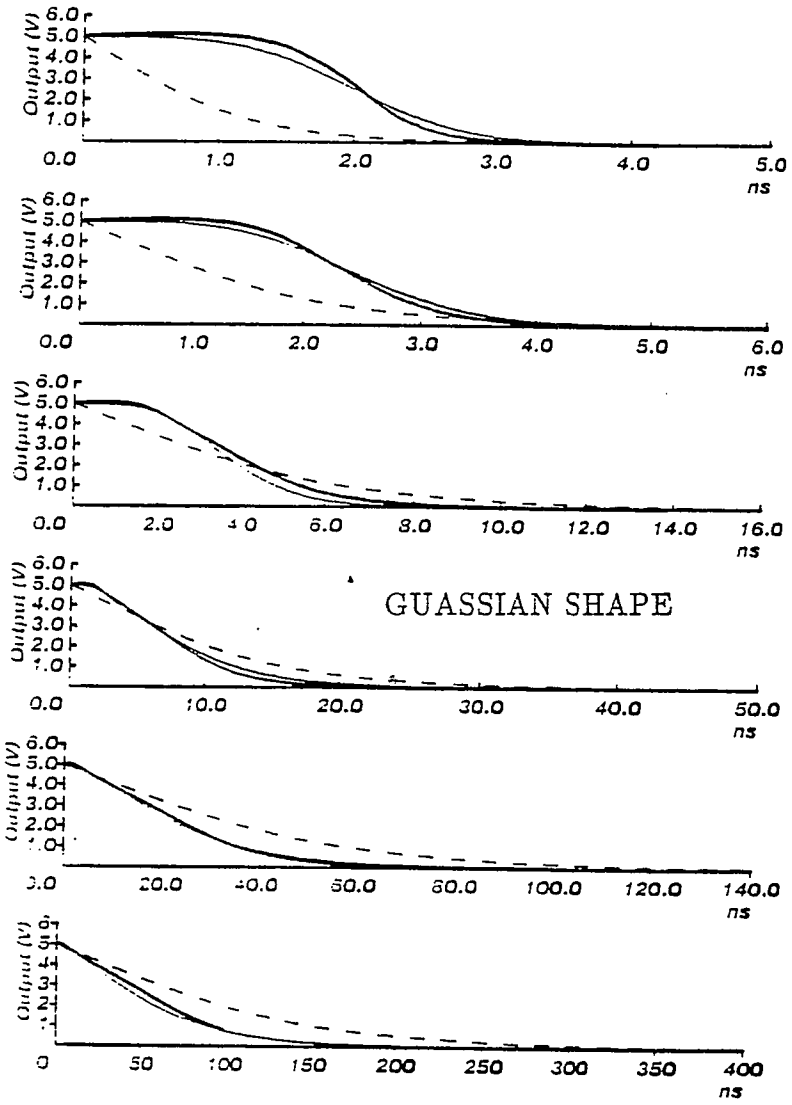


Figure 3.14:
Series of output voltage waveforms for various capacitive load confirming the Guassian nature[1]

### 3.5.1 Extension of the above Model for NAND and NOR Gates

In M-input NAND- or NOR- gates the delay Td generally can be calculated by the method similar to that of the inverter.

Spice simulations[1] for NAND- and NOR- gates, indicate that the output voltage for worst-case input signals are very similar to the output signals of symmetrical inverters. This similarity is MOS specific, a MOS transistor behaves (in lowest order) like a switched resistor. Then a series connection of devices behave like the switched series resistance, i.e., like an effective transistor with a reduced width. Since either a single one of the parallel devices or the effective series device is activated, we can regard NAND- and NOR- gates as effective inverters and hence we can calculate signal delays for these gates according to the inverter delay formula with appropriate gate type specific parameters such as the transconductance, transistor source or drain capacitance and the typical delay values.

# Chapter 4

# DISCUSSION ON SIMULATION AND MODEL TEST RESULTS

## 4.1 Introduction

This is the most important part of the entire thesis where the developed model results are being compared with the SPICE simulation results. Also the various assumptions while developing the model are very throughly discussed. The basic objective of developing an empirical timing model with least error in the calculation of delay, with simplified numerical representation, is very satisfactorily acheived.

In the subsequent sections we shall first see the sample calculations, and then shall proceed further veryfing the assumptions made during the various stages of the model development. Lastly comparing the SPICE simulation results with the model test results.

## 4.2 Sample Calculation

**Input Data**

[1] Supply voltage (Vdd) = 5volts

[2] Rise time ($T_{rise}$) = 10ns

[3] Threshold voltage ($V_{tn}$) = 0.59volts

[4] Transistor gain factor ($\beta_n$) = 1.3E-3amps/volts

[5] Load Capacitance ($C_l$) = 3E-12farads

[6] Slope ($S_L$) = 5E-8

[7] Resistance $R_l = 100\Omega$

**Calculation**

$$V_{gs} = \frac{V_{dd}t}{t_{rise}}$$

$$V_{tn} = \frac{V_{dd}t_1}{t_{rise}}$$

$$T_1 = \frac{V_{tn}}{slope}$$

T1 = 0.59 / [(5) / (10E-9)]
T1 = 1.18E-09 sec

$$T_a = 0.95 * t_{rise} + R_l C_l$$

Ta = 0.955 * 10E-9 + 100 * 3E-12
Ta = 12.5E-09 sec

$$V_x = V_{dd}\exp\frac{-t_{rise}}{T_a}$$

Vx = 5 * EXP [(-10E-9)/(12.5E-09)]

Vx =2.24V

$$T_2 = \frac{C(V_{dd} - V_x)}{\frac{\beta_n N_3 S_L V_{tn}}{2}}$$

T2 = [(3EXP-12)*(5 - Vx)]/[0.5*6.2*0.5EXP-08*1.3EXP-03*0.59]
T2 = 2.64E-09 sec

The Equation T2 can be calculated by various techniques as explianed in the chapter 3. We have the newton raphson method, and the approximation method. We use the approximation method for calculation of T2, reasons for using this method is explained in details in Appendix B. The value of constant $N_3$ in the above equation is obtained from Figure B.1. Figure B.1 and the equation attached in the Appendix B, are obtained after large simulation runs. It is seen that for both the two methods the results are approximately the same, but the compuatation time is more in Newton Raphson method which takes large iteration time.

$$T_x = \left(\frac{-T_2^{3/2}}{2\ln\frac{V_x}{V_{dd}}}\right)^{2/3}$$

Tx = [-2.64E-09 *(1.5)]/[2*ln(2.24/5.0)]exp[.666]
Tx = 1.95E-09

$$-T_3^{3/2} = 2T_x^{3/2}\ln\frac{4I_l T_x^{3/2}}{3C_l V_{dd}} - 2T_x^{3/2}\ln T_3^{1/2}$$

Solution of T3 can be obtained by Newton Raphson or approximation method as explained in the chapter 3.

On proceeding by the approximation, which is simplified, accurate and fast to compute, a rise-time dependent constant $N_4$ described in the Appendix B and chapter 3 is substituted in the above equation.

Hence the above equation of T3 becomes as follows,

$$-T_3^{3/2}N_4 = 2T_x^{3/2}\ln\frac{4I_l T_x^{3/2}}{3C_l V_{dd}}$$

Here the value of the constant $N_4$ from the equation attached in the appendix is 12.0, hence on substituting all the parameters in the above equation we get,

T3= 2.83E-09 sec

Once all the required parameters are known, now as per the definition we proceed towards the calcuation of the delay,

Delay = T3 - T1

TD = 1.6E-09 sec

## 4.3 Discussion on the Results

The discussion of the entire analysis is divided into two parts

1. Discussion on the assumptions.
2. Discussion on the timing calculation.

**Discussion on the assumptions:** This section compares the SPICE simulation results with the Model results for various assumptions that were made.

The assumptions made at different stages were about the behavior of the cross-over voltages, the time constant and a constant term N in the Equation 3.26 of cross-over voltage and the behavior of the output voltage.

This Table 4.1 given below shows a comparision between the SPICE simulation results and the Model results for load capacitance of 0.5pf for first assumption of cross-over voltage. The results strongly confirms the assumption of the cross-over voltage. This assumption is the primmary step before we go ahead for further calculation of T2. The basic reason for assuming the given equation is because the behavior of output voltage with respect to rise following the same shape. A Figure 4.1 shows the nature of the cross-over voltage

**Assumption for Cross-over voltage**

$$V_x = V_{dd} \exp \frac{-T_{rise}}{NT_a} \tag{4.1}$$

**Table 4.1 Behavior of Cross-over Voltage**

| *SPICE simulation results* | | | *MODEL test results* | |
|---|---|---|---|---|
| Obs No | Rise time in seconds | Cross-over Voltage in volts | Rise time in seconds | Cross-over Voltage in volts |
| 1 | 2E-09 | 1.0 | 2E-09 | 0.7 |
| 2 | 3E-09 | 0.95 | 3E-09 | 0.68 |
| 3 | 4E-09 | 0.86 | 4E-09 | 0.65 |
| 4 | 5E-09 | 0.79 | 5E-09 | 0.62 |
| 5 | 6E-09 | 0.75 | 6E-09 | 0.61 |
| 6 | 7E-09 | 0.71 | 7E-09 | 0.58 |
| 7 | 8E-09 | 0.66 | 8E-09 | 0.54 |
| 8 | 9E-09 | 0.61 | 9E-09 | 0.51 |
| 9 | 10E-09 | 0.585 | 10E-09 | 0.48 |
| 10 | 11E-09 | 0.55 | 11E-09 | 0.44 |
| 11 | 12E-09 | 0.53 | 12E-09 | 0.42 |
| 12 | 13E-09 | 0.51 | 13E-09 | 0.40 |
| 13 | 14E-09 | 0.48 | 14E-09 | 0.39 |
| 14 | 15E-09 | 0.468 | 15E-09 | 0.385 |
| 15 | 20E-09 | 0.46 | 20E-09 | 0.381 |
| 16 | 25E-09 | 0.45 | 25E-09 | 0.38 |
| 17 | 30E-09 | 0.42 | 30E-09 | 0.376 |
| 18 | 35E-09 | 0.41 | 35E-09 | 0.371 |
| 19 | 40E-09 | 0.407 | 40E-09 | 0.365 |
| 20 | 45E-09 | 0.403 | 45E-09 | 0.361 |
| 21 | 50E-09 | 0.4 | 50E-09 | 0.36 |

The graph of cross-over voltage versus the rise time for various values of capacitive load is shown in Figure 4.1 which further confirms the assumption.

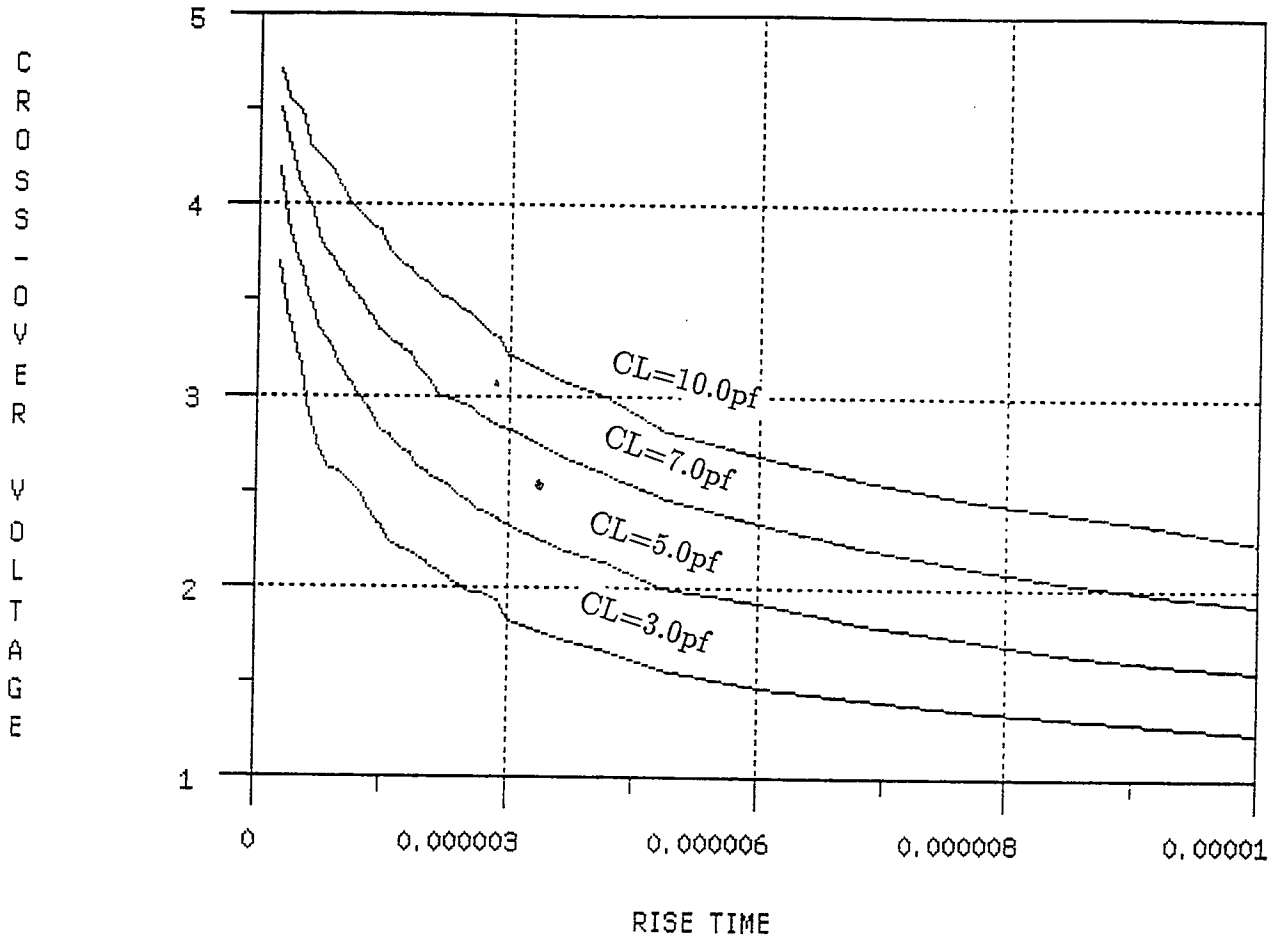


Figure 4.1: Graph of cross over voltage from simulation results

The above Equation 4.1 gives the performance of cross-over voltage. But we have two unknown factors$T_a$ and N in it. We calculate the value of $T_a$ as given in Equation 4.2 and as explianed in chapter3.

The assumption of $T_a$, when compared with SPICE simulation results give fairly accurate results. Table 4.2 shows the behavior of $T_a$ for load capacitance of 0.5pf.

**Assumption of Ta for getting Cross-over voltage**

$$T_a = 0.95 * T_{rise} + R_l C_l \tag{4.2}$$

**Table 4.2 Parameter Ta**

| *Spice simulation results* | | | *Model test results* | |
|---|---|---|---|---|
| Obs No | Rise time in seconds | Time-constant(Ta) in seconds | Rise time in seconds | Time-constant (Ta) in seconds |
| 1 | 2E-09 | 1.09E-09 | 2E-09 | 1.14E-09 |
| 2 | 3E-09 | 2.27E-09 | 3E-09 | 2.28E-09 |
| 3 | 4E-09 | 3.67E-09 | 4E-09 | 3.42E-09 |
| 4 | 5E-09 | 4.32E-09 | 5E-09 | 4.56E-09 |
| 5 | 6E-09 | 5.23E-09 | 6E-09 | 5.7E-09 |
| 6 | 7E-09 | 6.65E-09 | 7E-09 | 6.84E-09 |
| 7 | 8E-09 | 7.76E-09 | 8E-09 | 7.98E-09 |
| 8 | 9E-09 | 9.31E-09 | 9E-09 | 9.12E-09 |
| 9 | 10E-09 | 9.97E-09 | 10E-09 | 10.26E-09 |
| 10 | 11E-09 | 10.0E-09 | 11E-09 | 10.3E-09 |
| 11 | 12E-09 | 10.1E-09 | 12E-09 | 10.7E-09 |
| 12 | 13E-09 | 10.2E-09 | 13E-09 | 10.8E-09 |
| 13 | 14E-09 | 10.3E-09 | 14E-09 | 11.2E-09 |
| 14 | 15E-09 | 11.3E-09 | 15E-09 | 11.96E-09 |
| 15 | 20E-09 | 14.3E-09 | 20E-09 | 15.76E-09 |
| 16 | 25E-09 | 18.8E-09 | 25E-09 | 19.56E-09 |
| 17 | 30E-09 | 22.4E-09 | 30E-09 | 23.33E-09 |
| 18 | 35E-09 | 26.7E-09 | 35E-09 | 27.18E-09 |
| 19 | 40E-09 | 30.1E-09 | 40E-09 | 30.9E-09 |
| 20 | 45E-09 | 34.2E-09 | 45E-09 | 34.7E-09 |
| 21 | 50E-09 | 37.2E-09 | 50E-09 | 38.5E-09 |

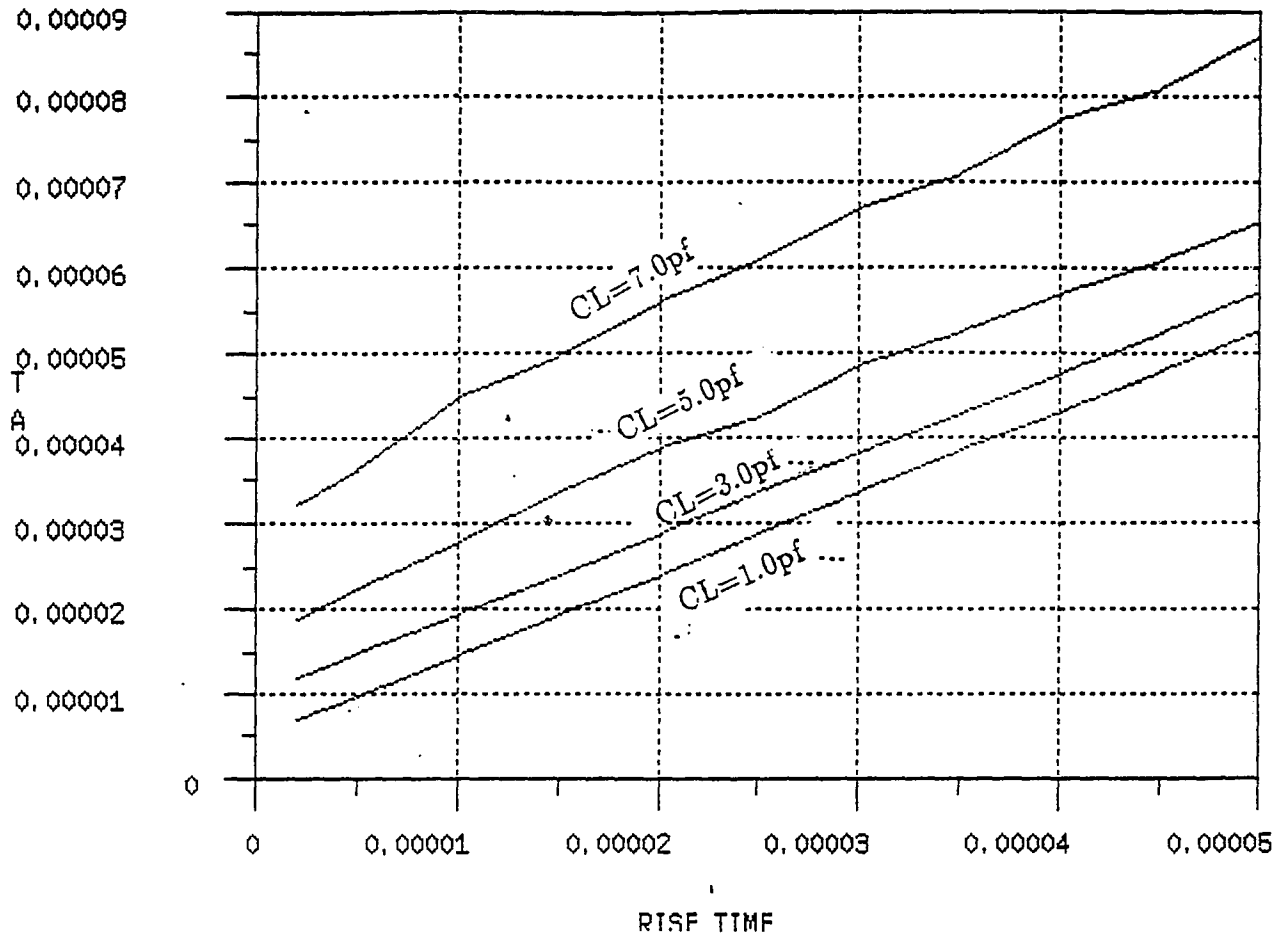


Figure 4.2: Graph of constant Ta versus rise time

The third unknown parameter N in the above Equation 4.1 exhibits the behavior as shown in the Figure 4.3 and discussed in the chapter3. To standardize the model for various capacitive load and rise times these constant is essential. From the various simulation results the nature of the constant is confirmed. Table 4.3 gives the comparison of the assumption N for load capacitance of 0.5pf

**Assumption for the term N**

Table 4.3 Parameter N

| *Spice simulation results* | | | *Model test results* | |
|---|---|---|---|---|
| Obs No | Rise time in seconds | Constant (N) | Rise time in seconds | Constant (N) |
| 1 | 2E-09 | 0.60 | 2E-09 | 0.5 |
| 2 | 3E-09 | 0.52 | 3E-09 | 0.49 |
| 3 | 4E-09 | 0.47 | 4E-09 | 0.487 |
| 4 | 5E-09 | 0.4685 | 5E-09 | 0.472 |
| 5 | 6E-09 | 0.468 | 6E-09 | 0.47 |
| 6 | 7E-09 | 0.4679 | 7E-09 | 0.465 |
| 7 | 8E-09 | 0.4672 | 8E-09 | 0.457 |
| 8 | 9E-09 | 0.467 | 9E-09 | 0.445 |
| 9 | 10E-09 | 0.466 | 10E-09 | 0.441 |
| 10 | 11E-09 | 0.465 | 11E-09 | 0.439 |
| 11 | 12E-09 | 0.463 | 12E-09 | 0.432 |
| 12 | 13E-09 | 0.46 | 13E-09 | 0.429 |
| 13 | 14E-09 | 0.45 | 14E-09 | 0.425 |
| 14 | 15E-09 | 0.44 | 15E-09 | 0.422 |
| 15 | 20E-09 | 0.424 | 20E-09 | 0.415 |
| 16 | 25E-09 | 0.42 | 25E-09 | 0.411 |
| 17 | 30E-09 | 0.40 | 30E-09 | 0.407 |
| 18 | 35E-09 | 0.39 | 35E-09 | 0.406 |
| 19 | 40E-09 | 0.388 | 40E-09 | 0.402 |
| 20 | 45E-09 | 0.383 | 45E-09 | 0.401 |
| 21 | 50E-09 | 0.38 | 50E-09 | 0.4 |

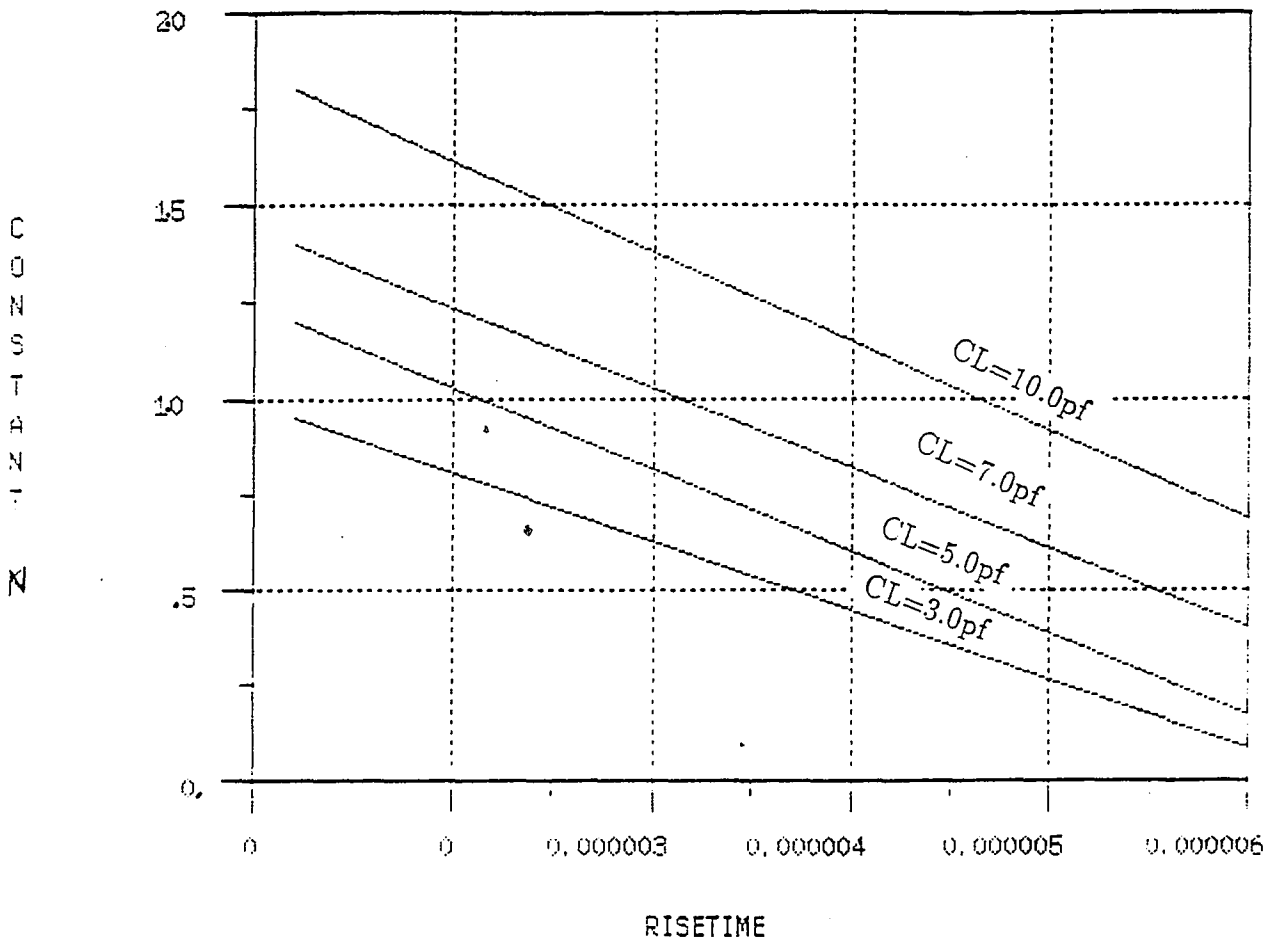


Figure 4.3: Graph of the constant N used in equation of Vx

The table given below compares the behavior of output voltage at various instant of time. It confirms the second assumption made during the calculation of T3. The accuracy and the entire timing analysis was based on this assumption, which was one of the important among the others. It is observed that the results are quite accurate. The Table 4.4 depicts the behavior of the output voltage for load capacitance of 0.5pf

**Assumption of Output voltage**

$$V_o = V_{dd} \exp \frac{-t^{\frac{3}{2}}}{2T^{\frac{3}{2}}} \tag{4.3}$$

**Table 4.4 Output Voltage**

| *Model test results* | | | *Simulation results* | |
|---|---|---|---|---|
| Obs No | Instantenous time in sec | Output voltage in volts | Instantaneous time in sec | Output voltage in volts |
| 1 | 0.2E-09 | 1.45 | 2E-09 | 1.42 |
| 2 | 0.3E-09 | 1.0 | 3E-09 | 1.1 |
| 3 | 0.4E-09 | 0.96 | 4E-09 | 1.03 |
| 4 | 0.5E-09 | 0.92 | 5E-09 | 0.97 |
| 5 | 0.6E-09 | 0.88 | 6E-09 | 0.93 |
| 6 | 0.7E-09 | 0.84 | 7E-09 | 0.88 |
| 7 | 0.8E-09 | 0.77 | 8E-09 | 0.83 |
| 8 | 0.9E-09 | 0.73 | 9E-09 | 0.80 |
| 9 | 1.0E-09 | 0.67 | 10E-09 | 0.74 |
| 10 | 1.1E-09 | 0.63 | 11E-09 | 0.67 |
| 11 | 1.2E-09 | 0.61 | 12E-09 | 0.63 |
| 12 | 1.3E-09 | 0.59 | 13E-09 | 0.61 |
| 13 | 1.4E-09 | 0.587 | 14E-09 | 0.609 |
| 14 | 1.5E-09 | 0.58 | 15E-09 | 0.59 |
| 15 | 2.0E-09 | 0.58 | 20E-09 | 0.55 |
| 16 | 2.5E-09 | 0.45 | 25E-09 | 0.48 |
| 17 | 3.0E-09 | 0.4 | 30E-09 | 0.43 |
| 18 | 3.5E-09 | 0.32 | 35E-09 | 0.38 |
| 19 | 4.0E-09 | 0.31 | 40E-09 | 0.35 |
| 20 | 4.5E-09 | 0.28 | 45E-09 | 0.31 |
| 21 | 5.0E-09 | 0.25 | 50E-09 | 0.28 |

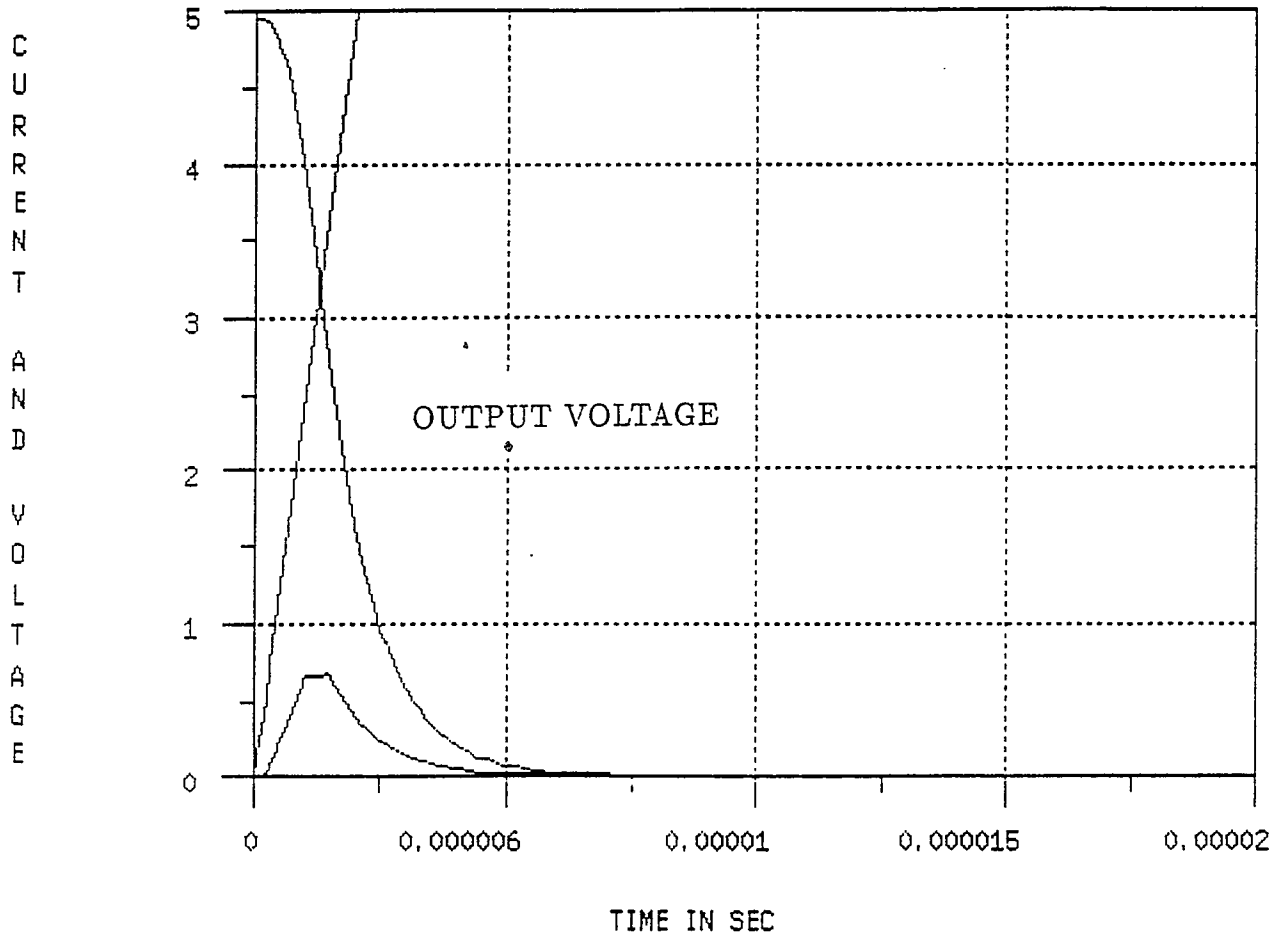


Figure 4.4: Graph of output voltage versus various instant of time for Cl=0.5pf

After going through the discussion on the assumption made, we now proceed towards the discussion of the timing analysis. The discussion on timing analysis shall ultimately conclude with the computation of the delay.

We shall initially start by calculating T1. As discussed in chapter3 T1 is the point at which the n-device starts conducting, and now we check the performance of T1 by comparing the SPICE results with the Model results.

**Tables 4.5 Performance of T1**

| *Load Capacitance = 0.1pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.2E-09 | 0.236E-09 |
| 2 | 3E-09 | 0.346E-09 | 0.352E-09 |
| 3 | 4E-09 | 0.46E-09 | 0.472E-09 |
| 4 | 5E-09 | 0.5E-09 | 0.591E-09 |
| 5 | 6E-09 | 0.6E-09 | 0.707E-09 |
| 6 | 7E-09 | 0.7E-09 | 0.821E-09 |
| 7 | 8E-09 | 0.85E-09 | 0.941E-09 |
| 8 | 9E-09 | 0.94E-09 | 1.01E-09 |
| 9 | 10E-09 | 1.07E-09 | 1.12E-09 |
| 10 | 11E-09 | 1.14E-09 | 1.292E-09 |
| 11 | 12E-09 | 1.4E-09 | 1.411E-09 |
| 12 | 13E-09 | 1.55E-09 | 1.531E-09 |
| 13 | 14E-09 | 1.65E-09 | 1.652E-09 |
| 14 | 15E-09 | 1.689E-09 | 1.771E-09 |
| 15 | 20E-09 | 2.2E-09 | 2.362E-09 |
| 16 | 25E-09 | 2.9E-09 | 2.952E-09 |
| 17 | 30E-09 | 3.3E-09 | 3.521E-09 |
| 18 | 35E-09 | 4.02E-09 | 4.132E-09 |
| 19 | 40E-09 | 4.6E-09 | 4.723E-09 |
| 20 | 45E-09 | 5.1E-09 | 5.321E-09 |
| 21 | 50E-09 | 5.5E-09 | 5.892E-09 |

**Table 4.6 Performance of T1**

| *Load capacitance 0.5pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.2E-09 | 0.236E-09 |
| 2 | 3E-09 | 0.346E-09 | 0.352E-09 |
| 3 | 4E-09 | 0.46E-09 | 0.472E-09 |
| 4 | 5E-09 | 0.5E-09 | 0.592E-09 |
| 5 | 6E-09 | 0.6E-09 | 0.707E-09 |
| 6 | 7E-09 | 0.7E-09 | 0.821E-09 |
| 7 | 8E-09 | 0.85E-09 | 0.94E-09 |
| 8 | 9E-09 | 0.94E-09 | 1.01E-09 |
| 9 | 10E-09 | 1.07E-09 | 1.12E-09 |
| 10 | 11E-09 | 1.14E-09 | 1.292E-09 |
| 11 | 12E-09 | 1.4E-09 | 1.413E-09 |
| 12 | 13E-09 | 1.55E-09 | 1.532E-09 |
| 13 | 14E-09 | 1.65E-09 | 1.651E-09 |
| 14 | 15E-09 | 1.689E-09 | 1.771E-09 |
| 15 | 20E-09 | 2.2E-09 | 2.362E-09 |
| 16 | 25E-09 | 2.9E-09 | 2.951E-09 |
| 17 | 30E-09 | 3.3E-09 | 3.521E-09 |
| 18 | 35E-09 | 4.02E-09 | 4.131E-09 |
| 19 | 40E-09 | 4.6E-09 | 4.72E-09 |
| 20 | 45E-09 | 5.1E-09 | 5.312E-09 |
| 21 | 50E-09 | 5.5E-09 | 5.892E-09 |

**Table 4.7 Performance of T1**

| *Load Capacitance = 1pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.2E-09 | 0.236E-09 |
| 2 | 3E-09 | 0.346E-09 | 0.354E-09 |
| 3 | 4E-09 | 0.46E-09 | 0.472E-09 |
| 4 | 5E-09 | 0.5E-09 | 0.591E-09 |
| 5 | 6E-09 | 0.7E-09 | 0.707E-09 |
| 6 | 7E-09 | 0.8E-09 | 0.823E-09 |
| 7 | 8E-09 | 0.85E-09 | 0.941E-09 |
| 8 | 9E-09 | 0.94E-09 | 1.012E-09 |
| 9 | 10E-09 | 1.07E-09 | 1.12E-09 |
| 10 | 11E-09 | 1.14E-09 | 1.29E-09 |
| 11 | 12E-09 | 1.4E-09 | 1.41E-09 |
| 12 | 13E-09 | 1.55E-09 | 1.53E-09 |
| 13 | 14E-09 | 1.65E-09 | 1.65E-09 |
| 14 | 15E-09 | 1.689E-09 | 1.77E-09 |
| 15 | 20E-09 | 2.2E-09 | 2.36E-09 |
| 16 | 25E-09 | 2.9E-09 | 2.95E-09 |
| 17 | 30E-09 | 3.3E-09 | 3.52E-09 |
| 18 | 35E-09 | 4.02E-09 | 4.13E-09 |
| 19 | 40E-09 | 4.6E-09 | 4.72E-09 |
| 20 | 45E-09 | 5.1E-09 | 5.31E-09 |
| 21 | 50E-09 | 5.5E-09 | 5.89E-09 |

**Table 4.8 Performance of T1**

| *Load capacitance 3pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.2E-09 | 0.236E-09 |
| 2 | 3E-09 | 0.346E-09 | 0.354E-09 |
| 3 | 4E-09 | 0.46E-09 | 0.472E-09 |
| 4 | 5E-09 | 0.5E-09 | 0.592E-09 |
| 5 | 6E-09 | 0.6E-09 | 0.707E-09 |
| 6 | 7E-09 | 0.7E-09 | 0.821E-09 |
| 7 | 8E-09 | 0.85E-09 | 0.941E-09 |
| 8 | 9E-09 | 0.94E-09 | 1.01E-09 |
| 9 | 10E-09 | 1.07E-09 | 1.12E-09 |
| 10 | 11E-09 | 1.14E-09 | 1.292E-09 |
| 11 | 12E-09 | 1.4E-09 | 1.41E-09 |
| 12 | 13E-09 | 1.55E-09 | 1.53E-09 |
| 13 | 14E-09 | 1.65E-09 | 1.652E-09 |
| 14 | 15E-09 | 1.689E-09 | 1.772E-09 |
| 15 | 20E-09 | 2.2E-09 | 2.362E-09 |
| 16 | 25E-09 | 2.9E-09 | 2.952E-09 |
| 17 | 30E-09 | 3.3E-09 | 3.52E-09 |
| 18 | 35E-09 | 4.02E-09 | 4.132E-09 |
| 19 | 40E-09 | 4.6E-09 | 4.72E-09 |
| 20 | 45E-09 | 5.1E-09 | 5.31E-09 |
| 21 | 50E-09 | 5.5E-09 | 5.89E-09 |

In the above tables only four cases have been discussed, that means T1 has been calculated for four different values of capacitive load, whereas the circuit has been tested for a wide range of capacitive load ranging from 0.1pf to 50pf

After getting the required results of T1, we now proceed towards the calculative part of T2. T2 is the intermideate phase of the timing analysis and, is that point of time when the current in the circuit is maximum. It also an instant when the rising input voltage meets the falling output voltage

This table given below shows a comparision between the SPICE simulation results and the Model results, the assumptions and the calculative part are as discussed in chapter3.

**Table 4.9 Performance of T2**

| *Load Capacitance = 0.1pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.3E-09 | 0.26E-09 |
| 2 | 3E-09 | 0.4E-09 | 0.38E-09 |
| 3 | 4E-09 | 0.5E-09 | 0.44E-09 |
| 4 | 5E-09 | 0.6E-09 | 0.495E-09 |
| 5 | 6E-09 | 0.71E-09 | 0.65E-09 |
| 6 | 7E-09 | 0.83E-09 | 0.795E-09 |
| 7 | 8E-09 | 0.93E-09 | 0.87E-09 |
| 8 | 9E-09 | 1.12E-09 | 1.0E-09 |
| 9 | 10E-09 | 1.29E-09 | 1.1E-09 |
| 10 | 11E-09 | 1.32E-09 | 1.2E-09 |
| 11 | 12E-09 | 1.42E-09 | 1.32E-09 |
| 12 | 13E-09 | 1.53E-09 | 1.46E-09 |
| 13 | 14E-09 | 1.67E-09 | 1.56E-09 |
| 14 | 15E-09 | 1.79E-09 | 1.6E-09 |
| 15 | 20E-09 | 2.0E-09 | 1.9E-09 |
| 16 | 25E-09 | 2.4E-09 | 2.17E-09 |
| 17 | 30E-09 | 2.9E-09 | 2.7E-09 |
| 18 | 35E-09 | 3.2E-09 | 2.98E-09 |
| 19 | 40E-09 | 3.7E-09 | 3.5E-09 |
| 20 | 45E-09 | 4.01E-09 | 3.87E-09 |
| 21 | 50E-09 | 4.4E-09 | 4.12E-09 |

**Table 4.10 Performance of T2**

| *Load capacitance 0.5pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.4E-09 | 0.388E-09 |
| 2 | 3E-09 | 0.5E-09 | 0.484E-09 |
| 3 | 4E-09 | 0.6E-09 | 0.55E-09 |
| 4 | 5E-09 | 0.78E-09 | 0.66E-09 |
| 5 | 6E-09 | 0.85E-09 | 0.76E-09 |
| 6 | 7E-09 | 0.97E-09 | 0.87E-09 |
| 7 | 8E-09 | 1.18E-09 | 1.1E-09 |
| 8 | 9E-09 | 1.33E-09 | 1.48E-09 |
| 9 | 10E-09 | 1.5E-09 | 1.79E-09 |
| 10 | 11E-09 | 1.72E-09 | 1.88E-09 |
| 11 | 12E-09 | 1.91E-09 | 1.96E-09 |
| 12 | 13E-09 | 2.12E-09 | 2.04E-09 |
| 13 | 14E-09 | 2.3E-09 | 2.12E-09 |
| 14 | 15E-09 | 2.43E-09 | 2.23E-09 |
| 15 | 20E-09 | 2.6E-09 | 2.54E-09 |
| 16 | 25E-09 | 3.2E-09 | 2.85E-09 |
| 17 | 30E-09 | 3.9E-09 | 3.7E-09 |
| 18 | 35E-09 | 4.5E-09 | 4.4E-09 |
| 19 | 40E-09 | 4.9E-09 | 4.75E-09 |
| 20 | 45E-09 | 5.3E-09 | 5.17E-09 |
| 21 | 50E-09 | 5.8E-09 | 5.68E-09 |

**Table 4.11 Performance of T2**

| *Load Capacitance = 1pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.5E-09 | 0.47E-09 |
| 2 | 3E-09 | 0.6E-09 | 0.55E-09 |
| 3 | 4E-09 | 0.78E-09 | 0.695E-09 |
| 4 | 5E-09 | 0.97E-09 | 0.856E-09 |
| 5 | 6E-09 | 1.12E-09 | 1.06E-09 |
| 6 | 7E-09 | 1.29E-09 | 1.17E-09 |
| 7 | 8E-09 | 1.43E-09 | 1.32E-09 |
| 8 | 9E-09 | 1.54E-09 | 1.4E-09 |
| 9 | 10E-09 | 1.7E-09 | 1.53E-09 |
| 10 | 11E-09 | 1.9E-09 | 1.81E-09 |
| 11 | 12E-09 | 2.1E-09 | 2.02E-09 |
| 12 | 13E-09 | 2.3E-09 | 2.2E-09 |
| 13 | 14E-09 | 2.5E-09 | 2.43E-09 |
| 14 | 15E-09 | 2.7E-09 | 2.65E-09 |
| 15 | 20E-09 | 3.2E-09 | 3.4E-09 |
| 16 | 25E-09 | 3.7E-09 | 3.6E-09 |
| 17 | 30E-09 | 4.2E-09 | 4.0E-09 |
| 18 | 35E-09 | 4.8E-09 | 4.4E-09 |
| 19 | 40E-09 | 5.3E-09 | 4.96E-09 |
| 20 | 45E-09 | 5.8E-09 | 5.5E-09 |
| 21 | 50E-09 | 6.2E-09 | 5.85E-09 |

Table 4.12 Performance of T2

| *Load capacitance 3pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.7E-09 | 0.9E-09 |
| 2 | 3E-09 | 1.0E-09 | 1.18E-09 |
| 3 | 4E-09 | 1.25E-09 | 1.37E-09 |
| 4 | 5E-09 | 1.4E-09 | 1.53E-09 |
| 5 | 6E-09 | 1.55E-09 | 1.68E-09 |
| 6 | 7E-09 | 1.61E-09 | 1.81E-09 |
| 7 | 8E-09 | 1.85E-09 | 1.94E-09 |
| 8 | 9E-09 | 2.0E-09 | 2.05E-09 |
| 9 | 10E-09 | 2.2E-09 | 2.64E-09 |
| 10 | 11E-09 | 2.4E-09 | 2.77E-09 |
| 11 | 12E-09 | 2.71E-09 | 2.89E-09 |
| 12 | 13E-09 | 2.93E-09 | 3.01E-09 |
| 13 | 14E-09 | 3.1E-09 | 3.13E-09 |
| 14 | 15E-09 | 3.4E-09 | 3.24E-09 |
| 15 | 20E-09 | 4.2E-09 | 3.74E-09 |
| 16 | 25E-09 | 4.4E-09 | 4.2E-09 |
| 17 | 30E-09 | 4.9E-09 | 5.54E-09 |
| 18 | 35E-09 | 5.6E-09 | 5.98E-09 |
| 19 | 40E-09 | 6.3E-09 | 6.40E-09 |
| 20 | 45E-09 | 7.2E-09 | 6.76E-09 |
| 21 | 50E-09 | 7.8E-09 | 7.2E-09 |

In the above tables only four cases have been discussed, that means T2 has been calculated for four different values of capacitive load, whereas the circuit has been tested for a wide range of capacitive load ranging from 0.1pf to 50pf

We have got the results of T1 and T2 and the only parameter remaining is T3. The table given below compares the simulation results with model results and confirms the accuracyu.

**Table 4.13 Performance of T3**

| *Load Capacitance = 0.1pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.24E-09 | 0.277E-09 |
| 2 | 3E-09 | 0.384E-09 | 0.392E-09 |
| 3 | 4E-09 | 0.495E-09 | 0.514E-09 |
| 4 | 5E-09 | 0.536E-09 | 0.631E-09 |
| 5 | 6E-09 | 0.632E-09 | 0.736E-09 |
| 6 | 7E-09 | 0.7382E-09 | 0.862E-09 |
| 7 | 8E-09 | 0.888E-09 | 0.877E-09 |
| 8 | 9E-09 | 0.992E-09 | 1.04E-09 |
| 9 | 10E-09 | 1.37E-09 | 1.42E-09 |
| 10 | 11E-09 | 1.5E-09 | 1.54E-09 |
| 11 | 12E-09 | 1.72E-09 | 1.65E-09 |
| 12 | 13E-09 | 1.88E-09 | 1.73E-09 |
| 13 | 14E-09 | 1.93E-09 | 1.88E-09 |
| 14 | 15E-09 | 2.03E-09 | 1.97E-09 |
| 15 | 20E-09 | 2.5E-09 | 2.04E-09 |
| 16 | 25E-09 | 3.3E-09 | 2.46E-09 |
| 17 | 30E-09 | 4.0E-09 | 2.87E-09 |
| 18 | 35E-09 | 4.13E-09 | 3.52E-09 |
| 19 | 40E-09 | 4.57E-09 | 3.93E-09 |
| 20 | 45E-09 | 5.1E-09 | 4.36E-09 |
| 21 | 50E-09 | 5.47E-09 | 4.77E-09 |

**Table 4.14 Performance of T3**

| *Load capacitance 0.5pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in s econd |
| 1 | 2E-09 | 0.5E-09 | 0.493E-09 |
| 2 | 3E-09 | 0.656E-09 | 0.652E-09 |
| 3 | 4E-09 | 0.75E-09 | 0.774E-09 |
| 4 | 5E-09 | 0.895E-09 | 0.89E-09 |
| 5 | 6E-09 | 1.0E-09 | 1.05E-09 |
| 6 | 7E-09 | 1.17E-09 | 1.14E-09 |
| 7 | 8E-09 | 1.33E-09 | 1.27E-09 |
| 8 | 9E-09 | 1.44E-09 | 1.33E-09 |
| 9 | 10E-09 | 1.5E-09 | 1.54E-09 |
| 10 | 11E-09 | 1.62E-09 | 1.731E-09 |
| 11 | 12E-09 | 1.831E-09 | 1.865E-09 |
| 12 | 13E-09 | 1.974E-09 | 1.978E-09 |
| 13 | 14E-09 | 2.082E-09 | 2.094E-09 |
| 14 | 15E-09 | 2.185E-09 | 2.241E-09 |
| 15 | 20E-09 | 2.601E-09 | 2.874E-09 |
| 16 | 25E-09 | 3.3E-09 | 3.323E-09 |
| 17 | 30E-09 | 3.7E-09 | 3.971E-09 |
| 18 | 35E-09 | 4.4E-09 | 4.579E-09 |
| 19 | 40E-09 | 4.9E-09 | 5.17E-09 |
| 20 | 45E-09 | 5.67E-09 | 5.809E-09 |
| 21 | 50E-09 | 6.09E-09 | 6.45E-09 |

**Table 4.15 Performance of T3**

| *Load Capacitance = 1pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.6E-09 | 0.6522E-09 |
| 2 | 3E-09 | 0.75E-09 | 0.7624E-09 |
| 3 | 4E-09 | 0.9E-09 | 0.910E-09 |
| 4 | 5E-09 | 1.0E-09 | 1.14E-09 |
| 5 | 6E-09 | 1.3E-09 | 1.30E-09 |
| 6 | 7E-09 | 1.34E-09 | 1.479E-09 |
| 7 | 8E-09 | 1.54E-09 | 1.601E-09 |
| 8 | 9E-09 | 1.62E-09 | 1.702E-09 |
| 9 | 10E-09 | 1.7E-09 | 1.841E-09 |
| 10 | 11E-09 | 1.84E-09 | 2.027E-09 |
| 11 | 12E-09 | 2.02E-09 | 2.125E-09 |
| 12 | 13E-09 | 2.21E-09 | 2.243E-09 |
| 13 | 14E-09 | 2.46E-09 | 2.376E-09 |
| 14 | 15E-09 | 2.54E-09 | 2.487E-09 |
| 15 | 20E-09 | 3.0E-09 | 3.072E-09 |
| 16 | 25E-09 | 3.6E-09 | 3.685E-09 |
| 17 | 30E-09 | 4.1E-09 | 4.28E-09 |
| 18 | 35E-09 | 4.7E-09 | 4.88E-09 |
| 19 | 40E-09 | 5.4E-09 | 5.48E-09 |
| 20 | 45E-09 | 5.83E-09 | 6.093E-09 |
| 21 | 50E-09 | 6.25E-09 | 6.693E-09 |

**Table 4.16 Performance of T3**

| *Load capacitance 9pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.9E-09 | 0.986E-09 |
| 2 | 3E-09 | 1.25E-09 | 1.38E-09 |
| 3 | 4E-09 | 1.44E-09 | 1.57E-09 |
| 4 | 5E-09 | 1.6E-09 | 1.74E-09 |
| 5 | 6E-09 | 1.8E-09 | 1.89E-09 |
| 6 | 7E-09 | 2.01E-09 | 2.03E-09 |
| 7 | 8E-09 | 2.21E-09 | 2.11E-09 |
| 8 | 9E-09 | 2.36E-09 | 2.28E-09 |
| 9 | 10E-09 | 2.5E-09 | 2.83E-09 |
| 10 | 11E-09 | 2.72E-09 | 2.95E-09 |
| 11 | 12E-09 | 2.93E-09 | 3.06E-09 |
| 12 | 13E-09 | 3.12E-09 | 3.2E-09 |
| 13 | 14E-09 | 3.31E-09 | 3.4E-09 |
| 14 | 15E-09 | 3.6E-09 | 3.92E-09 |
| 15 | 20E-09 | 4.0E-09 | 4.25E-09 |
| 16 | 25E-09 | 4.6E-09 | 4.88E-09 |
| 17 | 30E-09 | 5.4E-09 | 5.67E-09 |
| 18 | 35E-09 | 6.1E-09 | 6.42E-09 |
| 19 | 40E-09 | 6.9E-09 | 7.3E-09 |
| 20 | 45E-09 | 7.5E-09 | 7.89E-09 |
| 21 | 50E-09 | 7.99E-09 | 8.56E-09 |

Above given were four different tables confirming the results of T3. The actual simulation was carried for various different conditions of capacitive load but only few are shown above.

Since all the required parameters T1, T2, T3 are being calculated now as per the definition of delay i.e( Td = T3 - T1) we now proceed towards the calculation of Td.

The following table gives the final value of the delay in the circuit

**Table 4.17 Performance of Td**

| *Load Capacitance = 0.1pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results (Td) in second | Model results (Td) in second |
| 1 | 2E-09 | 0.037E-09 | 0.04E-09 |
| 2 | 3E-09 | 0.04E-09 | 0.04E-09 |
| 3 | 4E-09 | 0.038E-09 | 0.03E-09 |
| 4 | 5E-09 | 0.038E-09 | 0.04E-09 |
| 5 | 6E-09 | 0.038E-09 | 0.038E-09 |
| 6 | 7E-09 | 0.038E-09 | 0.042E-09 |
| 7 | 8E-09 | 0.039E-09 | 0.045E-09 |
| 8 | 9E-09 | 0.052E-09 | 0.056E-09 |
| 9 | 10E-09 | 0.3E-09 | 0.3E-09 |
| 10 | 11E-09 | 0.32E-09 | 0.3E-09 |
| 11 | 12E-09 | 0.33E-09 | 0.3E-09 |
| 12 | 13E-09 | 0.3E-09 | 0.3E-09 |
| 13 | 14E-09 | 0.3E-09 | 0.3E-09 |
| 14 | 15E-09 | 0.3E-09 | 0.32E-09 |
| 15 | 20E-09 | 0.3E-09 | 0.32E-09 |
| 16 | 25E-09 | 0.48E-09 | -0.5E-09 |
| 17 | 30E-09 | 0.73E-09 | -0.7E-09 |
| 18 | 35E-09 | 0.81E-09 | -0.8E-09 |
| 19 | 40E-09 | 0.88E-09 | -0.9E-09 |
| 20 | 45E-09 | 0.93E-09 | -1.0E-09 |
| 21 | 50E-09 | 1.07E-09 | -1.1E-09 |

**Subthreshold Conduction:**

After observing the above Table 4.17 it is seen that, for high rise time and low capacitive load the model results are negative. The main reason for such a result is the operation of the n-device in subthreshold region. Hence the assumption of the transistor conducting at t=T1 when the gate voltage to the n-device reaches the threshold voltage is no more valid. So for lower capacitive load and higher rise time the subthreshold current should be considered.

When gate voltage is below threshold voltage and the semiconductor is in weak inversion, the corresponding drain current is called subthreshold current. The subthreshold region is particularly important for low voltage, low power applications. In weak inversion, the drain current is dominated by the carrier diffusion and is an exponential function of terminal voltage, similar to the current in the bipolar transistor. The threshold voltages, Vtn, is commonly taken to be the gate to source voltages at which surface minority carrier concentration at the source is equal to the bulk impurity concentration, this is called strong inversion, the drain current, however does not decreases immediately to zero for $Vgs \leq Vtn$, so that Vtn does not define an adequate of threshold.

=An alternative definition is the weak inversion criterion, which is the gate to source voltage, Voff, at which the surface minority carrier density at the source is just equal to the intrinsic carrier concentration, ni, some models describing the subthreshold conduction assume that the channel current is essentially zero for$Vgs \leq Voff$ and the subthreshold characteristics are modeled for$Voff \leq Vgs \leq Von$ where Von is defined to be some voltage such that$Von \leq Vtn$.

For long channel devices, the subthreshold current is independent of the drain voltage for$Vds \geq 4Vtn$, since the surface potential is constant over the entire length of the channel. For short channel devices the surface potential exhibits a localized potential barrier. The height of this barrier is reduced by increasing the

drain voltage and the position of the peak shifts closer to the source region, therefore the subthreshold current depends on the drain voltage for a larger Vds range.

**Table 4.18 Performance of Td**

| *Load capacitance 0.5pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results (Td) in second | Model results (Td) in second |
| 1 | 2E-09 | 0.28E-09 | 0.26E-09 |
| 2 | 3E-09 | 0.31E-09 | 0.3E-09 |
| 3 | 4E-09 | 0.31E-09 | 0.3E-09 |
| 4 | 5E-09 | 0.33E-09 | 0.3E-09 |
| 5 | 6E-09 | 0.35E-09 | 0.35E-09 |
| 6 | 7E-09 | 0.4E-09 | 0.38E-09 |
| 7 | 8E-09 | 0.4E-09 | 0.395E-09 |
| 8 | 9E-09 | 0.4E-09 | 0.41E-09 |
| 9 | 10E-09 | 0.4E-09 | 0.42E-09 |
| 10 | 11E-09 | 0.4E-09 | 0.43E-09 |
| 11 | 12E-09 | 0.4E-09 | 0.43E-09 |
| 12 | 13E-09 | 0.42E-09 | 0.43E-09 |
| 13 | 14E-09 | 0.43E-09 | 0.44E-09 |
| 14 | 15E-09 | 0.43E-09 | 0.44E-09 |
| 15 | 20E-09 | 0.4E-09 | 0.44E-09 |
| 16 | 25E-09 | 0.4E-09 | 0.45E-09 |
| 17 | 30E-09 | 0.4E-09 | 0.45E-09 |
| 18 | 35E-09 | 0.42E-09 | 0.46E-09 |
| 19 | 40E-09 | 0.42E-09 | 0.48E-09 |
| 20 | 45E-09 | 0.5E-09 | 0.5E-09 |
| 21 | 50E-09 | 0.51E-09 | 0.54E-09 |

**Table 4.19 Performance of Td**

| *Load capacitance 1pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results in second | Model results in second |
| 1 | 2E-09 | 0.4E-09 | 0.43E-09 |
| 2 | 3E-09 | 0.4E-09 | 0.4332E-09 |
| 3 | 4E-09 | 0.4E-09 | 0.4373E-09 |
| 4 | 5E-09 | 0.5E-09 | 0.539E-09 |
| 5 | 6E-09 | 0.56E-09 | 0.604E-09 |
| 6 | 7E-09 | 0.59E-09 | 0.653E-09 |
| 7 | 8E-09 | 0.62E-09 | 0.661E-09 |
| 8 | 9E-09 | 0.67E-09 | 0.69E-09 |
| 9 | 10E-09 | 0.7E-09 | 0.727E-09 |
| 10 | 11E-09 | 0.7E-09 | 0.73E-09 |
| 11 | 12E-09 | 0.7E-09 | 0.732E-09 |
| 12 | 13E-09 | 0.7E-09 | 0.735E-09 |
| 13 | 14E-09 | 0.7E-09 | 0.73E-09 |
| 14 | 15E-09 | 0.7E-09 | 0.73E-09 |
| 15 | 20E-09 | 0.7E-09 | 0.73E-09 |
| 16 | 25E-09 | 0.71E-09 | 0.741E-09 |
| 17 | 30E-09 | 0.72E-09 | 0.743E-09 |
| 18 | 35E-09 | 0.72E-09 | 0.745E-09 |
| 19 | 40E-09 | 0.72E-09 | 0.76E-09 |
| 20 | 45E-09 | 0.73E-09 | 0.779E-09 |
| 21 | 50E-09 | 0.75E-09 | 0.8E-09 |

**Table 4.20 Performance of Td**

| *Load capacitance 3pf* | | | |
|---|---|---|---|
| Obs No | Rise time in second | Simulation results (Td) in second | Model results (Td) in second |
| 1 | 2E-09 | 0.7E-09 | 0.750E-09 |
| 2 | 3E-09 | 0.9E-09 | 1.0E-09 |
| 3 | 4E-09 | 1.0E-09 | 1.06E-09 |
| 4 | 5E-09 | 1.1E-09 | 1.14E-09 |
| 5 | 6E-09 | 1.18E-09 | 1.23E-09 |
| 6 | 7E-09 | 1.23E-09 | 1.35E-09 |
| 7 | 8E-09 | 1.27E-09 | 1.42E-09 |
| 8 | 9E-09 | 1.36E-09 | 1.5E-09 |
| 9 | 10E-09 | 1.5E-09 | 1.61E-09 |
| 10 | 11E-09 | 1.55E-09 | 1.67E-09 |
| 11 | 12E-09 | 1.6E-09 | 1.71E-09 |
| 12 | 13E-09 | 1.6E-09 | 1.82E-09 |
| 13 | 14E-09 | 1.65E-09 | 1.84E-09 |
| 14 | 15E-09 | 1.7E-09 | 1.86E-09 |
| 15 | 20E-09 | 1.7E-09 | 1.92E-09 |
| 16 | 25E-09 | 1.7E-09 | 1.95E-09 |
| 17 | 30E-09 | 2.0E-09 | 2.0E-09 |
| 18 | 35E-09 | 2.0E-09 | 2.2E-09 |
| 19 | 40E-09 | 2.3E-09 | 2.43E-09 |
| 20 | 45E-09 | 2.38E-09 | 2.47E-09 |
| 21 | 50E-09 | 2.49E-09 | 2.6E-09 |

The following table gives the percentage error of the developed model as compared to the SPICE results. In turn it depicts the accuracy of the approach followed.

**Table 4.21 % Error in model**

| *Load capacitance 0.1pf* | | |
|---|---|---|
| Obs No | Rise time in second | Error in the model in percentage |
| 1 | 2E-09 | 8.1 |
| 2 | 3E-09 | 0.0 |
| 3 | 4E-09 | 7.2 |
| 4 | 5E-09 | 5.2 |
| 5 | 6E-09 | 0.0 |
| 6 | 7E-09 | 9.0 |
| 7 | 8E-09 | 15.0 |
| 8 | 9E-09 | 7.0 |
| 9 | 10E-09 | 0.0 |
| 10 | 11E-09 | 6.0 |
| 11 | 12E-09 | 9.0 |
| 12 | 13E-09 | 1.0 |
| 13 | 14E-09 | 0.0 |
| 14 | 15E-09 | 6.6 |
| 15 | 20E-09 | 6.8 |
| 16 | 25E-09 | 4.0 |
| 17 | 30E-09 | 4.1 |
| 18 | 35E-09 | 1.23 |
| 19 | 40E-09 | 2.2 |
| 20 | 45E-09 | 7.56 |
| 21 | 50E-09 | 2.83 |

**Table 4.22 % Erroe in model**

| *Load Capacitance = 0.5pf* | | |
|---|---|---|
| Obs No | Rise time in second | Error in the model in percentage |
| 1 | 2E-09 | 7.14 |
| 2 | 3E-09 | 3.23 |
| 3 | 4E-09 | 3.2 |
| 4 | 5E-09 | 9.0 |
| 5 | 6E-09 | 0.0 |
| 6 | 7E-09 | 5.0 |
| 7 | 8E-09 | 1.25 |
| 8 | 9E-09 | 2.5 |
| 9 | 10E-09 | 5.0 |
| 10 | 11E-09 | 7.5 |
| 11 | 12E-09 | 7.8 |
| 12 | 13E-09 | 2.3 |
| 13 | 14E-09 | 2.34 |
| 14 | 15E-09 | 2.38 |
| 15 | 20E-09 | 10.0 |
| 16 | 25E-09 | 12.5 |
| 17 | 30E-09 | 12.5 |
| 18 | 35E-09 | 9.52 |
| 19 | 40E-09 | 14.2 |
| 20 | 45E-09 | 0.0 |
| 21 | 50E-09 | 5.88 |

Table 4.23 % Error in model

| *Load capacitance 1pf* | | |
|---|---|---|
| Obs No | Rise time in second | Error in the model in percentage |
| 1 | 2E-09 | 5.0 |
| 2 | 3E-09 | 6.25 |
| 3 | 4E-09 | 7.5 |
| 4 | 5E-09 | 8.0 |
| 5 | 6E-09 | 7.1 |
| 6 | 7E-09 | 10.2 |
| 7 | 8E-09 | 6.45 |
| 8 | 9E-09 | 2.98 |
| 9 | 10E-09 | 2.8 |
| 10 | 11E-09 | 2.7 |
| 11 | 12E-09 | 2.7 |
| 12 | 13E-09 | 2.76 |
| 13 | 14E-09 | 2.8 |
| 14 | 15E-09 | 2.9 |
| 15 | 20E-09 | 2.8 |
| 16 | 25E-09 | 2.8 |
| 17 | 30E-09 | 3.4 |
| 18 | 35E-09 | 2.7 |
| 19 | 40E-09 | 5.5 |
| 20 | 45E-09 | 6.8 |
| 21 | 50E-09 | 6.6 |

Table 4.24 % Error in model

| *Load capacitance 3pf* | | |
|---|---|---|
| Obs No | Rise time in second | Error in the model in percentage |
| 1 | 2E-09 | 7.0 |
| 2 | 3E-09 | 11.1 |
| 3 | 4E-09 | 6.0 |
| 4 | 5E-09 | 3.6 |
| 5 | 6E-09 | 4.2 |
| 6 | 7E-09 | 9.7 |
| 7 | 8E-09 | 11.8 |
| 8 | 9E-09 | 10.29 |
| 9 | 10E-09 | 7.33 |
| 10 | 11E-09 | 7.71 |
| 11 | 12E-09 | 6.82 |
| 12 | 13E-09 | 13.75 |
| 13 | 14E-09 | 11.5 |
| 14 | 15E-09 | 9.4 |
| 15 | 20E-09 | 12.9 |
| 16 | 25E-09 | 10.2 |
| 17 | 30E-09 | 0.0 |
| 18 | 35E-09 | 10.1 |
| 19 | 40E-09 | 5.6 |
| 20 | 45E-09 | 3.78 |
| 21 | 50E-09 | 4.41 |

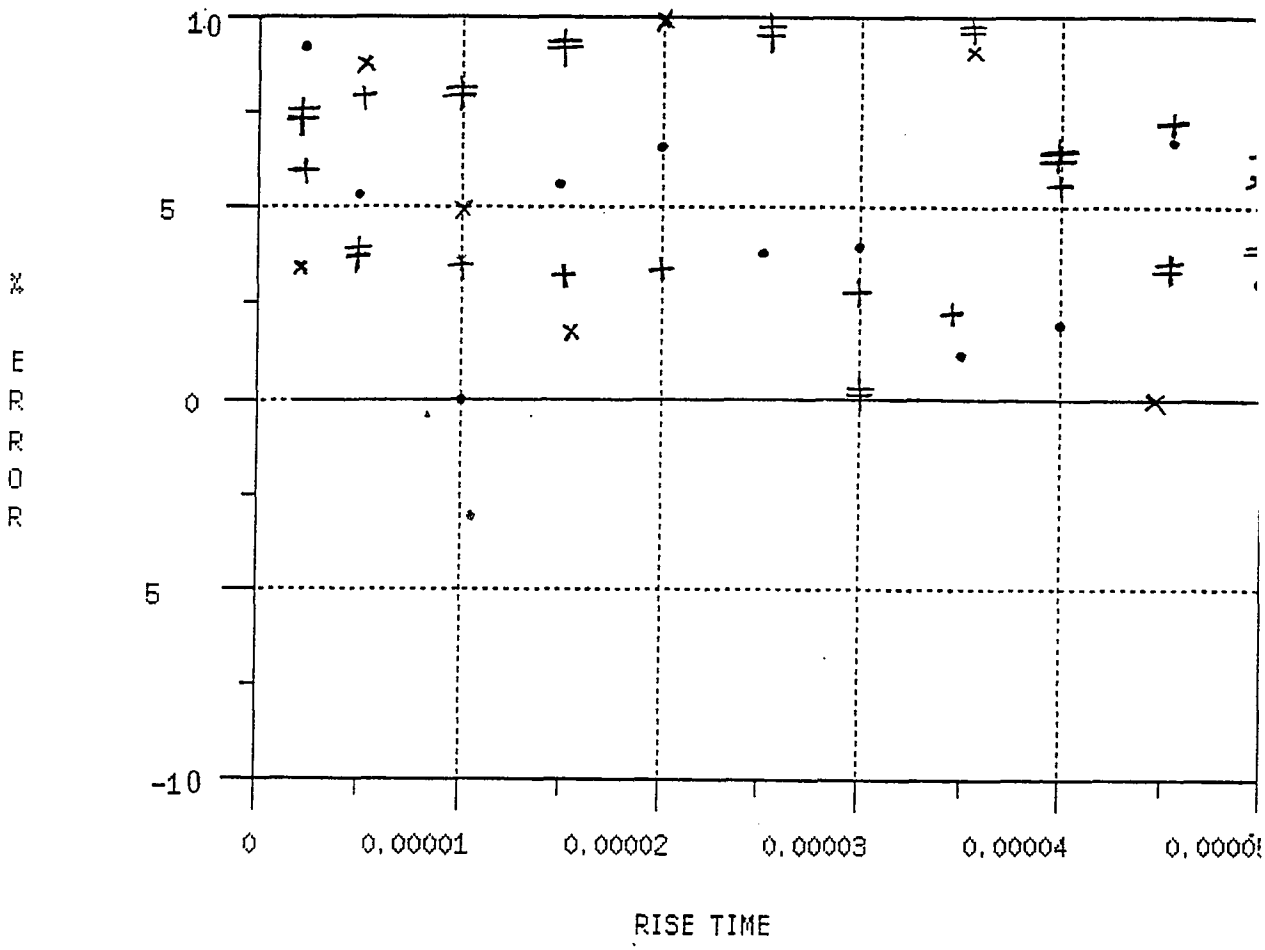


Figure 4.5: Error of the model as compared to the SPICE results

# Chapter 5

# CONCLUSION

After carefully analyzing the entire work it is concluded that the main objective of developing a timing model with the best possible accuracy is very well achieved. The reasons for slight variation that occured, will be discussed in subsequent sections.

The timing models based on Linear RC approach, to calculate the delay of the circuit has an error in estimation ranging from 30% to 40%. The timing model developed on the charge conservation principle has an error in calculating the delay ranging from 2% to 8% (slightly over 8% in few cases). This accuracy of the developed model was confirmed after large simulation runs, and for various different conditions i.e for load capacitance ranging from, 0.1pf to 10pf and for various rise-time

The model presented provides designers with higher accuracy than the over simplified model presented in previous works. Nevertheless, some inaccuracy is still present. More precisely, the inaccuracy is directly proportional to the output load

and inversely proportional to the input signal rise time. Medium values of load resistance combined with short input rise-time or larger values of load resistance combined with longer rise-times, will make this situation happen.

The fact that the model is slightly deviating from required performance because, equating the load current to the n-channel transistor current that is, for an output low going transition is no longer valid and the current of p-channel device is also to be considered to get the desired accuracy.

The following observations were made which may result in increasing the accuracy. The decrease in the accuracy of the model starts, when the time in which the n-channel transistor stays in the saturation region becomes larger than the rise time of the input signal. In other words, as long as the saturation period is shorter than the rise-time of the signal, model accurately tracks the output waveform computed by SPICE. The longer the saturation time with respect to input rise-time, less accurate is the model.

The another important point that was observed was the behavior of the modeled circuit for low capacitive load and high rise time. Taking a specific case of fall time delay estimation, it was seen that for low capacitive load the charge stored in the capacitor discharges very fast. However, as the time taken by the input voltage to rise to Vtn to make the device fully conducting is relatively longer. So if we proceed with the numerical equations given above, it shall give negative value of delay. Hence for such cases the subthreshold current has to be considered, since the n-device starts conducting before the threshold voltage is reached in subthreshold region.

The accuracy of any timing model depends on the inclusion of several factors. These include input waveform slopes, transistor model parameters, device capacitances, parasitic, overlapping inputs, waveform voltage levels, process gain

factor, transistor gain factor and transistor configurations within subcircuits. All of these issues must be addressed in order to obtain the accuracy which is required by designers.

The model presented takes into consideration most of the factors, due to which the results are very close to the desired ones. However for increasing the accuracy the transistors period of conduction in saturation region should be very thoroughly studied, which can help in improving the performance further.

It is further analyzed that the timing delay is high dimensional and nonlinear function of the fore-mentioned parameters and is difficult to be represented by a simple delay model directly in terms of these parameters.

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# Appendix A:

These are the SPICE input file, for various capacitive load.

```
c* CMOS INVERTER
* INPUT LISTING OF PARAMETERS
VDD 1 0 5V
VIN 3 0  PULSE (0 5 0NS 10NS 0NS 50NS 200NS)
* (0 5 10NS 50NS 20NS 100NS 200NS)
V1 6 4 0V
V2 4 5 0V
V3 4 7 0V
MN1 6 3 1 1 MOD1 W=3U L=3U
MN2 5 3 0 0 MOD2 W=3U L=3U
CL 7 0 0.5E-12
.MODEL MOD2 NMOS LEVEL=2 LD=.280000U TOX=520.00E-10 VTO=.587229 KP=3.848
+050E-05 GAMMA=.922197 PHI=.600000 UO=200.00 UEXP=1.001000E-03 UCRIT=999
+000 DELTA 1.59123 VMAX=100000 XJ=.400000U LAMBDA=2.208002E-02 NFS=5.033532E+11
+ NEFF=1.001000E+11 TPG=1.000 RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4
+ MJ=0.5 CJSW=6.0E-10 MJSW=.33 NSUB=4.575777E+15
.MODEL MOD1 PMOS LEVEL=2 LD=.2800000U  TOX=520.00E-10 NSUB=2.534947E+14
+ VTO=-.78405 KP=1.394594E-05 GAMMA=.536443 PHI=.6 UO=100.0 UEXP=.171475
+ UCRIT=51857.9 DELTA=1.89818 VMAX=100000 XJ=.4U LAMBDA=4.720123E-02
+ NFS=8.870574E+11 NEFF=1.001000E-02 NSS=0.00000E+00 TPG=-1.0000 RSH=55
+ CGSO=4.0E-10 CGDO=4.0E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33
.TRAN .1NS 100NS 0NS
.OPTION LIMPTS=100000
.PRINT TRANS I(V1) I(V2) I(V3) V(3) V(7)
.PLOT TRANS I(V2) V(3) V(7)
.WIDTH OUT=80
.END
```

```
c* CMOS INVERTER
* INPUT LISTING OF PARAMETERS
VDD 1 0 5V
VIN 3 0  PULSE (0 5 0NS 10NS 0NS 50NS 200NS)
* (0 5 10NS 50NS 20NS 100NS 200NS)
V1 6 4 0V
V2 4 5 0V
V3 4 7 0V
MN1 6 3 1 1 MOD1 W=3U L=3U
MN2 5 3 0 0 MOD2 W=3U L=3U
CL 7 0 3.0E-12
.MODEL MOD2 NMOS LEVEL=2 LD=.280000U TOX=520.00E-10 VTO=.587229 KP=3.848
+050E-05 GAMMA=.922197 PHI=.600000 UO=200.00 UEXP=1.001000E-03 UCRIT=999
+000 DELTA 1.59123 VMAX=100000 XJ=.400000U LAMBDA=2.208002E-02 NFS=5.033532E+11
+ NEFF=1.001000E+11 TPG=1.000 RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4
+ MJ=0.5 CJSW=6.0E-10 MJSW=.33 NSUB=4.575777E+15
.MODEL MOD1 PMOS LEVEL=2 LD=.2800000U  TOX=520.00E-10 NSUB=2.534947E+14
+ VTO=-.78405 KP=1.394594E-05 GAMMA=.536443 PHI=.6 UO=100.0 UEXP=.171475
+ UCRIT=51857.9 DELTA=1.89818 VMAX=100000 XJ=.4U LAMBDA=4.720123E-02
+ NFS=8.870574E+11 NEFF=1.001000E-02 NSS=0.00000E+00 TPG=-1.0000 RSH=55
+ CGSO=4.0E-10 CGDO=4.0E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33
.TRAN .1NS 100NS 0NS
.OPTION LIMPTS=100000
.PRINT TRANS I(V1) I(V2) I(V3) V(3) V(7)
.PLOT TRANS I(V2) V(3) V(7)
.WIDTH OUT=80
.END
```

```
c* CMOS INVERTER
* INPUT LISTING OF PARAMETERS
VDD 1 0 5V
VIN 3 0  PULSE (0 5 0NS 10NS 0NS 50NS 200NS)
* (0 5 10NS 50NS 20NS 100NS 200NS)
V1 6 4 0V
V2 4 5 0V
V3 4 7 0V
MN1 6 3 1 1 MOD1 W=3U L=3U
MN2 5 3 0 0 MOD2 W=3U L=3U
CL 7 0 1.0E-12
.MODEL MOD2 NMOS LEVEL=2 LD=.280000U TOX=520.00E-10 VTO=.587229 KP=3.848
+050E-05 GAMMA=.922197 PHI=.600000 UO=200.00 UEXP=1.001000E-03 UCRIT=999
+000 DELTA 1.59123 VMAX=100000 XJ=.400000U LAMBDA=2.208002E-02 NFS=5.033532E+1
+ NEFF=1.001000E+11 TPG=1.000 RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4
+ MJ=0.5 CJSW=6.0E-10 MJSW=.33 NSUB=4.575777E+15
.MODEL MOD1 PMOS LEVEL=2 LD=.2800000U  TOX=520.00E-10 NSUB=2.534947E+14
+ VTO=-.78405 KP=1.394594E-05 GAMMA=.536443 PHI=.6 UO=100.0 UEXP=.171475
+ UCRIT=51857.9 DELTA=1.89818 VMAX=100000 XJ=.4U LAMBDA=4.720123E-02
+ NFS=8.870574E+11 NEFF=1.001000E-02 NSS=0.00000E+00 TPG=-1.0000 RSH=55
+ CGSO=4.0E-10 CGDO=4.0E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33
.TRAN .1NS 100NS 0NS
.OPTION LIMPTS=100000
.PRINT TRANS I(V1) I(V2) I(V3) V(3) V(7)
.PLOT TRANS I(V2) V(3) V(7)
.WIDTH OUT=80
.END
```

```
c* CMOS INVERTER
* INPUT LISTING OF PARAMETERS
VDD 1 0 5V
VIN 3 0  PULSE (0 5 0NS 10NS 0NS 50NS 200NS)
* (0 5 10NS 50NS 20NS 100NS 200NS)
V1 6 4 0V
V2 4 5 0V
V3 4 7 0V
MN1 6 3 1 1 MOD1 W=3U L=3U
MN2 5 3 0 0 MOD2 W=3U L=3U
CL 7 0 7.0E-12
.MODEL MOD2 NMOS LEVEL=2 LD=.280000U TOX=520.00E-10 VTO=.587229 KP=3.848
+050E-05 GAMMA=.922197 PHI=.600000 UO=200.00 UEXP=1.001000E-03 UCRIT=999
+000 DELTA 1.59123 VMAX=100000 XJ=.400000U LAMBDA=2.208002E-02 NFS=5.033532E+11
+ NEFF=1.001000E+11 TPG=1.000 RSH=20 CGSO=5.2E-10 CGDO=5.2E-10 CJ=4.5E-4
+ MJ=0.5 CJSW=6.0E-10 MJSW=.33 NSUB=4.575777E+15
.MODEL MOD1 PMOS LEVEL=2 LD=.2800000U  TOX=520.00E-10 NSUB=2.534947E+14
+ VTO=-.78405 KP=1.394594E-05 GAMMA=.536443 PHI=.6 UO=100.0 UEXP=.171475
+ UCRIT=51857.9 DELTA=1.89818 VMAX=100000 XJ=.4U LAMBDA=4.720123E-02
+ NFS=8.870574E+11 NEFF=1.001000E-02 NSS=0.00000E+00 TPG=-1.0000 RSH=55
+ CGSO=4.0E-10 CGDO=4.0E-10 CJ=3.6E-4 MJ=0.5 CJSW=6.0E-10 MJSW=0.33
.TRAN .1NS 100NS 0NS
.OPTION LIMPTS=100000
.PRINT TRANS I(V1) I(V2) I(V3) V(3) V(7)
.PLOT TRANS I(V2) V(3) V(7)
.WIDTH OUT=80
.END
```

# Appendix:B

The calculation of the transistor delay is explained in detail in chapter 3 and chapter 4. During the delay calculations their were various terms that were introduced but not discussed in details, such as $R_l$, $N_3$, $N_4$. These terms are used in various stages of delay calculation. This subsequent sections gives an enitre review of these terms, its applicabilty and use.

The value of the function $R_l$ used in Equation 3.29 is calculated as follows

$$R_l = \frac{L}{W \mu C_{ox} V_{dd}}$$

where

L is the length of the transistor

W is the width of the transistor

$C_{ox}$ is the oxide capacitance and

$\mu$ is the mobility of the n-channel device.

Then proceeding further towards Equation 3.24 and Equation 3.46 it is seen that, there are two ways to handle Equations 3.24 and Equation 3.46 the first method is the Newton Raphson method and the other is the approximation method. The Newton Raphson method can be summarized, as Equation 3.24 can be rewritten as.

If a function $f(x)$ is given as follows

$f(x) = ax^4 + bx^3 + cx^2 + dx + e$

We first take the derivative of the function $f(x)$ called $f'(x)$ and then divide the original function by the derivate of that function and subtract the result from the initial expected value.

It can be described as follows,

$x'(t) = x(t) - \frac{f(x)}{f'(x)}$

where $x(t)$ is the initial expected value and $x'(t)$ is the first iterated value, then we treat the obtained value $x'(t)$ as the expected value and do the second iteration to obtain the second expected value.

The equation shall look like the following one,

$x''(t) = x'(t) - \frac{f(x')}{f'(x')}$

where $x''(t)$ is the expected value after second iteration, and $x'(t)$ is the expected value after the first iteration.

After a large number of iterations it gives the final expected value, hence in Newton Raphson method an initial expected value has to be obtained to get the final value, so if the initial expected value is far away from the expected value it shall take tremendous computational time to come to the final answer.

Generally speaking, it is difficult to predict a reasonable initial value for the Newton Raphson iteration method. As a result, computation time using the Newton Raphson method may be unacceptably long, limiting practical use of our model.

As an alternative, an approximation method is sought to be more practical. Large number of simulation results show that the first and the third terms in Equation 3.24 are very small. They have a negligible effect on final result of T2. Therefore we decided to eliminate these two terms in the Equation 3.24.

To improve the accuracy of the simplified equation, a rise-time dependent parameter $N_3$ was introduced.

$$N_3 = \frac{-11}{48ns}(t_{rise} - 2ns) + 12.5$$

This equation is obtained through a large amount of simulations and calculations. Figure B.1 shows the results of $N_3$ versus rise-time.

Similarly another parameter $N_4$ was introduced for Equation 3.46 after a large number of simulation runs.

$$N_4 = \frac{-2.5}{48ns}(t_{rise} - 2ns) + 5.5$$

Figure B.2 shows the results of $N_4$ versus rise-time.