Investigations of gate turn-off structures

Hans Werner Becke
New Jersey Institute of Technology

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INVESTIGATIONS OF
GATE TURN-OFF STRUCTURES

by

Hans Werner Becke

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Dissertation submitted to the Faculty of the Graduate School of the New Jersey Institute of Technology in partial fulfillment of the requirement for the degree of

Doctor of Engineering Science

1981
Title of Thesis: Investigation of Gate Turn-Off Structures

Name of Candidate: Hans Werner Becke
Doctor of Engineering Science, 1981

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Dr. R. P. Misra
Professor of Electrical Engrg.
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Degree to be Conferred: D. Eng. Sc., 1981

Mr. Becke holds a B.S. degree in EE from the Ohm-Polytechnical Institute, Nuremberg, Germany (1953). He received the MSEE degree from New Jersey Institute of Technology (1966) and has completed his dissertation for a D.Eng.Sc. in Electrical Engineering at the same institute (1981).

Mr. Becke has over 20 years of experience in the semiconductor field. The major portion of his career he spent with RCA Corp. From 1961 to 1967 he worked mainly on GaAs devices, such as bipolar power transistors, IR diodes and semiconductor lasers. He is credited with the development of the first GaAs insulated gate-field effect transistor.

From 1967 on, Mr. Becke was engaged in development of silicon technology for high power transistor structures and dielectrically isolated IC's. Noteworthy are his contributions in the area of gate turn-off thyristors directed toward achievement of safe turn-off and high performance, and in the development of power MOS FETS.

In 1980, Mr. Becke joined the High Voltage IC Department of Bell Labs, where he is currently designing high voltage dielectrically isolated devices.

Mr. Becke holds 11 patents and has published 16 papers dealing with semiconductor topics.1

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1 A list of Publications and Patents is included at the end of this thesis, following the bibliography.
ABSTRACT

Research and Development was done on gate turn-off devices. The aim was i) to improve turn-off capability without compromise of turn-on, on-state, and useful temperature range, ii) to implement "safe" turn-off.

A) The dependence of the electrical device characteristics on cathode width for an optimized vertical structure was determined. Fall times of 100 to 200 nsec and risetimes of <400 nsec were simultaneously obtained for average current densities of 53 A/cm² @ T_j = 125°C. From spreading resistance analysis the fast t_r and t_f response is shown to be a consequence of proper Au-distribution in the active device volume.

From transient analysis it is concluded that for safe turn-off d²i_A/dt² should never become positive during the fall phase, and that the differential turn-off gain should remain less than unity during the tail period. These requirements are realized by means of a voltage source with a series inductance as gate input for turn-off. As a result
a switching capability of 1.56kW (resistive load) @ 75°C case temperature at 50kHz and with 97% device efficiency is obtained for a chip of 0.15cm².

B) Anode shorts for improvement of turn-off without the necessity of excessive lifetime reduction were also investigated. These shorts substantially reduce the turn-on sensitivity.

A Schottky barrier in series with the non-regenerative region, which parallels the thyristor section, restored the turn-on sensitivity at low temperatures while retaining the turn-off capability at high temperatures.

For 30A (J = 200 A/cm²) turn-off @ +125°C the gate trigger current was ~10mA and 60mA @ -40°C for devices with Schottky barriers and without Schottky barriers, respectively.

C. The incidence of catastrophic failures due to filamentary burn-out was drastically reduced through introduction of a dynamic ballasting (defocusing) concept. This approach features a resistively ballasted cathode (~7Ω/square) with an insulated
center, i.e., contacted only at the periphery.

Therefore, the formation of small area, high current density filaments is largely inhibited. Using this principle, device operation was extended from -20°C to +125°C for conventional devices, to a range from -60°C for sensitive turn-on \( (I_{gt} = 300\mu A) \) to +150°C for safe turn-off @ \( I_{T \, off(max)} = 8.5A \) \( (J = 55A/cm^2) \) for the ballasted devices.
PREFACE

The search for efficient electronic power switches has gained more and more importance during the last decade. Energy shortage and inflation have made it necessary to look for new technological solutions to provide devices for power conversion equipment that will be both more efficient and at the same time economical.

The Gate-Turn-Off thyristor, though known conceptually since the early 60's, has in the past eluded attempts to make it a practical reality as a viable, useful electronic component.

The experimental work, subject of this thesis, was directed toward identification of the problems with this device, and to gain a better understanding, at least qualitatively, of the turn-off process.

Hopefully, the new concepts introduced to improve device performance have contributed toward advancement of the state-of-the-art. The results, especially those obtained by the application of a Schottky barrier in series with anode shorts and the implementation of the dynamic ballasting principle, are very encouraging. They should provide an incentive for further investigations of GTO-structures and eventually lead to a complete understanding of phenomena related to this device, such that from a theoretical basis device performance and limitations can be predicted.
I appreciate the help provided by Professor R. P. Misra of NJIT as my Thesis Advisor. I am also greatly indebted to Dr. M. H. Zambuto for the help and encouragement received over the years of my graduate studies, the doctoral program. My thanks also to Dr. K. S. Sohn and Dr. M. Natapoff for taking the time to critically read this dissertation.

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I acknowledge the great value of discussions related to this work I had with many of my colleagues, especially to Messrs. J. M. Neilson, K. P. Smith, R. Amantea, and R. Martinelli I extend my gratitude.

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Last but not least, I thank Mrs. R. Lepree for the fast and flawless typing of this manuscript.
To Friedl and Hans-Dieter
<table>
<thead>
<tr>
<th>Chapter</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>PREFACE</td>
<td>ii</td>
</tr>
<tr>
<td>I. INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>A. Thyristors and Transistors as Electronic Switches</td>
<td>1</td>
</tr>
<tr>
<td>B. The Gate Turn-Off Thyristor (GTO)</td>
<td>3</td>
</tr>
<tr>
<td>1. Simple, First Order Observations</td>
<td>3</td>
</tr>
<tr>
<td>2. Qualitative, Two-Dimensional Considerations</td>
<td>6</td>
</tr>
<tr>
<td>3. A Double Gate Layer, Shorted Anode GTO</td>
<td>9</td>
</tr>
<tr>
<td>4. Interdigitation, Series Schottky Barrier, and Dynamic Ballasting</td>
<td>11</td>
</tr>
<tr>
<td>II. THEORY OF GATE TURN-OFF IN FOUR LAYER DEVICES</td>
<td>14</td>
</tr>
<tr>
<td>A. A Two-Dimensional, Analytical Model</td>
<td>14</td>
</tr>
<tr>
<td>1. The Turn-Off Velocity</td>
<td>16</td>
</tr>
<tr>
<td>2. The Storage Time and Maximum Turn-Off Gain</td>
<td>24</td>
</tr>
<tr>
<td>3. The Lateral Base Resistance and Maximum Turn-Off Anode Current</td>
<td>25</td>
</tr>
<tr>
<td>4. The Fall Time</td>
<td>27</td>
</tr>
<tr>
<td>B. A Two-Section, Charge Control Model</td>
<td>29</td>
</tr>
<tr>
<td>1. The Charge Control Concept</td>
<td>29</td>
</tr>
<tr>
<td>2. The Junction Voltages</td>
<td>30</td>
</tr>
<tr>
<td>3. The Current Loop Equations</td>
<td>32</td>
</tr>
<tr>
<td>4. The Computation Method</td>
<td>36</td>
</tr>
<tr>
<td>5. Base Charges and Currents During Turn-Off</td>
<td>37</td>
</tr>
</tbody>
</table>
III. A HIGH SPEED, HIGH VOLTAGE EPI-BASE STRUCTURE .......... 41
   A. Motivation .................................................. 41
   B. Choice of Vertical Structure ............................. 46
      1. Gate Sheet Resistance ................................. 47
      2. Minority Carrier Lifetime ............................... 51
   C. Choice of Horizontal Geometry (Interdigitation) .... 53
   D. Process for Device Fabrication ......................... 55
   E. Results ...................................................... 59
      1. Static Data ............................................... 61
      2. Major Test Conditions .................................. 63
      3. Turn-On .................................................... 63
      4. Turn-Off Characteristics (General Waveforms) .... 66
      5. Influence of the Gate Series Inductance .......... 69
      6. Dependence on Cathode Width ......................... 73
      7. Turn-Off Criteria and Current Densities .......... 75
      8. Influence of Negative Gate Bias and Temperature 79
      9. Turn-Off For Varying Loads ............................ 82
     10. Switching Performance ................................ 85
     11. Gold Distribution and Life Time ..................... 92
     12. Power Switching Capabilities ....................... 96
IV. SERIES SCHOTTKY BARRIERS AND DYNAMIC BALLASTING .......................... 101
   
   A. Anode Shorts and Schottky Barriers ........................................ 101
       1. Device Structure and Geometry ........................................... 101
       2. Turn-On With and Without Schottky Barriers .......................... 106
       3. Turn-On Sensitivity and Turn-Off Capability ......................... 109
   
   B. Dynamic Ballasting (Defocusing) ............................................ 112
       1. Defocusing Principle and Device Structure ............................ 114
       2. Turn-Off With and Without Dynamic Ballasting ....................... 116
       3. Summary of Results ............................................................ 120

V. CONCLUSION .................................................................................. 124
   
   A. High Speed-High Voltage Gate Turn-Off Device ............................ 124
   B. Anode Shorts and Schottky Barriers ......................................... 125
   C. Dynamic Ballasting (Defocusing) ............................................. 125

APPENDIX A. COMPUTER PROGRAM FOR PHOTO MASK SET GENERATION .......... 127

APPENDIX B. PHOTO MASK SET FOR 3x3 ARRAY OF GTO DEVICES ................. 145

APPENDIX C. STATIC DATA FOR GTO'S WITH STANDARD CATHODE AND DYNAMICALLY BALLASTED CATHODE .................................................. 153

BIBLIOGRAPHY .................................................................................. 160
<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1</td>
<td>Static Data for GTO Thyristor with Varying Cathode Width</td>
<td>62</td>
</tr>
<tr>
<td>3.2</td>
<td>Peak Current Density for GTO During Turn-Off</td>
<td>93</td>
</tr>
<tr>
<td>3.3</td>
<td>Components of Dissipated Energy/Cycle in μJoules for GTO (Device Type 3)</td>
<td>98</td>
</tr>
<tr>
<td>4.1</td>
<td>Effect of Resistive Cathode and Dynamic Ballasting (Defocusing) on GTO Temperature Behavior</td>
<td>121</td>
</tr>
</tbody>
</table>
## LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-1. GTO Thyristor</td>
<td>4</td>
</tr>
<tr>
<td>1-1a. Schematic Four Layer Structure</td>
<td>4</td>
</tr>
<tr>
<td>1-1b. Composite NPN-PNP Structure</td>
<td>4</td>
</tr>
<tr>
<td>1-1c. Equivalent Transistor Circuit</td>
<td>4</td>
</tr>
<tr>
<td>1-1d. Loop Gain Diagram</td>
<td>4</td>
</tr>
<tr>
<td>1-2. Turn-Off Process in Conventional GTO-Thyristor</td>
<td>8</td>
</tr>
<tr>
<td>1-2a. GTO-Thyristor in &quot;On&quot; State</td>
<td>8</td>
</tr>
<tr>
<td>1-2b. GTO-Thyristor During Turn-Off</td>
<td>8</td>
</tr>
<tr>
<td>1-2c. Lateral Voltage Drop $V_G &gt; V_G br$</td>
<td>8</td>
</tr>
<tr>
<td>1-3. Turn-Off Process in GTO Structure with Low Resistance, High Breakdown Gate Layer</td>
<td>10</td>
</tr>
<tr>
<td>1-3a. GTO-Thyristor with Buffer Area in &quot;On&quot; State</td>
<td>10</td>
</tr>
<tr>
<td>1-3b. GTO-Thyristor with Buffer Area During Turn-Off</td>
<td>10</td>
</tr>
<tr>
<td>2-1. Conditions for Turn-Off of a GTO</td>
<td>15</td>
</tr>
<tr>
<td>2-1a. Schematic Circuit Diagram</td>
<td>15</td>
</tr>
<tr>
<td>2-1b. Input Drive Function</td>
<td>15</td>
</tr>
<tr>
<td>2-1c. Output Response</td>
<td>15</td>
</tr>
<tr>
<td>2-2. Electron-Hole Plasma &quot;Squeezed&quot; Toward Center of Cathode During Turn-Off Process</td>
<td>17</td>
</tr>
<tr>
<td>2-3. Model for Deriving Turn-Off Parameters for a GTO Thyristor (after D. Wolley)</td>
<td>18</td>
</tr>
<tr>
<td>2-3a. Two-Dimensional Arrangement</td>
<td>18</td>
</tr>
<tr>
<td>2-3b. Electron Distribution in Z-Direction</td>
<td>18</td>
</tr>
<tr>
<td>2-3c. Form Function of Electron Distribution in X-Direction</td>
<td>18</td>
</tr>
<tr>
<td>Figure</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>------</td>
</tr>
<tr>
<td>2-4. Storage Time vs. Turn-Off Gain (after D. Wolley)</td>
<td>26</td>
</tr>
<tr>
<td>2-5. Input Current ( I_G ) and Output Current Response ( I_A ) as Function of Time for GTO-Thyristor During Turn-Off</td>
<td>28</td>
</tr>
<tr>
<td>2-6. Thyristor Model for Definition of Charge Control Equation</td>
<td>31</td>
</tr>
<tr>
<td>2-6a. Thyristor Element N</td>
<td>31</td>
</tr>
<tr>
<td>2-6b. Two Transistor Equivalent</td>
<td>31</td>
</tr>
<tr>
<td>2-7. Voltage vs. Charge for Cathode Junction ( J_1 ), or Anode Junction ( J_3 ) (after M. Kurata)</td>
<td>33</td>
</tr>
<tr>
<td>2-8. GTO Two-Section Model (after M. Kurata)</td>
<td>34</td>
</tr>
<tr>
<td>2-9. Equivalent GTO-Thyristor Circuit for Two-Section Model (after M. Kurata) Closing ( S_1 ) Initiates Turn-Off</td>
<td>35</td>
</tr>
<tr>
<td>2-10. Base Charges and Anode Current for Two-Section GTO-Thyristor Model During Turn-Off (After M. Kurata)</td>
<td>39</td>
</tr>
<tr>
<td>2-10a. P-Base Charge and N-Base Charge vs. Time</td>
<td>39</td>
</tr>
<tr>
<td>2-10b. Current Components vs. Time</td>
<td>39</td>
</tr>
<tr>
<td>3-1. Comparison of Power Transistors and Thyristors as an Electronic Switch Showing Power Loss In &quot;On&quot; State</td>
<td>42</td>
</tr>
<tr>
<td>J is Average Collector Current Density and Anode Current Density for Transistors and Thyristors, respectively</td>
<td>42</td>
</tr>
<tr>
<td>3-2. Comparison of Power-Switching Capability with Respect to Cost as a Function of Frequency for Thyristors, GTO's, and Transistors</td>
<td>45</td>
</tr>
<tr>
<td>Figure</td>
<td>Page</td>
</tr>
<tr>
<td>--------------</td>
<td>------</td>
</tr>
<tr>
<td>3-3. Impurity Concentration Profiles for GTO-SCR Structures</td>
<td>48</td>
</tr>
<tr>
<td>3-3a. Graded Base (double diffused)</td>
<td>48</td>
</tr>
<tr>
<td>3-3b. Uniform Base (epitaxial)</td>
<td>48</td>
</tr>
<tr>
<td>3-3c. Inverted Base (epitaxial; ion implanted and diffused)</td>
<td>48</td>
</tr>
<tr>
<td>3-4. Rise Time $t_r$, Fall Time $t_f$, and &quot;On&quot; State Voltage vs. Sheet Resistance of (gated) P-Base</td>
<td>50</td>
</tr>
<tr>
<td>3-5. Rise Time $t_r$, Fall Time $t_f$, and &quot;On&quot; State Voltage vs. Average Lifetime (Au Doping) for GTO Thyristor</td>
<td>52</td>
</tr>
<tr>
<td>3-6. Test Array of GTO-Thyristors Having Varying Cathode Widths Clockwise from Upper Left: Test Pattern (Rectangular Cathode Sites) 1, 2, 3, 4; Device (Tapered Cathode Fingers) 1, 2, 3, 4</td>
<td>54</td>
</tr>
<tr>
<td>Microphotograph of Section of Actual Device Wafer at &quot;Define Cathode Area&quot; Processing Stage (see Figure 3-7, Step 7, and Appendix B, Mask 03)</td>
<td>54</td>
</tr>
<tr>
<td>3-7. Basic Process Outline for Fabrication of High Speed, Epi Base GTO-Thyristor (3 pages)</td>
<td>58</td>
</tr>
<tr>
<td>3-8. Two-Point Probe - Spreading Resistance Profile for High Frequency-Epi Base Structure</td>
<td>60</td>
</tr>
<tr>
<td>3-9. Input-Output Waveforms for GTO Thyristor in Anode Load Configuration</td>
<td>64</td>
</tr>
<tr>
<td>3-10. Turn-On Characteristic of High-Frequency GTO-Thyristor at 25°C and 125°C Device 1, 2, 3, and 4</td>
<td>65</td>
</tr>
<tr>
<td>3-10a. Gate Turn-On Current $I_{GT} = f(t)$ Anode Load Current Response $I_A = f(t)$</td>
<td>65</td>
</tr>
<tr>
<td>3-10b. $[I_{GT}, I_A] = f(t)$</td>
<td>65</td>
</tr>
<tr>
<td>Figure</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>3-11.</td>
<td>Turn-Off Characteristics for High-Frequency GTO-Thyristor (Example of Waveforms)</td>
</tr>
<tr>
<td>3-12.</td>
<td>Turn-Off for GTO-Thyristor ([I_A, I_{gq}] = f(t)) with Gate Series Inductance (L_{gs}) as Parameter Device Type 3 (4-mil Cathode)</td>
</tr>
<tr>
<td>3-13.</td>
<td>Turn-Off Behavior of GTO-Thyristor with varying Cathode Width ([I_A, I_{gq}] = f(t)) (W_k = L_x) as Parameter</td>
</tr>
<tr>
<td>3-14.</td>
<td>Differential Turn-Off Gain ((d\alpha/dI_{gq})) vs. Time for GTO Thyristors having different Cathode Widths under Identical Input and Output Conditions; showing safe Turn-Off for Device Types 2, 3, 4 (2, 4 and 8 mil cathode), and indicating Onset of Turn-Off Failure for Device Type 1 (20 mil Cathode). (V_D = 200) V, (I_T = 8) A, (V_{goc} = -15) V, (L_{gs} = 4.6) (\mu)H, (T = 25)°C (for (I_A, I_{gq} = f(t)), See Figure 3-13</td>
</tr>
<tr>
<td>3-15.</td>
<td>Turn-Off Behavior of GTO-Thyristor for Varying Negative Gate Bias ([I_A, I_{gq}] = f(t), V_{goc}) Parameter Device Type 3 (4-mil Cathode)</td>
</tr>
<tr>
<td>3-16.</td>
<td>Turn-Off for GTO-Thyristor dependent on Temperature ([I_A, I_{gq}] = f(t), T) Parameter Device Type 3 (4-mil Cathode)</td>
</tr>
<tr>
<td>3-17.</td>
<td>Fall Time for GTO-Thyristor as Function of (Open Circuit) Gate-Source Voltage (t_f = f(V_{goc})), (W_k = L_x) as Parameter (2 = ) Device Type 2 (8-mil Cathode) (3 = ) Device Type 3 (4-mil Cathode) (4 = ) Device Type 4 (2-mil Cathode)</td>
</tr>
<tr>
<td>3-18.</td>
<td>Turn-Off Characteristics for GTO-Thyristor with Varying Load Current. Input Source ((V_{goc}, L_{gs} \text{ Kept Constant}) ([I_A, I_{gq}] = f(t), R_L) Parameter Device Type 3 (4-mil Cathode)</td>
</tr>
<tr>
<td>Figure</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>------</td>
</tr>
<tr>
<td>3-19. Turn-Off Gain and Storage Time for GTO Thyristor with Varying Load Current Input Source ((V_{goc}, L_{gs})) Kept Constant Device 3 (4-mil Cathode)</td>
<td>86</td>
</tr>
<tr>
<td>3-20. Switching Performance of GTO Thyristor as Function of Temperature. Device 2 (8-mil Cathode) Conditions: (I_T = 8\ A) = constant, (V_D = 200\ V), (L_{gs} = 4.6\ \mu H)</td>
<td>87</td>
</tr>
<tr>
<td>3-20a. Storage Time (t_S = f(T))</td>
<td>87</td>
</tr>
<tr>
<td>3-20b. Rise Time and Fall Time ([t_r, t_f] = f(T))</td>
<td>87</td>
</tr>
<tr>
<td>3-21. Switching Performance of GTO-Thyristor as Function of Temperature, Device 3 (4-mil Cathode) Conditions: (I_T = 8\ A) = constant, (V_D = 200\ V), (L_{gs} = 4.6\ \mu H)</td>
<td>88</td>
</tr>
<tr>
<td>3-21a. Storage Time (t_S = f(T))</td>
<td>88</td>
</tr>
<tr>
<td>3-21b. Rise Time and Fall Time ([t_r, t_f] = f(T))</td>
<td>88</td>
</tr>
<tr>
<td>3-22. Switching Performance of GTO-Thyristor as Function of Temperature, Device 4 (2-mil Cathode) Conditions: (I_T = 8\ A) = constant, (V_D = 200\ V), (L_{gs} = 4.6\ \mu H)</td>
<td>89</td>
</tr>
<tr>
<td>3-22a. Storage Time (t_S = f(T))</td>
<td>89</td>
</tr>
<tr>
<td>3-22b. Rise Time and Fall Time ([t_r, t_f] = f(T))</td>
<td>89</td>
</tr>
<tr>
<td>3-23. Peak Gate Current Required for Turning Off a GTO Thyristor as Function of Temperature and Negative Gate Bias Conditions: (I_T = 8\ A) = constant, (V_D = 200\ V), (L_{gs} = 4.6\ \mu H)</td>
<td>91</td>
</tr>
<tr>
<td>3-23a. (I_{GT} = f(T), V_{goc} ) Parameter, 8-mil Cathode</td>
<td>91</td>
</tr>
<tr>
<td>3-23b. (I_{gqm} = f(T), V_{goc} ) Parameter, 4-mil Cathode</td>
<td>91</td>
</tr>
<tr>
<td>3-23c. (I_{gqm} = f(T), V_{goc} ) Parameter, 2-mil Cathode</td>
<td>91</td>
</tr>
<tr>
<td>Figure</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>------</td>
</tr>
<tr>
<td>3-24. Two-Point Probe Spreading Resistance Profile (C-D) through $P^+$ Gate showing Total Up Conversion of $N^-$ Region. (Insert shows Schematic of Cross Section and Probe Travel Pass)</td>
<td>94</td>
</tr>
<tr>
<td>3-25. Two-Point Probe Spreading Resistance Profile (A-B) through $N^+$ Cathode Showing Partial Up Conversion of $N^-$ Region in Direction of $P^+$ Anode. (Insert shows Schematic of Cross Section and Probe Travel Pass)</td>
<td>94</td>
</tr>
<tr>
<td>3-26. Comparison of Power-Switching Capability with Respect to Cost as a Function of Frequency for Thyristors, GTO's, and transistors (The cost Line at $f = 50$ kHz indicates where the GTO Type D3 would be in this graph for 400 V, 8 A operation using the data of Table 3-3)</td>
<td>99</td>
</tr>
<tr>
<td>4-1. GTO Structure showing Anode Short (By-Pass Transistor) and Series Schottky Barrier aligned with Center of Cathode</td>
<td>102</td>
</tr>
<tr>
<td>4-2. Geometry Overlay of Cathode and Anode Surface showing non-regenerative Center Region (Anode Short or Schottky Diode)</td>
<td>105</td>
</tr>
<tr>
<td>4-3. VI Characteristics of GTO showing Difference in Turn-On for Device with Anode Short (G400-1, Left) and Device with Series Schottky Barrier (G400-8, Right)</td>
<td>107</td>
</tr>
<tr>
<td>4-4. Turn-On Sensitivity as Function of Temperature for GTO with Anode Short (dashed line) and Series Schottky Diode (solid line)</td>
<td>110</td>
</tr>
<tr>
<td>4-5. Maximum Turn-Off Capability for GTO as Function of Temperature</td>
<td>111</td>
</tr>
<tr>
<td>4-6. Turn-Off Failure for GTO-SCR at Location Most Remote from Gate Contact</td>
<td>113</td>
</tr>
<tr>
<td>4-7. Schematic of Epi-GTO featuring Resistive Cathode with Isolated Center to achieve Dynamic Ballastting (Defocusing)</td>
<td>115</td>
</tr>
</tbody>
</table>
Figure 4-8. Cathode Load Response $I_K = f(t)$ (Left), and Anode Current $I_A = f(t)$ (Right) for Epitaxial (N)PN$^-$N(P$^+$) GTO-Thyristor with Std. Diffused Cathode Emitter (Top) and Resistive, Defocused Cathode Emitter (Bottom) $T = 125^\circ C$, Vert. = 2A/Div, Hor. = 10 $\mu$s/Div .................. 117

Figure 4-9. Turn-Off Response for Epitaxial (N)PN$^-$N(P$^+$) GTO in Cathode Load Circuit, $I_K = f(t)$ (Left), $I_A = f(t)$ (Right). Top Traces are for fully Metallized, Resistive Cathode; Bottom Traces are for Edge Metallized Defocused Cathode. $T = 125^\circ C$, Vert. = 2A/Div, Hor. = 2 $\mu$s/Div .................. 119

A-1. Sample Plots Language Statement (Top) and Computer Generated Artwork (Bottom). The "Figure" numbers that Follow the Plots Statements (separated by semicolons) Correspond to Numbered Shapes on the Artwork (After B. J. Korenjak'74-1) ............. 128

A-2. Computer Program (Plots Language) for Artwork Generation to Produce Photomask Set for 3x3 Array of GTO-Devices; Line 10-8020, 14 pages (see Appendix B and Figure 3-6) ..................... 131

B-1. Photomask Set for Fabrication of 3x3 Array of GTO Test Geometries, Center Contains Diagnostics and Alignment Pattern. (For Dimensions and Use in Process See pp. 53-55, and 56-58, respectively) ..................... 146

C-1. Static Data of Computer-Tested All-Epitaxial GTO-Thyristors. Lot 97E; Standard Cathode, $R_{sk} \sim 0.7\Omega /\square$ (See Chapter IV, Table 4-1) ..................... 154

C-2. Static Data of Computer-Tested All-Epitaxial GTO-Thyristors. Lot 97H; Implanted, Defocused Cathode, $R_{sk} \sim 20\Omega /\square$ ..................... 157
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Page of First Appearance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_1$</td>
<td>Common base current gain of transistor 1, (NPN)</td>
<td>4</td>
</tr>
<tr>
<td>$a_2$</td>
<td>Common base current gain of transistor 2, (PNP)</td>
<td>4</td>
</tr>
<tr>
<td>$\beta_1$</td>
<td>Common emitter current gain of transistor 1, (NPN)</td>
<td>4</td>
</tr>
<tr>
<td>$\beta_2$</td>
<td>Common emitter current gain of transistor 2, (PNP)</td>
<td>4</td>
</tr>
<tr>
<td>$D_n$</td>
<td>Diffusion coefficient</td>
<td>19</td>
</tr>
<tr>
<td>$E_{A(f_1)}$</td>
<td>Anode energy absorbed during fall time $t_{f1}$</td>
<td>97</td>
</tr>
<tr>
<td>$E_{A(f_2)}$</td>
<td>Anode energy absorbed during tail period $t_{f2}$</td>
<td>97</td>
</tr>
<tr>
<td>$E_{A(tr)}$</td>
<td>Anode energy absorbed during rise time interval</td>
<td>97</td>
</tr>
<tr>
<td>$E_{D(tot)}$</td>
<td>(Total) Absorbed energy per cycle</td>
<td>96</td>
</tr>
<tr>
<td>$E_{G(f_1)}$</td>
<td>Gate energy absorbed during fall time $t_{f1}$</td>
<td>97</td>
</tr>
<tr>
<td>$E_{G(f_2)}$</td>
<td>Gate energy absorbed during tail period $t_{f2}$</td>
<td>97</td>
</tr>
<tr>
<td>$E_{G(tr)}$</td>
<td>Gate energy absorbed during rise time interval</td>
<td>97</td>
</tr>
<tr>
<td>$E_{(on)}$</td>
<td>&quot;On&quot; state energy</td>
<td>97</td>
</tr>
<tr>
<td>$E_{t(off)}$</td>
<td>(Total) Turn-off energy absorbed</td>
<td>97</td>
</tr>
<tr>
<td>$E_{t(on)}$</td>
<td>(Total) Turn-on energy absorbed</td>
<td>97</td>
</tr>
<tr>
<td>$f$</td>
<td>Frequency</td>
<td>98</td>
</tr>
<tr>
<td>$F_D$</td>
<td>Duty factor</td>
<td>96</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Page of First Appearance</td>
</tr>
<tr>
<td>---------</td>
<td>--------------------------------------------------</td>
<td>--------------------------</td>
</tr>
<tr>
<td>$G_{gq}$</td>
<td>Turn-off gain</td>
<td>6</td>
</tr>
<tr>
<td>$G_{gq}(\text{max})$</td>
<td>Maximum turn-off gain</td>
<td>24</td>
</tr>
<tr>
<td>$G_{L}$</td>
<td>Loop gain</td>
<td>5</td>
</tr>
<tr>
<td>$h_{FE}$</td>
<td>DC-current gain (common emitter)</td>
<td>66</td>
</tr>
<tr>
<td>$\Theta$</td>
<td>Thermal resistance</td>
<td>98</td>
</tr>
<tr>
<td>$I_A$</td>
<td>Anode Current</td>
<td>4</td>
</tr>
<tr>
<td>$I_{A(\text{max})}, I_{T \text{off}(\text{max})}$</td>
<td>Maximum anode current that can be turned off</td>
<td>27</td>
</tr>
<tr>
<td>$I_G$</td>
<td>Gate current</td>
<td>4</td>
</tr>
<tr>
<td>$I_{gt}$</td>
<td>Gate trigger current</td>
<td>50, 61</td>
</tr>
<tr>
<td>$I_{gq}$</td>
<td>Gate current during turn-off</td>
<td>66</td>
</tr>
<tr>
<td>$I_k$</td>
<td>Cathode Current</td>
<td>15</td>
</tr>
<tr>
<td>$I_T$</td>
<td>&quot;On&quot; state current (forward conduction current)</td>
<td>50, 82</td>
</tr>
<tr>
<td>$I_z$</td>
<td>$z$-component of current</td>
<td>20</td>
</tr>
<tr>
<td>$J_1$</td>
<td>Gate-cathode junction</td>
<td>16</td>
</tr>
<tr>
<td>$J_2$</td>
<td>Center (forward blocking) junction</td>
<td>16</td>
</tr>
<tr>
<td>$J_3$</td>
<td>Anode (reverse blocking) junction</td>
<td>16</td>
</tr>
<tr>
<td>$J_z$</td>
<td>$z$-component of current density</td>
<td>19</td>
</tr>
<tr>
<td>$J_{z(\text{max})}$</td>
<td>Maximum Current Density</td>
<td>21</td>
</tr>
<tr>
<td>$J_{z(\text{on})}$</td>
<td>(Average) On-state current density</td>
<td>21</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Page of First Appearance</td>
</tr>
<tr>
<td>---------</td>
<td>-------------------------------------------------------</td>
<td>--------------------------</td>
</tr>
<tr>
<td>$L_{gs}$</td>
<td>Gate Series Inductance</td>
<td>68</td>
</tr>
<tr>
<td>$L_n$</td>
<td>Diffusion Length (minority carriers)</td>
<td>19</td>
</tr>
<tr>
<td>$L_x$</td>
<td>Cathode Width</td>
<td>18</td>
</tr>
<tr>
<td>$L_y$</td>
<td>Cathode Length</td>
<td>16</td>
</tr>
<tr>
<td>$N, n$</td>
<td>Donor (electron) dominated semiconductor region</td>
<td>4</td>
</tr>
<tr>
<td>$N^-, n^-$</td>
<td>Lightly doped N region</td>
<td>8, 17</td>
</tr>
<tr>
<td>$N^+, n^+$</td>
<td>Heavily doped N region</td>
<td>8, 17</td>
</tr>
<tr>
<td>$</td>
<td>N_A</td>
<td>$</td>
</tr>
<tr>
<td>$</td>
<td>N_D</td>
<td>$</td>
</tr>
<tr>
<td>$n_e$</td>
<td>Electron concentration</td>
<td>18</td>
</tr>
<tr>
<td>$P, p$</td>
<td>Acceptor (hole) dominated semiconductor region</td>
<td>4</td>
</tr>
<tr>
<td>$P^-, p^-$</td>
<td>Lightly doped P region</td>
<td>8, 17</td>
</tr>
<tr>
<td>$P^+, p^+$</td>
<td>Heavily doped P region</td>
<td>8, 17</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Power dissipation</td>
<td>99</td>
</tr>
<tr>
<td>$q$</td>
<td>Electron charge</td>
<td>19</td>
</tr>
<tr>
<td>$\Delta Q$</td>
<td>Charge in $\Delta x_b$</td>
<td>22</td>
</tr>
<tr>
<td>$Q_N^1$</td>
<td>Charge in Base</td>
<td>29</td>
</tr>
<tr>
<td>$Q_{off}$</td>
<td>Total charge in device volume during turn-off</td>
<td>11</td>
</tr>
<tr>
<td>$R_g$</td>
<td>Lateral gate resistance</td>
<td>25</td>
</tr>
</tbody>
</table>

\footnote{For definition of symbols in Pg. 29-40 Kurata's notation is strictly followed. Please turn to the defining Figures 2-6 and 2-10.}
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Page of First Appearance</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_G$</td>
<td>Gate series resistance</td>
<td>15</td>
</tr>
<tr>
<td>$R_i$</td>
<td>Internal device resistance</td>
<td>14</td>
</tr>
<tr>
<td>$R_L$</td>
<td>Load resistance</td>
<td>14</td>
</tr>
<tr>
<td>$R_{sp}, R_{\square p}$</td>
<td>Gate (p-base) sheet resistance</td>
<td>48, 51</td>
</tr>
<tr>
<td>$\rho_p$</td>
<td>Average gate (P-base) resistivity</td>
<td>25</td>
</tr>
<tr>
<td>$t$</td>
<td>Time</td>
<td>22</td>
</tr>
<tr>
<td>$T$</td>
<td>Temperature</td>
<td>50</td>
</tr>
<tr>
<td>$t_1$</td>
<td>Time instant at initiation of turn-off</td>
<td>11</td>
</tr>
<tr>
<td>$t_2$</td>
<td>Time instant at completed turn-off (Q = 0)</td>
<td>11</td>
</tr>
<tr>
<td>$t_d$</td>
<td>Delay time</td>
<td>--</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Fall time</td>
<td>15</td>
</tr>
<tr>
<td>$t_{f1}$</td>
<td>(Forced) Fall time to tail break</td>
<td>96</td>
</tr>
<tr>
<td>$t_{f2}$</td>
<td>Tail decay time constant</td>
<td>96</td>
</tr>
<tr>
<td>$T_j$</td>
<td>Junction temperature</td>
<td>98</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>(Total) Turn-off time</td>
<td>119</td>
</tr>
<tr>
<td>$t_{on}$</td>
<td>(Total) Turn-on time</td>
<td>64</td>
</tr>
<tr>
<td>$\tau_{pA}$</td>
<td>Hole life time in vicinity of anode</td>
<td>97</td>
</tr>
<tr>
<td>$t_p$</td>
<td>P-base (Gate) transit time</td>
<td>48</td>
</tr>
<tr>
<td>$t_{p(\text{off})}$</td>
<td>Duration of turn-off pulse</td>
<td>96</td>
</tr>
<tr>
<td>$t_{p(\text{on})}$</td>
<td>Duration of turn-on pulse</td>
<td>96</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Rise time</td>
<td>50, 51</td>
</tr>
<tr>
<td>$t_s$</td>
<td>Storage time</td>
<td>15</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
<td>Page of First Appearance</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
<td>--------------------------</td>
</tr>
<tr>
<td>T</td>
<td>Duration of period</td>
<td>96</td>
</tr>
<tr>
<td>$\tau_B$</td>
<td>Minority carrier lifetime in base (Gate)</td>
<td>29</td>
</tr>
<tr>
<td>$\tau_{\text{eff}}$</td>
<td>Effective lifetime</td>
<td>19</td>
</tr>
<tr>
<td>$\tau_n$</td>
<td>(Average) lifetime in N-base</td>
<td>50, 51</td>
</tr>
<tr>
<td>$\tau_P$</td>
<td>(Average) lifetime in P-base (gate)</td>
<td>73</td>
</tr>
<tr>
<td>$V_A$</td>
<td>Anode Voltage</td>
<td>14</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Anode supply voltage</td>
<td>50, 68</td>
</tr>
<tr>
<td>$V_{\text{DRXM}}$</td>
<td>(Maximum) forward blocking voltage with parallel gate-cathode resistor</td>
<td>61</td>
</tr>
<tr>
<td>$V_{G\text{ br}}, V_{Gk}$</td>
<td>Gate-Cathode breakdown voltage</td>
<td>8</td>
</tr>
<tr>
<td>$V_{goc}$</td>
<td>Gate source voltage</td>
<td>68</td>
</tr>
<tr>
<td>$v_s$</td>
<td>Spreading velocity</td>
<td>66</td>
</tr>
<tr>
<td>$V_T$</td>
<td>On-state voltage (across anode-cathode), forward voltage drop</td>
<td>51</td>
</tr>
<tr>
<td>$W_P$</td>
<td>(Gated) P-base width</td>
<td>16</td>
</tr>
<tr>
<td>$x_{j1}$</td>
<td>Cathode-gate junction depth coordinate</td>
<td>47</td>
</tr>
<tr>
<td>$x_{j2}$</td>
<td>Center (forward blocking) junction depth coordinate</td>
<td>47</td>
</tr>
<tr>
<td>$x_{j3}$</td>
<td>Anode (reverse blocking) junction depth coordinate</td>
<td>47</td>
</tr>
<tr>
<td>$x_b$</td>
<td>Transition coordinate (moving boundary during turn-off)</td>
<td>16</td>
</tr>
<tr>
<td>$\Delta x_{b}$</td>
<td>Transition region from &quot;On&quot; state to &quot;Off&quot; state</td>
<td>16</td>
</tr>
</tbody>
</table>
I. INTRODUCTION

A. Thyristors and Transistors as Electronic Switches

Four layer semiconductor structures (i.e., NPNP or PNPN), generically known as thyristors, exhibit characteristics similar to those of gas thyratrons. They may be triggered from a high voltage blocking state ("off") into a high current state ("on") by means of a single pulse applied to the control electrode, the gate. Thus, we could consider this semiconductor structure the electronic switch analogous of the electro-mechanical, latching relay.

Once the four layer device is in the "on" state, it is self regenerative, and turn-off may be achieved only if the anode voltage is removed for a time, sufficiently long to cause the decay of conduction current below the "holding" level.

We may now compare the features for electronic switching of a transistor with those of a thyristor.

Transistors can be switched from the control electrode (base) into the "on" state with considerable power gain. For example: the drive power may be 1.5 watts, derived from a 50% duty cycle square wave input of 1.5 volts and 2.0 amperes. The load power may be 750 watts for a current of 10 amperes through a resistive load with a 150 volt supply voltage. Thus the power gain is 500. The drive power has to be supplied to the base during the entire "on" time. Turn-off (without regard to speed) is accomplished by simple interruption of the drive circuit.
Thyristors can be switched from the gate with even higher power gain, because the trigger current may be kept in the milliampere range and the output current is limited essentially by the load resistance. For example: The input energy for triggering may be 150 x 10^{-9} watt-seconds for a 1 milliampere, 1.5 volt input pulse lasting 100 microseconds. The load power may be 750 watts for a current of 10 amperes through a resistive load, switched at a rate of 1.0 kilohertz with 50% duty cycle from a 150 volt supply. Thus, the power gain is 1 x 10^7, indeed very high.

A drive pulse is not required during the "on" time. Turn-off is accomplished by interruption of the load current, i.e., by means of commutation of this current through passive and active components of similar ratings than those specified for the actual power switch. Therefore, a considerable turn-off effort is required.

As we can see, the transistor is good for turn-on and poor for the "on" state when used as an electronic switch, while the thyristor is excellent for the "on" state and poor for turn-off, considering the same class of applications. Generally, transistors are more suitable for lower power and higher frequency operation, whereas thyristors are better employed when higher power output and lower frequency is called for.
B. The Gate Turn-Off Thyristor (GTO)

A desirable technical solution to an electronic switch would be, to have a device which combines the high frequency and/or high power capabilities of both transistors and thyristors, respectively, which can be switched "on" and "off" from the control electrode with a high power gain, and in addition does not need external drive power in order to remain in the "on" state.

Indeed, examination of the physics for four-layer structures and application of transistor theory indicates, that the realization of such a switch is possible. This switch is known as a Gate Turn-Off thyristor (GTO).

A device with turn-off capability from the gate was first described by J. M. Goldey, et al.\(^{60-1}\) and R. H. vanLigten, et al.\(^{60-2}\).

The important points of the existing theory for GTO's will be presented in chapter II. However, some general, qualitative statements concerning the possibility of turn-off from the gate and the difficulties encountered are given here.

1. Simple, First Order Observations

The four layer structure of Figure 1-1a may be considered as a composite of an NPN and a PNP structure interconnected as shown in Figure 1-1b. Thus, a two-transistor equivalent circuit can be constructed containing a complementary transistor pair in a feedback configuration as shown in Figure 1-1c. From the currents and gain
Figure 1-1. GTO Thyristor

Figure 1-1a. Schematic Four Layer Structure
Figure 1-1b. Composite NPN-PNP Structure
Figure 1-1c. Equivalent Transistor Circuit
Figure 1-1d. Loop Gain Diagram
factors in this figure, we may show in Figure 1-1d the loop gain with the gate terminal included. From these, we obtain the following:

\[ G_L = \beta_1 \beta_2 \frac{\alpha_2 I_A + I_G}{\alpha_2 I_A} \]  

where: 
- \( G_L \) = total loop gain,
- \( \beta_1 \) = common emitter current gain of transistor T1
- \( \beta_2 \) = common emitter current gain of transistor T2
- \( \alpha_1 \) = common base current gain of transistor T1
- \( \alpha_2 \) = common base current gain of transistor T2
- \( I_A \) = anode current, and
- \( I_G \) = gate current

The condition for "turn-on" is given when the value of the loop gain reaches unity. Thus, the device will switch into the conducting state at

\[ G_L = \beta_1 \beta_2 \frac{\alpha_2}{\alpha_2} \frac{I_A + I_G}{I_A} \geq 1 \]  

Since the gain for any transistor initially increases with current to a peak value, once the product \( \beta_1 \beta_2 \) becomes unity, the device will remain "on" without a gate signal.

It is now apparent that the condition for "turn-off" is reached, if it is possible to reduce the loop gain by some means again to a value equal or less to unity. This can be accomplished by reversal of the gate current. Thus, for turn-off, the relation 1-2 for the loop
gain $G_L$ changes to

$$G_L = \beta_1 \beta_2 \frac{\alpha_2}{\alpha_2} \frac{I_A - I_G}{I_A} \leq 1$$  \hspace{1cm} 1-3

We may now define a "turn-off gain" as the ratio of anode current in the "on" condition to the gate current necessary to reduce the loop gain to unity. Using equation 1-3 and the relation

$$\alpha = \beta/(\beta + 1)$$

we get

$$\frac{I_A}{I_G/G_L=1} = G_{eq} = \frac{\alpha_1}{(\alpha_1 + \alpha_2)^{-1}}$$  \hspace{1cm} 1-4

Equation 1-4 gives some qualitative guidance for the choice of the $\alpha$'s. It can be seen that a high turn-off gain may be obtained for $\alpha_1$ being close to unity if $\alpha_2$ is kept small (i.e., $\approx 0.2$) at the same time. However, above discussion is only useful for explaining the basic concept of obtaining turn-off in an NPNP structure. Specifically, we have to take notice of the fact that any practical device is three dimensional, and variations in at least two dimensions have to be considered.

2. Qualitative, Two-Dimensional Considerations

The dynamic behavior of a two-dimensional model is described by E. D. Wolley in which he finds a relationship between turn-off gain and turn-off time under the assumption of a constant gate current during the turn-off phase. M. Kurata developed this two-dimensional approach further using the charge control concept.
CAD model assumes that in the expression for the (one dimensional) turn-off gain the $\alpha$'s are constant.

In an actual device, however, the $\alpha$'s are functions of current density, temperature, anode voltage, and spatial distribution, and a constant gate current can only be approximated. Furthermore, the turn-off process involves a continuously changing current distribution within the device. Thus, when considered from this point of view, the $\alpha$'s become functions of time. Therefore, Equation 1-4 does not provide sufficient insight into the turn-off mechanism of a GTO.

In general, during the turn-off process the conducting electron hole plasma is deflected from an area close to the gate having the highest negative potential to the most remote area beneath the cathode with the least negative potential. Figure 1-2 illustrates this fact. In Figure 1-2a, we see the device in its "on-state" condition, conducting uniformly over the entire cathode area. Upon application of a negative bias to the gate, the plasma is "squeezed" into a high current density filament as shown in Figure 1-2b. Resultant local heating will often cause hot spots and thus device failure. This phenomenon is similar to reverse second breakdown in transistors, but generally more severe; because of the regenerative nature of this device, the current is restricted only by the external load resistance. Moreover, the negative gate current flowing through the lateral base resistance during turn-
Figure 1-2a. GTO-Thyristor in "On" State

Figure 1-2b. GTO-Thyristor during Turn-Off

Figure 1-2c. Lateral Voltage Drop—$V_G > V_G\text{ br}$

Figure 1-2. Turn-Off Process in Conventional GTO-Thyristor
off will produce a voltage drop which may reach the gate-cathode breakdown voltage at a current smaller than that required for turn-off as shown in Figure 1-2c. Under this condition the turn-off voltage will not be sufficient to extinguish the remote filament. Therefore, turn-off cannot occur and the device fails.

3. A Double Gate Layer, Shorted Anode GTO

It is apparent from the analysis of the gate turn-off process that for a reliable gate turn-off the following basic features are desirable:

a. A low lateral resistance of the gated base region,
b. A high breakdown voltage for the gate-cathode junction,
c. A non-regenerative section (away from the gate contact) in which the final conducting filament will extinguish itself.

Figure 1-3 depicts a structure in which these essential features are incorporated. A low resistivity p-layer in the gated base provides the low lateral resistance while a higher resistivity p-layer on top, in contact with the cathode junction, assures a high gate-breakdown voltage. In addition, adjacent to the four layer section a non-regenerative section has been included away from the gate contact. The "on-state" condition is shown in Figure 1-3a. It is essentially the same as for the conventional structure. The by-pass current through the three layer NPN transistor section can be negligible with respect
Figure 1-3a. GTO-Thyristor with Buffer Area in "On" State

Figure 1-3b. GTO-Thyristor with Buffer Area during Turn-Off

Figure 1-3. Turn-Off Process in GTO Structure with Low Resistance, High Breakdown Gate Layer
to normal rated anode current. 1)

Upon application of a negative bias to the gate, the plasma is again "squeezed" into a high density filament, as shown in Figure 1-3b. But now, current is deflected into the non-regenerative three layer section and cannot sustain itself. Further, the negative gate (base) current flows through the low resistivity base layer section, producing little lateral voltage drop, while independently the gate-cathode breakdown voltage can be kept high. Thus, avalanching (as depicted in Figure 1-2c) is prevented. As a result, safe turn-off is implemented more readily.

4. Interdigitation, Series Schottky Barrier, and Dynamic Ballasting

A very essential characteristic, desirable for a GTO is to achieve turn-off at a low negative gate voltage.

For turn-off, charge only has to be removed in accordance with the general relation

$$Q_{off} = \int_{t_1}^{t_2} I_A(t) \, dt$$

1-5

where $Q_{off}$ is the total charge in the device, $t_1$ is the time at the onset of the gate turn-off pulse, and $t_2$ is the instant at which the

---

1This is true only for the case that the width of the cathode is large compared to the size of the shorting N region, see figure 1-3.
sum of the $\alpha$'s is reduced to less than unity at every point within the entire structure, as required by equation 1-3. This process is basically independent of voltage. Thus, the importance of a high gate-cathode breakdown is diminished (feature b discussed in the previous section).

A design which is highly interdigitated or finely subdivided is obviously of advantage. It will minimize lateral sweepout times for minority carriers.

An investigation of the dependence of electrical characteristics on the geometry of a GTO-thyristor (mainly the width of the cathode for constant area) and an explanation of the behavior of such two-dimensional devices is subject of chapter III.

In the course of this work it became apparent that although marked improvements in turn-off were achieved through interdigitation as well as a better understanding of the circuit-device interaction was obtained, the implementation of non-regenerative regions (feature c, sometimes described as "anode shorts" or "by-pass transistors") would greatly impair turn-on performance, especially at low temperatures. A unique concept was introduced by the author by adding a Schottky barrier in series with the bypass transistor to the GTO-structure\(^{79-1}\) thus negating the adverse effects on turn-on while retaining the improved features for turn-off, independent of cathode width and cathode spacing. Chapter IV-A gives details about these experiments and analyzes the results.
Still, there were burn-out spots due to high current density filaments in the center of the cathode observed. This led to the introduction of the principle of "defocusing" or "dynamic ballasting" [80-1].

Briefly, this method uses a slightly resistive cathode layer, the sheet resistance being closely controlled by ion implantation. The center of the cathode is insulated from the cathode metal. During the "on" state at nominal current densities, the vertical resistance is small and has little effect on the internal forward voltage drop. While the device is being turned off, however, the "squeezing" of current into a narrow, high current density filament is markedly impaired owing to the high lateral emitter resistance and related voltage drops which in turn debias the center of the cathode. Chapter VI-B deals with this aspect of preventing failures in GTO-structures.
II. THEORY OF GATE TURN-OFF IN FOUR LAYER DEVICES

The previous chapter described the condition for turn-off in an NPNP structure in a most general manner; i.e., in terms of the loop gain \( G_L < 1 \) (Equation 1-3) and the turn-off gain \( G_{gq} \) (Equation 1-4). However, it was pointed out that these formulae were of little practical value, because the current gains \( (\alpha_1 \text{ and } \alpha_2) \) in an actual device are device geometry and time dependent which we call space-time dependent. Thus, at least, a dynamic two-dimensional model is required to explain physical happenings in the interior of the GTO-thyristor which may relate to the electrical characteristics observed at the terminals.

A. A Two-Dimensional Analytical Model

Duane Wolley\(^{66-1}\) proposed a two-dimensional, analytical model which contains several important features describing the turn-off for a four layer device.

In Figure 2-la, the schematic for turn-off is depicted. Initially, the NPNP structure is conducting the current \( I_A \) being determined simply by the anode voltage \( V_A \) and the load resistance \( R_L \) (assuming the "on" resistance of the device \( R_A << R_L \)). A step function is applied to the gate (Figure 2-lb) by closing the switch in the gate lead; i.e., a negative potential at the base of the NPN transistor section will cause a negative gate current \( I_G \) to flow and tend to reverse bias the cathode-emitter to a value of \(-V_G\). The output response is seen in Figure 2-lc.
Figure 2-1a. Schematic Circuit Diagram

STEP FUNCTION (SWITCH CLOSED)

Figure 2-1b. Input Drive Function

Figure 2-1c. Output Response

Figure 2-1. Conditions for Turn-Off of a GTO
For the duration of the storage time $t_s$, the anode current remains essentially constant, the minority carrier electron-hole plasma is being "squeezed" toward the center of the device as shown in Figure 2-2.

For the duration of the fall time $t_f$, the plasma density is being reduced by the gate current until the blocking junction $J_2$ comes out of saturation and the device turns off.

1. The Turn-Off Velocity

In order to obtain a quantitative evaluation for the storage time and fall time, the velocity with which the plasma is squeezed laterally toward the center of the cathode is determined.

The conditions are derived from the model in Figure 2-3. Here, the net rate of removal of minority carriers from an elemental volume ($\Delta x_b w L_y$) at the boundary $x_b$, between the "on" and "off" region is considered; the center is taken as the origin (see Figure 2-3a). The cathode-emitter junction is reverse biased ("off") to the right of $\Delta x_b$, i.e., toward the gate with the negative potential applied. It is forward biased ("on") in the region to the left of $\Delta x_b$, i.e., toward the center of the emitter.

The gradient of the electron concentration in the "on" region is constant in the $z$-direction, pure diffusion is assumed for carrier transport across the N-base (see Figure 2-3b).
Figure 2-2. Electron-Hole Plasma "Squeezed" Toward Center of Cathode during Turn-Off Process
Figure 2-3. Model for Deriving Turn-Off Parameters for a GTO Thyristor (after D. Wolley66-1)

Figure 2-3a. Two-Dimensional Arrangement

Figure 2-3b. Electron Distribution in Z-Direction

Figure 2-3c. Form Function of Electron Distribution in X-Direction
The removal of minority carriers at the boundary $x_b$ is the gate current $I_G/2$ minus the electron diffusion current into the elemental volume in the $x$-direction, the magnitude of which is set by the slope $1/L_n$. $L_n$ is defined as an effective diffusion length dependent on electric field, minority carrier lifetime, and ambipolar diffusion coefficient ($L_n = \sqrt{D_n \tau_{\text{eff}}}$). Reasonably, $L_n$ is assumed to have the value of the diffusion length for minority carriers in the gated base. Thus, the carrier distribution in the $x$-direction (lateral) is of the shape $f(x)$ as shown in Figure 2-3c.

The general expression for the minority carrier distribution in the gated base can now be written as

$$n(x,z) = n(x)f(x)$$ \hspace{1cm} (2-1)

Note: The distribution is assumed constant in the $y$-direction over the length $L_y$, of the cathode stripe.

The current density in the $z$-direction is then according to the diffusion part of the minority carrier transport equations

$$J_z(x,z) = qD_n \frac{\partial n(x,z)}{\partial z}$$ \hspace{1cm} (2-2)

and with substituting Equation 2-1 into 2-2

$$J_z(x,z) = qD_n f(x) \frac{\partial n(x)}{\partial z}$$ \hspace{1cm} (2-3)
However, since the gradient across \( w \) is constant (Figure 2-3b)

\[
\frac{\partial n(z)}{\partial z} = -\frac{n_e}{w_p}
\]

and

\[
n(z) = -\int_0^{w_p} \frac{n_e}{w_p} \, dz = n_e \left(1 - \frac{z}{w_p}\right)
\]

The electron distribution along \( x \) as shown in Figures 2-3 is

\[
f(x) = \begin{cases} 
1 & 0 < x < x_b \\
\exp\left(-\frac{(x-x_b)}{L_n}\right) & x_b < x < \infty
\end{cases}
\]

The cathode current is given by

\[
I_k = 2I_z = 2L_y \int_0^\infty J_z(x, z) \, dx
\]

and using Equations 2-3, 2-4, and 2-6

\[
I_k = -2L_y \left[ \int_0^{x_b} qD_n \frac{n_e}{w_p} \, dx + \int_{x_b}^\infty qD_n \frac{n_e}{w_p} \exp\left(-\frac{(x-x_b)}{L_n}\right) \, dx \right]
\]

The evaluated integral then assumes the form

\[
I_k = -2L_y qD_n \frac{n_e}{w_p} \left(x_b + L_n\right)
\]
An important consequence of Equation 2-9 is, that the highest electron concentration will occur in the completely "squeezed" state for \( x_b = 0 \) at the center of the emitter. The current density is then rising to

\[
J_{z(\text{max})} = J_{z(\text{on})} \left( \frac{L_x}{L_n} \frac{I_A - I_G}{I_A} \right)
\]

where

\[
J_{z(\text{on})} = \frac{I_k}{L_x L_y}
\]

is the uniform current density throughout the active device area in the "on" state prior to initiation of "turn-off".

For the determination of the lateral diffusion current into the elemental volume \((\Delta x, w_p L_y)\) we set

\[
I_x(x_b) = L_y \int_{0}^{w_p} J_x(x_b, z) \, dz
\]

where \( J_x \) is similarly determined as in Equation 2-2

\[
J_x(x_b, z) = qD_n \frac{\partial n(x, z)}{\partial x}
\]

evaluated at \( x = x_b \) yields as seen from Figure 2-3c and condition 2-6

\[
J_x(x_b, z) = qD_n n(z)f'(x_b) = qD_n n(z) \left( -\frac{1}{L_n} \right)
\]
Now, the electron distribution in the z-direction can be substituted from Equation 2-5, which allows Equation 2-12 to be written as

\[ I_x(x_b) = -L_y q \frac{D_n}{2L_n} n_e \int_0^{w_p} (1 - \frac{z}{w_p}) dz \]

\[ = -L_y q \frac{D_n}{2L_n} n_e w_p \]

The minority carrier charge within the elemental volume is given by

\[ \Delta Q = -L_y q \Delta x_b \int_0^{w_p} n(x,z) dz \]

assuming \( f(x) \sim f(x_b) = 1 \) throughout \( \Delta x_b \), \( n(z) \) may be again substituted from Equation 2-5 resulting in

\[ \Delta Q = -L_y q n_e \Delta x_b \frac{w_p}{2} \]

Finally, the net change of charge in the elemental volume with time is the sum of the (conventional) diffusion current \( I_x(x_b) \) and the gate current \( I_G/2 \), i.e.,

\[ \frac{\Delta Q}{\Delta t} = I_x + \frac{I_G}{2} \]
Substituting Equations 2-15 and 2-17 into Equation 2-18 gives

$$-L_y q n_e \frac{\Delta x_b}{\Delta t} \left( \frac{w}{2} \right) = -L_y q \frac{D_n}{2L_n} n_e w p + \frac{I_G}{2}$$

then solved for $\Delta x_b/\Delta t$ is

$$\frac{\Delta x_b}{\Delta t} = \frac{D_n}{L_n} - \frac{I_G}{L_y q n_e w_p}$$  \hspace{1cm} 2-19

An explicit expression for the turn-off velocity is obtained by solving Equation 2-9 for the electron concentration at the cathode emitter edge $(z=0)$ and substituting it into Equation 2-19; with $\Delta x_b + 0$ we obtain

$$\frac{dx_b}{dt} = \frac{D_n}{L_n} + \frac{I_G}{I_k w_p} \left( \frac{2D_n}{w_p} \right) (x_b + L_n)$$  \hspace{1cm} 2-20

The cathode current during turn-off is

$$I_k = I_A - I_G$$  \hspace{1cm} 2-21

and the transit time for carriers through the base can be expressed as

$$t_p = \frac{w_p^2}{2D_n}$$  \hspace{1cm} 2-22
further, with the turn-off gain as defined in Equation 1-4

\[ G_{t-o} = \frac{I_A}{I_G} \]  

we can write Equation 2-20 as follows

\[ \frac{dx_b}{dt} = \frac{x_b + L_n}{t_p (G_{gq} - 1)} + \frac{D_n}{L_n} \]  

2. The Storage Time and Maximum Turn-Off Gain

The storage time \( t_s \) is essentially the time it takes to squeeze the electron-hole plasma from its original uniform flow through the entire device cell of length \( L_y \) and width \( L_x \) into a filamentary line of width \( 2L_n \). One can therefore integrate equation 2-24 in \( x \) between the limits \( L_x/2 \) and \( L_n \),

\[ - \int_0^{t_s} dt = t_p (G_{gq} - 1) \int_{L_x/2}^{L_n} \frac{dx_b}{x_b + L_n - t_p (G_{gq} - 1) D_n L_n} \]  

which results in

\[ t_s = t_p (G_{gq} - 1) \ln \frac{(2L_n L_y / w_p)^2 + (4L_n^2 / w_p^2) - G_{gq} + 1}{(4L_n^2 / w_p^2) - G_{gq} + 1} \]  

The storage time \( t_s \) approaches infinity when the denominator of the logarithmic term in Equation 2-26 goes to zero, i.e., we obtain for the maximum turn-off gain

\[ G_{gq}(\text{max}) = \frac{4L_n^2}{w_p^2} + 1 \]
Equation 2-26 can be used to calculate the storage time as a function of turn-off gain. The results of such calculations are depicted in Figure 2-4 using the lateral diffusion length $L_n$ as parameter. As can be seen, the storage time is a strong function of the turn-off gain.

It should be noted that this turn-off gain is set by the external input circuit and output circuit conditions (see Figure 2-1a) and is limited by the internal device impedance. The turn-off gain of the one-dimensional device (i.e., in the "squeezed" state) is still governed by Equation 1-4. Thus, it is apparent that the smaller of the two values, which is obtained from either Equation 1-4 or Equation 2-27, becomes the limiting gain.

3. The Lateral Base Resistance and Maximum Turn-Off Anode Current

The lateral gate current $I_G$ during turn-off causes a voltage drop along the cathode emitter junction. This voltage drop may reach the cathode-gate breakdown voltage as observed by van Ligten and Navon and limit the allowable current to be turned off. For the device model of Figure 2-3a the maximum lateral gate resistance is experienced when the "on" region is reduced to its minimum width of $2L_n$. Thus, this lateral gate resistance beneath the half width $L_x/2$ of the cathode emitter is determined as

$$R_g = \frac{L_x - L_n}{\rho_p \frac{w}{W_L y}}$$

2-28
Figure 2-4. Storage Time vs. Turn-Off Gain
(after D. Wolley66-1)
where $\bar{\rho}_p$ is the average resistivity of the unmodulated, active gate region. Because of the restriction (see Figure 1-2c)

$$\frac{I_C}{2} R_g < V_{Gbr}$$  \hspace{1cm} 2-29

where $V_{Gbr}$ is the gate-cathode breakdown voltage, there exists an upper limit for the anode current that can be turned off. With the assumption that $(L_x/2) \gg L_n$ it then follows from Equations 2-23, 2-28, and 2-29, that

$$I_{A(max)} = \frac{4 G_{gq} V_{Gbr} w_L}{\bar{\rho}_p L_x}$$  \hspace{1cm} 2-30

4. The Fall Time

The fall time is determined by the time required to remove the charge from the volume of the device after the center junction comes out of saturation and becomes reverse biased. The negative gate current aids the removal of carriers, the time constant is short as for transistors with negative base drive. However, the charge in the ungated base ($N^-$) section must either drift or diffuse to the center junction and be collected there, or recombine with majority carriers. It then follows that there is generally a second time constant associated with the turn-off of a GTO thyristor. This second time constant causes a so-called "tail" in the turn-off characteristic and it is a function of the lifetime of minority carriers in the ungated base. An example for the output current-input current response with time is given in Figure 2-5.
Figure 2-5. Input Current $I_G$ and Output Current Response $I_A$ as Function of Time for GTO-Thyristor During Turn-Off75-1
B. A Two-Section, Charge Control Model

1. The Charge Control Concept

Mamuro Kurata developed a CAD-model for turn-off using the charge control approach. This procedure was originally described by Beaufoy and Sparks for transistors, and later applied by Davies and Petrucella to thyristors. Here, the basic idea is to take the current continuity equation, for example, as given below in one dimension for an NPN transistor

$$\frac{\partial I}{\partial z} = q \frac{\partial n(z)}{\partial t} + q \frac{n(z)}{\tau_B}$$  \hspace{1cm} 2-31

and integrate it across the base, i.e., between the limits $z = 0$ and $z = W_p$, after multiplying both sides by $\partial z$. The result is

$$I_B = \frac{d Q_N}{dt} + \frac{Q_N}{\tau_B}.$$  \hspace{1cm} 2-32

Thus, in equation 2-32 for the base current $I_B$ the carrier density $n(z)$ as a variable is now replaced by the total excess charge $Q_N$ in the base, its spatial distribution does not enter.

Equation 2-32 may be adapted to a thyristor element $N$, such that the charge control conditions describe the carrier dynamics in the vertical ($z$) direction. Adjacent elements, laterally interconnected by appropriately modeled base resistances to include conductivity modulation, can then be used to set up a two-dimensional, numerical simulation for turn-off.
However, let us first consider the four layer structure of Figure 1-1a and 1-1b and label the currents as shown in Figure 2-6. The resultant expressions for the NPN transistor section and PNP transistor section are in accordance with Equation 2-32

\[
I_1(N+1) - I_1(N) + I_{C2}(N) = \frac{dQ_1(N)}{dt} + \frac{Q_1(N)}{\tau_{B1}}
\]

and

\[
I_2(N) - I_2(N+1) + I_{C1}(N) = \frac{dQ_2(N)}{dt} + \frac{Q_2(N)}{\tau_{B2}}
\]

respectively.

For the numerical treatment of the turn-off process, Equations 2-33 and 2-34 assume different forms as the thyristor element N transits from the saturation condition, in the "on-state", through the non-saturation phase, where both transistors are in the active region, into the depletion state. For mathematical details and assumptions we refer to M. Kurata's original treatment. 74-1

2. The Junction Voltages

Next, "some relations must be assumed between the base charges Q(N) and the junction voltages V_j(N), to obtain a self-consistent device model". For the cathode junction J_1 during the conducting state a low, constant voltage is assumed. During reverse blocking, however, a depletion layer is formed. This depletion layer can be interpreted as a negative charge, the voltage developed across being proportional to the total number of fixed charges, the junction capacitance is assumed constant.
Figure 2-6a. Thyristor Element N

Figure 2-6b. Two Transistor Equivalent

Figure 2-6. Thyristor Model for Definition of Charge Control Equation
Therefore, plotting \( V_{j1} = f(Q_1) \) results in two asymptotes. \( V_{j1} = V_{j10} \) constant for positive \( Q_1 \), and \( V_{j1} = (Q_1/C_{j1}) + V_{j10} \) for negative \( Q_1 \) as depicted in Figure 2-7. The actual dependence of \( V_j \) on \( Q \) is then obtained from a curve fitting method such that the requirement \( V_j \rightarrow 0 \) for \( Q \rightarrow 0 \) is met. The result can be expressed as

\[
V_{j1}(N) = \frac{Q_1(N)}{2C_{j1}(N)} + V_{j10}(N) - \sqrt{\left( \frac{Q_1(N)}{2C_{j1}(N)} \right)^2 + V_{j10}(N)^2} \quad 2-35
\]

which is also plotted in Figure 2-7.

The relation for the anode junction \( V_{j3}(N) \) is of the same form.

\[
V_{j3}(N) = \frac{Q_2(N)}{2C_{j3}(N)} + V_{j30}(N) - \sqrt{\left( \frac{Q_2(N)}{2C_{j3}(N)} \right)^2 + V_{j30}(N)^2} \quad 2-36
\]

The voltage across the center junction can be expressed as

\[
V_{j2}(N) = \sqrt{\left( \frac{f(N)}{2C_{j2}(N)} \right)^2 + V_{j20}(N)^2} - \frac{f(N)}{2C_{j2}(N)} \quad 2-37
\]

where \( f(N) \) has the dimension of a charge consisting of two parts, an injection component during conduction, represented by the product of a current and a transit time, and a depletion charge, given by the product of a capacitance and voltage. Again, for details we refer to Ref. 74-1.

3. The Current Loop Equations

Finally, the loop equations are set up. The device structure shown in Figure 2-8 is subdivided into two sections and can be represented by an equivalent schematic as is shown in Figure 2-9.
Figure 2-7.
Voltage vs. Charge for Cathode Junction $J_1$, or Anode Junction $J_3$ (after M. Kurata)\textsuperscript{74-1}
Figure 2-8.
GTO Two-Section Model
(after M. Kurata) 74-1
Figure 2-9.
Equivalent GTO-Thyristor Circuit for Two-Section Model (after M. Kurata)74-1
Closing S1 initiates Turn-off
The loop equations are thus

\[ V_{j1}(1) = -V_{GCS} + \left[ R_{B_1}(1) + R_G \right] I_1(1) \] 2-38
\[ V_{j1}(2) = V_{j1}(2) + R_{B_1}(2) I_1(2) \] 2-39
\[ V_{j2}(2) + R_{B_1}(2) I_1(2) = V_{j2}(1) + R_{B_2}(2) I_2(2) \] 2-40
\[ V_{j1}(1) + V_{j2}(1) + V_{j3}(1) + R_A(1) I_A(1) + R_L [I_A(1) + I_A(2)] \]
\[ = V_{ACS} \] 2-41
\[ V_{j1}(2) + V_{j2}(2) - V_{j3}(2) + R_A(2) I_A(2) + R_L [I_A(1) + I_A(2)] \]
\[ = V_{ACS} \] 2-42

Equations 2-33 to 2-42 are the basis for a thyristor model, the turn-off behavior of which may be calculated by a numerical approach.

4. The Computation Method

For the numerical solution we first choose the appropriate form of the charge control equations 2-33 and 2-34, dependent whether the device section considered is in saturation, the active transistor mode, or in reverse bias, i.e., in the depletion state. Then, the expressions for the junction voltages in equations 2-35, 2-36 and 2-37 are substituted into equations 2-38 and 2-41 for \( N = 1 \), and in equations 2-39, 2-40, and 2-41 for \( N = 2 \), respectively.
Therefore, a total of 9 equations with 9 variables has to be solved simultaneously for this two-section model.\footnote{For a model containing M sections, a total of (5M-1) simultaneous equations must be solved.}

Because the charges as well as the currents are non-linear, an iterative scheme (Newton-Raphson's principle) is utilized, i.e., the variables $Q_1 \sim I_2$ are replaced by $(Q_1 + \delta Q_1) \sim (I_2 - \delta I_2)$ etc. The result is a system of linear equations containing the variables $\delta Q_1(1), \delta Q_1(2), \delta Q_2(1), \delta Q_2(2), \delta I_A(1), \delta I_A(2), \delta I_1(1), \delta I_1(2)$, and $\delta I_2(2)$, the solution of which can be obtained by application of the Gaussian elimination method. This set of solutions is valid for one instant of time, and is repeated at suitably spaced intervals until $I_A = 0$. The steady state solution, i.e., $dQ_1(N)/dt = 0$ and $dQ_2(N)/dt = 0$ in equations 2-33 and 2-34, provides the initial conditions for the transient solutions.

5. **Base Charges and Currents During Turn-Off**

We will now look at an example for turn-off. The intention is not to discuss the validity of the quantitative values obtained, but rather to observe the relative distribution of charges and currents as a function of time in both device sections.

Necessary input parameters are the doping profile, lateral dimensions of the device structure, lifetimes in the base regions $\tau_{B1}$ and $\tau_{B2}$, anode and source voltages $V_{ACS}$ and $V_{GCS}$, and the external resis-
tances $R_L$ and $R_C$.

For a typical triple diffused thyristor profile as shown on the right hand side of Figure 2-8 the surface concentrations and vertical dimensions are: $C_{NE} = 4 \times 10^{21}$, $C_{PB} = 3 \times 10^{18}$, $C_{NB} = 2 \times 10^{14}$, $C_{PE} = 3 \times 10^{18}$ (cm$^{-3}$), and $W_{NE} = 10$, $W_{PB} = 40$, $W_{NB} = 150$, $W_{PE} = 30(\mu)$, respectively.

The lifetime in the P-base is assumed $\tau_{B1} = 5\mu$s, whereas in the N-base $\tau_{B2} = 2.5\mu$s.

For lateral dimensions the following values are chosen (see Figure 2-8): $h_C = 200$, $h_G = 200$, $h_{CG} = 100(\mu)$ and the length of the device is $h_L = 4000\mu$. Further, $V_{ACG} = 200V$, $V_{GCS} = 10V$, $R_L = 250\Omega$, and $R_C = 100\Omega$.

Assuming for the collector time constants the low injection value

$$\tau_C = 2\tau_B \left[ \sinh^2 \left( \frac{W_B}{2L_B} \right) \right],$$

the one dimensional turn-off gain can be determined from

$$G_{gq} = \frac{1 + \tau_{C2}/\tau_{B2}}{1 - \left(\tau_{CL}/\tau_{B1}\right)\left(\tau_{C2}/\tau_{B2}\right)}$$

which can be shown to be identical to Equation 1-4.

Using the given input data and a turn-off gain of 10 we obtain the results plotted in Figure 2-10. Figure 2-10a shows the base charges. We notice, the excess charge in the P-base $Q_1(1)$ of section 1 is extracted fast, i.e., the N-emitter is shut off in this region. The
Figure 2-10b. Current Components vs. Time

Figure 2-10a. P-Base Charge and N-Base Charge vs. Time

Figure 2-10. Base Charges and Anode Current for Two-Section GTO-Thyristor Model during Turn-off (After M. Kurata)
charge in the N base $Q_2(1)$ is swept out into Section 2. Indeed $Q_2(2)$ increases initially and $I_{j2}(2)$, the current through the center junction of this section, is larger than the anode current $I_A(2)$ throughout the turn-off phase as seen in Figure 2-10b. Most of the anode current $I_A(1)$ injected into section 1 flows laterally to the center of section 2.

The important feature to notice is that, while the total anode current $I_A$ remains constant, the current in section 2 increases appreciably, and peaks about the time $Q_1(1)$ vanishes. This phenomena very clearly demonstrates the "squeezing" of the conduction area into a filament, similarly as assumed for D. Wolley's analytical model. In Kurata's approach, the charge in the N-base and conductivity modulation is included, however. Further, the time-dependent current waveform $I_A(t)$ by and large resembles that seen for actual devices, although a pronounced recombination tail (see Figure 2-5) is not produced.

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1 Of interest here is a one-dimensional analysis of turn-off phenomena by M. Naito et al. In this analysis an exact numerical solution of a full set of semiconductor equations including high injection effects is used and turn-off waveforms can be remarkably well simulated. Though this one-dimensional model does provide "a great deal of insight into the device's operation", it does not lend itself to aid in solving problems concerning current filamentation, and device failures due to excessively high local current densities during turn-off.

2 D'yakonov and Levinstein have made calculations "of the maximum value of the density of minority carriers in a filament and of their spatial distribution as a function of the turn-off gate current". Their theory ignores injection during the turn-off process, i.e., in Equation 1-5, the total charge $Q_{off}$ would be $Q(t_1)$, no further charge is added. A reference to time is absent. Thus, standing filaments, heating and burn-out failure cannot be predicted. Yet, the treatment in 80-2 points toward filament formation in support of Wolley's and Kurata's theories.
III. A HIGH SPEED, HIGH VOLTAGE EPI-BASE STRUCTURE

Progress in semiconductor technology and process control have made it possible to obtain reasonably tight tolerances for the physical parameters of multilayer semiconductor structures. Also, the possibility to use the digital computer for the artwork generation of photomasks have made it feasible to produce multiple patterns of different devices, side by side, on the same wafer. These facts were applied to investigate the dependence of the electrical characteristics for vertically identical GTO structures as a function of the horizontal geometry. They are described in this chapter in some detail.

A. Motivation

In the introduction it was mentioned that it would be desirable to combine the features of a transistor and a thyristor for obtaining an electronic switch offering advantages over either types of these conventional devices. The incentive to investigate such a transistor-thyristor hybrid becomes apparent by considering the internal loss, i.e., the power dissipation of a device chip as a function of the average current density.

Figure 3-1 illustrates the general trend. In this figure we observe two bands of rising power dissipation, one for transistors the other for thyristors, intersecting each other.

In particular, transistors have small losses at low current densities. The dissipation rises rapidly for average collector current densities exceeding 30A/cm².

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1A summary of preliminary results is presented in Reference 77-2.
POWER DISSIPATION PER OUTPUT AMPERE (WATTS/AMPERE) = (V)

NOTE:

THE (OPERATING) CURRENT DENSITY IS 10 TO 50 A/cm² FOR TRANSISTORS, 40 TO 200A/cm² FOR THYRISTORS

FOR VCE
- LOW VOLTAGE (60 - 90V)
- HIGH VOLTAGE (300 - 450V)

1500 V

TRANSISTORS

HIGH SPEED
Au DOPED
τ<1µs

LOW SPEED
NO Au
τ>10µs

THYRISTORS

Figure 3-1. Comparison of Power Transistors and Thyristors as an Electronic Switch showing Power Loss in “On” State

J is Average Collector Current Density and Anode Current Density for Transistors and Thyristors, respectively
It is obvious that for high voltage transistors the dissipation is more severe (left hand border of the region) than for low voltage types (right hand border). High voltage transistors have a relatively thick, high resistivity region. Base widening occurs and a pronounced quasi-saturation characteristic causes a marked increase of the collector saturation voltage and a rapid current gain fall-off. It should be noted that considerable base (drive) dissipation is added to the collector loss at high current densities, above 50A/cm².

In contrast, thyristors have some initial dissipation at low current densities because of the additional voltage drop due to the anode junction (0.7 to 0.9 volts for silicon). However, the internal voltage drop remains low as the current density is increased. The power dissipation for thyristors crosses the transistor regions in the neighborhood of 20 to 100A/cm² and then remains below that for higher current densities. The reason for this lower dissipation is of course the conductivity modulation of the high resistivity active regions due to electron-hole injection, and the absence of any gate dissipation in the conducting state due to the regenerative property. Further, it should be pointed out that because of the conductivity modulation, the power dissipation for thyristors is relatively independent of the (blocking) voltage capability.

The losses are effected by the minority carrier lifetime, however. For the on-state, the smaller the lifetime the greater the losses.
For high lifetimes, where diffusion is the major carrier transport mechanism, the lower limit of the dissipation region is approached. This fact applies to low frequency devices as indicated in Figure 3-1.

For high frequency devices the lifetime has to be decreased in order to minimize switching losses, for instance, through deliberate introduction of minority carrier traps by means of gold diffusion. Then, carrier transport is partially aided by a drift field, at the expense of an additional voltage drop. Thus, a higher dissipation results during the on-period, and the upper boundary of the thyristor region in Figure 3-1 is approached.

We may conclude from the foregoing discussion and Figure 3-1 that for operating a switch above average chip current densities of 50A/cm² with low on-state dissipation a thyristor-like structure is mandatory.

Figure 3-2 attempts to compare the power switching capability with respect to device cost (VA/$)¹ as a function of the frequency for a switch mode power supply using either thyristors or transistors.

We observe that it is possible to switch about 30,000 volt amperes per dollar with thyristors. However, applications are in general limited to low frequencies. Expensive, bulky components, including

¹It should be noted that the boundaries designating the VA/$ regions for thyristors and transistors were arrived at by taking the performance data and the sales price (100-999 quantities) for a large number of commercial and industrial devices from various manufacturers several years ago, and assuming arbitrarily a 40% margin. Though the price structure may have changed since that time, the relative relation is still valid.
Figure 3-2. Comparison of Power-Switching Capability with Respect to Cost as a Function of Frequency for Thyristors, GTO's, and Transistors
additional active devices for commutation are required. This results in excessive weight and high cost for the total system.

On the other hand, transistors will allow switching at higher frequencies. Yet, the device geometries are more complicated, voltages are limited, dissipation becomes a problem, as shown in Figure 3-1 before. A switching capability of about 1200 volt amperes per dollar is feasible at a frequency of 50kHz according to the transistor performance curve in Figure 3-2. There are fewer circuit elements necessary, and they are lighter and less expensive. The total system is simpler and cheaper, but the attainable volt ampere product per dollar is small. Therefore, very high power conditioning equipment usually employs thyristors operating at low frequencies, while small power supplies can be made with simple transistor circuits.

Again, a gate turn-off device suggests itself as an economical solution to improved performance. A higher power switching capability should be obtained approaching that of thyristors at frequencies similar to those realized with transistors as indicated by the dashed curve in Figure 3-2. A GTO can be controlled for turn-off as well as for turn-on from the gate electrode without commutating the output current and removal of the output voltage, making possible comparable circuit simplicity as for transistors.

B. Choice of Vertical Structure

For the design of the vertical structure of a GTO choices and compromises as are valid for transistors and thyristors have to be applied. The impurity profile comprises the superposition of the donor and
acceptor concentration achieved by means of multiple diffusion steps, epitaxial crystal growth, and the initial, high resistivity starting material.

1. **Gate Sheet Resistance**

Of paramount importance for a GTO is a low lateral resistance of the active, gated base region (see Figure 1-2c, pp. 8, and Equation 2-30, pp. 27) while maintaining a reasonably high gate-cathode breakdown voltage. The various options are depicted in Figure 3-3.

Figure 2-3a shows the conventional double diffused profile of the gated NPN section in terms of absolute donors and acceptors shown at left, and the resulting net impurity profile shown to the right. The gate conductivity as well as the gate breakdown voltage are very sensitive to variations of $x_{j1}$. Because of the graded base having a rapid concentration fall-off and high value at the intersection where $|N_A| = |N_D|$, one obtains usually a high base sheet resistance $R_{sp}$ and a low breakdown voltage $V_{Gbr}$.

Figure 3-3b shows an epitaxially grown gate layer and a diffused cathode, resulting in a "quasi" uniform base. Here, the dependence of gate sheet resistance and breakdown voltage on variations of $x_{j1}$ is less pronounced. Also, assuming the same base width ($x_{j2} - x_{j1}$) as for the illustration of Figure 3-3a, the square profile and a lower concentration crossover allow for a decrease in gate resistance and an increase in breakdown voltage.
Figure 3-3a. Graded Base (double diffused)

Figure 3-3b. Uniform Base (epitaxial)

Figure 3-3c. Inverted Base (epitaxial; ion implanted and diffused)

Figure 3-3. Impurity Concentration Profiles for GTO-SCR Structures
Finally, Figure 3-3c shows the case where initially a precise amount of gate impurities is implanted into the substrate. Then, a diffusion followed by an epitaxial deposition of a high resistivity portion forms a double gate layer (see also Figure 1-3, pp. 10). We may easily recognize that here the gate sheet resistance and breakdown voltage are very insensitive to variations of $x_{j1}$, provided the crossover remains in the high resistivity portion. For this inverted base profile gate sheet resistance and breakdown voltage are virtually independent.

A thorough investigation of this structure yielded excellent results for GTO's having a wide cathode (>20 mils) and a high gate breakdown voltage (>70 volt). However, the current gain of the NPN section is a rather strong function of the inverted profile. Further, if a low gate turn-off voltage (<30 volts) is one of the (circuit) requirements, the advantage offered by the inverted base concept is largely lost.

Therefore, the uniform base profile of Figure 3-3b emerges as the best compromise and was chosen for the experiments reported on.

The absolute value and importance of a close control of the gate sheet resistance is apparent from the variation of the main electrical characteristics such as the risetime, fall time, and forward voltage drop on this parameter, as is explicit from the data plotted in Figure 3-4. A change of ±20% in gate sheet resistance brings about a twofold change for these electrical characteristics, the lifetime in the N-base being kept constant. In particular, the data given in Figure 3-4 apply to a lifetime $\tau_n \approx 1.2$ microseconds and a gate sheet
Figure 3-4. Rise Time $t_r$, Fall Time $t_f$, and "On" State Voltage vs. Sheet Resistance of (gated) P-Base
resistance $R_{sp} \approx 180 \text{ ohms/square}$\textsuperscript{1} for $t_r(25) = t_f(125)$, where $t_r(25)$ is the risetime at 25°C and $t_f(125)$ is the fall time at 125°C.

2. Minority Carrier Lifetime

The second physical parameter with great influence on the electrical behavior of a GTO is the minority carrier lifetime, specifically the hole lifetime in the wide N-base. In Figure 3-5 we have plotted the rise time $t_r$, fall time $t_f$ and the forward voltage drop $V_T$ as a function of the average lifetime $\tau_n$ in the N-base over a range of 0.8 to 1.4 microseconds, again the gate sheet resistance being kept constant 75-1.

The adjustment of $\tau_n$ was achieved by varying the conditions for the gold diffusion 66-2, 72-1, 75-1. Other means of lifetime control, such as using platinum 75-2, 76-1 or employing electron and gamma irradiation 77-3 were not considered in this study.

It is of course desirable to keep the lifetime low in order to minimize the "tail" in the turn-off phase (see Figure 2-5). However, the lower limit is dictated by the affordable rise time $t_r$ and forward voltage drop $V_T$. A value for $\tau_n$ in the order of 1.0 microsecond, corresponding to a gold diffusion time of 2.0 hours at a temperature of 850°C, appeared to yield a reasonable optimum.

\textsuperscript{1}It should be noted that this represents a deliberate change from usual values. For a "standard" transistor base or thyristor gate $R_S$ is at least an order of magnitude higher, in the range of 1000-10000 ohms/square.
Figure 3-5. Rise Time $t_r$, Fall Time $t_f$, and "On" State Voltage vs. Average Lifetime (Au Doping) $\tau$ for GTO Thyristor^{75-1}
C. Choice of Horizontal Geometry (Interdigation)

The horizontal geometry was designed with the aim to obtain a meaningful evaluation of the GTO behavior as a function of the lateral turn-off distance $L_x$ (see Figure 2-3a), i.e., the cathode width. For this purpose it would be desirable to fabricate devices with different cathode widths simultaneously on the same wafer. All devices, however, should have the same size, approximately equal total cathode area, and a similar current distribution and heat flow pattern at high current densities. This was accomplished by making use of computer aided mask design procedures.\(^75-4\)

In particular, a program was written to create a 3x3 array of test geometries varying the cathode width over one order of magnitude. The computer program is attached as Appendix A, the test pattern is shown in Figure 3-6\(^1\). The area of the total array is 456x456 mils\(^2\), subdivided into 9 individual devices of 152x152 mils\(^2\). The cathode area was kept at about 4000 mil\(^2\); i.e., 15 to 20% of the total area was utilized as cathode. For cathode widths values of 20, 8, 4, and 2 mils were selected. The upper value was predetermined from experiments such that functioning devices (i.e., turn-off) could be obtained with negative gate voltages not exceeding 20 volts for average on-state current

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\(^1\)Figure 3-6 is a microphotograph of an array as obtained on a wafer in process, the white areas being the cathode sites opened in the masking oxide. The photomask itself is shown in Appendix B, pp. 147, Mask B-M03.
Figure 3-6. Test Array of GTO-Thyrists having Varying Cathode Widths
Clockwise from Upper Left: Test Pattern (Rectangular Cathode Sites) 1,2,3,4; Device (Tapered Cathode Fingers) 1,2,3,4

Microphotograph of Section of Actual Device Wafer at “Define Cathode Area” Processing Stage
(see Figure 3-7, Step 7, and Appendix B, Mask 03)
densities of about 50A/cm$^2$ ($\approx 250A/cm^2$ cathode current densities). The lower limit of 2 mils was set in order to keep the influence of lateral diffusions and sidewall effects reasonable. As can be seen in Figure 3-6, the 20 mil cathode (Pattern 1) is located in the upper left hand corner, followed clockwise by the 8 mil, 4 mil and 2 mil cathode design, respectively (Pattern 2, 3 and 4). At opposite locations within the array, matching counterparts for each pattern are placed having slightly tapered cathode sites, however (Device 1, 2, 3, and 4). The taper has two functions: a) it lowers voltage drops along the cathode fingers at high currents, b) it will shift the final current filament during turn-off toward the base of the finger in a controlled fashion. This predictable coordinate in the design is a prerequisite for an effective placement of anode shorts (see Figure 1-3) and it is of advantage for implementing the principle of dynamic ballasting as will be discussed in the following chapter.

The center pattern serves as a diagnostic device and alignment key.

D. Process for Device Fabrication

With the vertical structure chosen and the horizontal geometry determined a fabrication process was developed, the basic steps of which are outlined in Figure 3-7 on the following three pages. Figure 3-7 should be largely self-explanatory. The process contains several special features which are not found in a conventional device fabrication, however. In step 2 a low resistivity P-type layer is epitaxially grown
Starting Material, Si <[111]> axis
25 < ρ < 45 Ωcm, ~ 9 mil thick

2

epi-LAYER, P-TYPE

N-

Grow epitaxial gate layer; 0.25 Ωcm
1.2 mil - grind and etch backside
to total thickness of 7.2 mils

3

SiO₂

P

N-

Grow initial oxide, 12000 Å -
6 hrs. @ 1000°C

4

Define P⁺ gate-contact areas by
photolithography (see B-Mask 01)

5

BOROSILICATE

P⁺

P

N-

Deposit Boron diffusion source,
diffuse 1 hr. @ 1225°C -
form anode and gate-contact layer

6

SiO₂

P

N⁻

Strip Boron glass and oxide,
regrow new oxide, 12000 Å
6 hrs. @ 1000°C

7

SiO₂

P

N⁻

Define cathode areas in oxide
photolithographically (B-Mask 03)
Deposit $N^+$ Cathode from $\text{POCl}_3$ source, -5-15-20 min. @ 1200°C

Etch off phosphosilicate and $\text{SiO}_2$.
Drive in Boron and Phosphorus at 1265°C for 30 min. with simultaneous growth of final oxide; slow cool to 800°C @ 3°C/min.

Define Mesa grid in oxide (see B-Mask 06)

Etch Mesa about 3 mils deep using HF-HNO$_3$.
Individual devices with plane forward blocking junction are formed.

Remove oxide overhang (B-Mask 06)

Apply glass frit (IP820), fire and anneal glass in special two-zone furnace. Junction $J_2$ is now passivated.

Deposit protective low temperature oxide, synthesized from $\text{SiH}_4$ and $\text{O}_2$, over wafer top, ~6000 Å
Etch bottom oxide off, plate Gold on backside, diffuse in two-zone furnace using special conditions - \( t \sim 1.0 \, \mu s \)

Define cathode and gate contact areas in oxide (B-Mask 04)

Evaporate trimetal (Al-Ti-Ni), define contact pattern (B-Mask 07, inverse) sinter metal for 20 min. @ 425 °C

Separate devices by laser scribing; test dice

Assemble units on TO-3 stem, RTV coat and seal. Final stabilization bake: 24 hrs. @ 150°C.

Figure 3-7. Basic Process Outline for Fabrication of High Speed, Epi Base GTO-Thyristor (3 pages)
on a high resistivity N-type substrate. The sequence 13 to 15 shows a junction glass passivation compatible with a subsequent gold diffusion.

A typical resistivity profile along a cross section through a finished device (through the center of the device structure at step 16, or 17 with metal removed) is given in Figure 3-8. This profile was obtained by angle lapping a sample and taking two point probe - spreading resistance measurements \(^{74-2, 79-4}\). We see the cathode layer \(w_k\) on the left, having a very low resistivity of \(5 \times 10^{-3} \ \Omega \text{cm}\), the junction \(x_{j2}\) being located 11 microns from the top surface. The anode layer \(w_A\) is seen on the right hand side, the junction \(x_{j3}\) being located 24 microns from the bottom surface. The forward blocking junction \(x_{j2}\) separates the low resistivity gate layer (\(w_G = 19\) micron, \(\rho_{\min.} = 0.28\ \Omega \text{cm}\)) from the high resistivity N base (\(w_N = 126\) micron, \(\bar{\rho} = 36\ \Omega \text{cm}\)) which is the leftover portion of the initial substrate and is supporting the high breakdown voltage.

E. Results

Devices were fabricated in accordance with the process described in the previous section, and they were subjected to an extensive electrical evaluation.

In general, a distinct difference in behavior of devices having either parallel cathodes or tapered cathodes could not be established because of overlapping distributions for the various electrical parameters. Therefore, data and results presented in this section are applicable to both versions.
Figure 3-8. Two-Point Probe - Spreading Resistance Profile for High Frequency-Epi Base Structure
1. **Static Data**

Results of static data for one typical set of devices are given in Table 3-1. These devices come from the same wafer and were selected from the lower side of the $I_{gt}$ and $V_T$ distribution.

As can be seen the forward blocking voltage $V_{D_{RXM}}$ lies between 600 and 700 volts and is geometry independent. This value is surface-contour limited below the actual bulk breakdown. The gate-cathode breakdown voltage $V_{CK}$ of approximately 21 volts is also independent of geometry and is consistent for a planar junction with a profile as shown around $X_{j1}$ in Figure 3-8. The forward voltage drop $V_T$ and the gate trigger current are strongly dependent on cathode width. The variation of cathode area from device 1 to 4 is less than ±20%, and the increase in $V_T$ from 1.8 volt for the 20 mil cathode to 3.4 volts for the 2 mil cathode may point toward a somewhat non-uniform current distribution. This fact is contradicted by the increase in gate trigger current which is roughly proportional to the periphery indicating a reasonable uniform turn-on, which certainly points toward uniform conduction in the steady-state condition. The increase in $V_T$ with decreasing cathode width can be explained if one takes into account the gettering effect of the phosphorus cathode layer on the gold concentration $^{72-1}$ in the active gate region.

The wide cathode will more effectively getter toward the center of the cathode and establish a relatively uniform lifetime $\bar{\tau}$ beneath the cathode.
<table>
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<th>WCath. (mils)</th>
<th>VDRXM (V)</th>
<th>VGK (V)</th>
<th>VT (V)</th>
<th>Igt (mA)</th>
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</table>

Conditions for

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<th>0.2 mA</th>
<th>10 A</th>
<th>12 V</th>
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</thead>
<tbody>
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<td>IRGK</td>
<td>IT</td>
<td>VA</td>
<td></td>
</tr>
</tbody>
</table>

Table 3-1. Static Data for GTO Thyristor with Varying Cathode Width
The narrow cathode will be more dominated by edge effects, i.e., less gettering is experienced. Hence, a lower average lifetime $\tau$ is achieved leading to a shorter diffusion length and consequently to a higher forward voltage. This effect may be enhanced because of sidewall injection resulting in a higher average gate width $W_G$ reducing the effective transport factor even more.

2. **Major Test Conditions**

Switching characteristics were determined using a pulsed anode supply and a resistive load. The input-output wave forms are schematically given in Figure 3-9.

A turn-on pulse of 1 ampere with a 50 nanosecond rise time and an approximately 10 microsecond duration was applied to the gate. A negative turn-off pulse was applied from a voltage source about 50 microseconds later. Generally, an inductance was put in series with the input. The time duty cycle was kept below 2.5% in order to avoid internal device heating. All data presented were taken with an anode supply voltage $V_{DD}$ of 200 volts, and without a snubber network or a voltage clamp across the output of the device under test.

3. **Turn-On**

The turn-on characteristics are shown in Figure 3-10. The delay time $t_d$ is less than 50 nanoseconds and the rise time is about 500 and 400 nanoseconds, for 25°C (Figure 3-10a) and 125°C (Figure 3-10b), respectively.

The surprising feature is that there is virtually no dependence of rise time $t_r$ on cathode width. One would expect that device 1 with a 20 mil wide cathode exhibits the longest $t_r$. However, quite contrary, the
Figure 3-9. Input-Output Waveforms for GTO Thyristor in Anode Load Configuration
Figure 3-10a. Gate Turn-On Current $I_{GT} = f(t)$
Anode Load Current Response $I_A = f(t)$

Figure 3-10b. [$I_{GT}, I_A] = f(t)$

Figure 3-10. Turn-On Characteristic of High-Frequency GTO-Thyristor at 25°C and 125°C
Device 1, 2, 3, and 4
trend is actually reversed. Device 4 with a 2 mil cathode width has the longest rise time as evident from the traces in Figure 3-10a.

The reason for this must be a differing spreading velocity in the individual devices. Since the spreading velocity is proportional to the square root of the lifetime, $v_s \propto \sqrt{\tau}$, we may conclude that the lifetime beneath the active gate decreases with decreasing cathode width. This fact is consistent with the observations made about the variations in forward voltage drop $V_T$ in Section 3, thus confirming a more pronounced gettering of gold under the wider cathodes.

Lastly, we notice in Figure 3-10 that the turn-on condition for an output current $I_A = 8A$ and for the duration of the input pulse represents the equivalent of a forced current gain $h_{FE} = 8$, $h_{FE}$ being the DC-current gain, as is customarily defined for transistors.

4. **Turn-Off Characteristics (General Waveforms)**

The turn-off waveforms are shown in Figure 3-11. These waveforms represent a typical example of the input-output relationship for currents and voltages as a function of time during the turn-off phase.

In Figure 3-11a we see the negative gate current $I_{gq}(t)$ and the corresponding anode current response $I_A(t)$ at the gate terminal and anode terminal, respectively. The coinciding input voltage $V_{gq}(t)$ and the output voltage response $V_A(t)$ are traced in Figure 3-11b. The application of the turn-off pulse, $t=0$, occurs at the first vertical grid line on the left hand side of the display.
Figure 3-11. Turn-Off Characteristics for High-Frequency GTO-Thyristor (Example of Waveforms)
The gate current $I_{gq}$ rises approximately linear during the whole storage phase $t_s$ ($\approx 1.4$ microseconds), while the anode current remains constant ($I_A = 8A$). The slope of the gate current is mainly a function of the gate series inductance $L_{gs}$ ($\approx 4.6\mu H$) and the open circuit-gate source voltage $V_{goc}$ ($-10V$). The maximum gate current $I_{gq\ max}$ ($\approx 2A$) is reached after the storage phase is completed and the anode current is in the fall period just before the current traces intersect each other (Figure 11a).

At that point the cathode junction is reverse biased and has assumed the gate source voltage $V_{goc}$ ($-10V$); the voltage across the inductance being zero.

The fall of the anode current $I_A$ is now aided by the reversal of the polarity at the gate inductance $L_{gs}$, and the additional negative turn-off voltage which is developed at the gate (Figure 11b), while the stored energy in $L_{gs}$ is being discharged. Actually, it may be noticed that the gate cathode junction is driven into breakdown acting as a voltage clamp for approximately 0.3 microseconds. During this period the negative gate current $I_{gq}$ decreases to zero with a slope determined by $L_{gs}$ and the gate breakdown voltage $V_{CBR}$ ($\approx 22V$) and then the gate voltage assumes the open-circuit value $V_{goc} = -10V$. The small tail of anode current decays simultaneously and the center junction $J_2$ recovers and becomes reverse biased. Thus, the anode voltage $V_A$ assumes the supply voltage $V_D = 200V$. The overshoot of about 100 volts and the ringing is a consequence of some lead inductance in the load circuit, interacting with the device.
output capacitance. Since the maximum value of the transient voltage remained well below the actual junction breakdown of \( J_2 \), no efforts were made to reduce this parasitic inductance for the measurements presented here.

5. The Influence of the Gate Series Inductance

An inductance in series with the gate proved to be an important element for safely operating a GTO. In Figure 3-12 we see the turn-off characteristics for a device type 3 (4 mil cathode). Curve 1 shows the gate current and anode current without an inductance connected between the gate and the voltage source. For curve 2 and 3 an inductance of 4.6 microhenry and 11.8 microhenry were inserted, respectively. The open circuit gate voltage was \( V_{goc} = -15 \) volts in all cases.

As can be seen in curve 1 the storage time \( t_s \) lasts about 0.5\( \mu \)s and the fall time \( t_f \) only 0.1\( \mu \)s. The peak gate current \( I_{gq \text{ max}} \) reaches 4 amperes, i.e., the turn-off gain \( G_{gq} = 2 \). Further, as the (average) anode current \( I_A \) reaches the break at approximately 3% of the On-state current, the negative gate current breaks also. The "tail" current in the anode is identical to the gate current, the decay time being about 0.5\( \mu \)s. This is a situation as described in Chapter II and shown in Figure 2-5. At the break, the cathode has shut off and is reverse biased, the negative voltage being smaller than the gate-cathode junction breakdown voltage.

For the curves 2 and 3 the storage time \( t_s \) increases while the peak gate current \( I_{gq \text{ max}} \) decreases. The falltime, however, is at least as
GATE SERIES INDUCTANCE \( (L_{gs}) \)

1. \( 0 \mu H \)
2. \( 4.6 \mu H \)
3. \( 11.8 \mu H \)

\( t = 0.5 \mu s / \text{DIV.} \quad T = 25^\circ C \quad I = 1A / \text{DIV.} \)

Figure 3-12. Turn-Off for GTO-Thyristor \([I_A, I_{gq}] = f(t)\) with Gate Series Inductance \(L_{gs}\) as Parameter Device Type 3 (4-mil Cathode)
fast as in the case for curve 1, i.e., $t_f = 0.1\mu s$. The break and tail for the anode current $I_A$ remain relatively unchanged.

The significant difference is in the waveform of the gate current, the magnitude of which stays always above the anode tail current. This fact indicates that cathode current flows in the reverse direction, the entire gate-cathode junction $J_\perp$ is in avalanche breakdown (as shown in Figure 3-11b before) and the GTO stays safely turned off.

It must be emphasized here that the snap into breakdown by means of an inductive kick is rather different from the local edge breakdown caused by the lateral voltage drop due to $I_{gq}$ flowing through the resistive gate region beneath the cathode.

In the first case the electron-hole plasma is being rapidly extinguished once it has been squeezed into a filament during the storage phase as evidenced from the negative potential built-up across the gate-cathode terminal (see Figure 3-11b).

In the latter case the electron-hole plasma keeps flowing in a partially squeezed condition and a negative potential is never developed across the gate-cathode terminal because the center section of the cathode junction remains forward biased (see Figure 1-2c, pp. 8). Thus, a hot spot forms and eventual device failure results due to local burn-out.

Turning our attention now to the peak reverse gate current, for instance for curve 3, we notice that this value is now 2 amperes rather than 4 amperes as for curve 1. The turn-off gain is here increased to
$C_gq = 4$, while the internal lateral voltage drop is kept to one-half of that developed in case 1. Also, the negative gate bias is equal to the highest possible voltage, namely the cathode breakdown voltage $V_{Gbr} = -23V$, while the open circuit drive voltage, $V_{goc} = -15V$, can be considerably lower.

It is obvious that it would be much more difficult to achieve turn-off if the maximum gate current would be limited through an added external resistance. The turn-off voltage available would be much lower than the open circuit voltage at the critical point where the current density in the device has reached a local maximum. In addition, a portion of the turn-off energy delivered by the gate drive source is needlessly dissipated in the series resistor.

The above discussion leads to the following summary about the influence of a gate series inductance for turn-off of a GTO:

a. an increased turn-off gain can be obtained,
b. lower lateral internal voltage drops are encountered,
c. the applied source voltage can be lower and is not as critical, and
d. an increase in storage time must be tolerated.

In general, with the application of a gate series inductance a safe turn-off condition can be maintained, and as an indirect benefit a smaller device may be employed for generating the drive function to achieve turn-off.
6. Dependence on Cathode Width

The effect of the cathode width on the turn-off behavior of a GTO is of great interest. Figure 3-13 depicts the input current-output current time response of devices with a 20 mil, 8 mil, 4 mil, and 2 mil wide cathode, curves 1, 2, 3, and 4, respectively.

The input circuit and the drive condition as well as the output supply voltage and load resistance were kept constant \( (L_{gs} = 4.6\mu H, V_{goc} = -15V, V_D = 200V, R_L \approx 25\Omega) \).

We observe that the storage time \( t_s \) and the fall time \( t_f \) are pronounced functions of the cathode width. The storage time increases from 0.7 microseconds for the 2.0 mil cathode (curves 4) to 1.5 microseconds for the 20 mil cathode (curves 1). The fall time changes from approximately 0.1 microseconds for the 2 mil cathode to 0.6 microseconds for the 20 mil cathode. The turn-off gain remains relatively unchanged.

These results differ from previously published data by Kao and Brewster\(^{74-3}\) who report that both storage time \( t_s \) and turnoff time \( (t_s + t_f) \) "were much the same and did not depend on cathode width". Their case, therefore, implies that one-dimensional conditions existed, i.e., the cathode width \( L_x < 2L_n \). This would require a minimum lifetime \( \tau_p \approx 50 \) microseconds for the maximum cathode width of 25 mils that was used in Reference 74-3. Such a long lifetime causes a large recombination tail (see Figure 2-5, pp. 28). Consequently, this
CATHODE WIDTH

1 = 20 MIL  3 = 4 MIL
2 = 8 MIL  4 = 2 MIL

\( t = 0.2 \ \mu \text{s}/\text{DIV.} \ T = 25^\circ \text{C} \)

\( I = 1 \text{A/DIV.} \ V_{goc} = -15 \text{V} \)

\( Lgs = 4.6 \ \mu \text{H} \)

Figure 3-13. Turn-Off Behavior of GTO-Thyristor
with varying Cathode Width \(|I_A, I_{gq}| = f(t)\)
\( W_K = L_X \) as Parameter
device would suffer from excessive switching dissipation and be vulnerable to retriggers. These conditions can only be remedied by adding a polarized snubber network in parallel to the anode, and high speed operation and circuit efficiency are greatly impaired, however.

7. Turn-Off Criteria and Current Densities

Considering the waveforms obtained in this work for varying cathode width some important turn-off criteria may be established.

Examining the $I_A$-traces depicted in Figure 3-13 during the fall period we detect that for devices 2, 3, and 4 the slope $dI_A/dt$ increases up to the tail break point. Also, the maximum gate current is reached only after the anode current has substantially decreased.

That does not hold for Device 1. Here the slope of $I_A$ goes through an inflection at about 4A decreasing with time, i.e., the second derivative of anode current with respect to time $d^2I_A/dt^2$ becomes negative. Also, the gate current displays a broad maximum and peaks long before the anode current is intersected. From such a waveform we may infer that in this case for the 20 mil wide cathode the lateral base resistance gains dominance toward the end of the storage phase. Thus, the gate source voltage is marginal for turn-off and a pronounced inductive voltage spike as for instance seen in Figure 3-11b is absent. A slight decrease in turn-off voltages or increase in temperature will cause failure to turn-off.
The difference between safe turn-off and potential turn-off failure becomes rather clear if we plot the ratio of anode current to gate current \( \frac{dI_A}{dI_{gq}} \) against time during the turn-off phase as is shown in Figure 3-14 using the waveshapes of Figure 3-13.

Without a gate series inductance turn-off, i.e., the storage phase, will commence with infinity at \( t = 0 \), where the gate current is \( I_{gq} = 0 \) and the anode current \( I_A = I_T \), and then monotonically decrease to unity at the tail break, from which point anode current and gate current are identical (see Figure 2-5 and 3-12 trace 1).

With the gate series inductance the differential turn-off gain \( \frac{dI_A}{dI_{gq}} \) behaves similar from \( t = 0 \) throughout the storage phase and fall phase. But at the tail break the differential turn-off gain is now much less than unity and it approaches unity for \( I_A \to 0 \) and \( I_{gq} \to 0 \) in an asymptotic fashion. This behavior constitutes a safe turn-off condition as is exhibited by devices 2, 3, and 4 (8, 4, and 2 mil cathode).

In contrast for device 1 (20 mil cathode) the differential turn-off gain never reaches unity during the fall time but rather shows an increase of \( \frac{dI_A}{dI_{gq}} \) toward the end of the fall time signaling instability. The peak will grow or move out in time with either a slight increase in local temperature or decrease in gate source voltage and eventually cause turn-off failure as mentioned above.
The inserted table in Figure 3-14 gives the "conventional" turn-off gain $G_{Gq}$, the ratio of the on-state current $I_T$ to the maximum negative gate current $I_{Gq\max}$, during turn-off. As should be noted $G_{Gq}$ is identical for device 1 and device 4, and it is clearly demonstrated by the given example that the use of this electrical parameter in the literature may lead to erroneous conclusions unless additional information is provided.

The danger of destruction existing for a GTO is evident from 1st order estimates of current densities which may develop locally during turn-off. Table 3-2 shows the (worst case) peak current densities for the four geometries investigated in this study. The assumptions for the given values of $J_{o(max)}$ are that the total on-state current $I_T = 8A$ is flowing through an area of width $2L_n$, and the lifetime $\tau$ beneath the cathode is of the order of 1 microsecond.

One sees immediately that for a uniform line turn-off over the length of the cathode sites "reasonable" conditions exist (two-dimensional case: $J_{o(max)}2d$ ranging from 462 A/cm$^2$ to 3340 A/cm$^2$). Unfortunately, these lines will not stay uniform, but rather degenerate to spots having a diameter of $2L_n$. Therefore, extreme conditions are highly probable (three-dimensional case: $J_{o(max)}3d$ ranging from 5000 A/cm$^2$ to 87000 A/cm$^2$!). Though counteracting mechanism tends to limit $J_o$, i.e., Auger effects and bandgap narrowing, the necessity of narrow cathodes and careful design of turn-off circuits becomes rather explicit.
Figure 3-14. 
Differential Turn-Off Gain \( \frac{dI_A}{dI_{gq}} \) vs. Time for GTO Thyristors having different 
Cathode Widths under Identical Input and 
Output Conditions; showing safe Turn-Off 
for Device Types 2, 3, 4 (2, 4 and 8 mil cathode, 
respectively), and indicating Onset of Turn-
Off Failure for Device Type 1 (20 mil Cathode). 
\( V_D=200 \text{ V}, I_T=8 \text{ A}, V_{goc}=-15 \text{ V}, \) 
\( L_{gs}=4.6 \mu \text{H}, T=25^\circ \text{ C} \) (for \( I_A, I_{gq}=f(t) \)).
See Figure 3-13.
8. **Influence of Negative Gate Bias and Temperature**

Figure 3-15 shows the turn-off characteristic of Device 3 (4 mil cathode) for varying open-circuit gate voltages $V_{goc} = -20V$, -15V, -10V, and -5V, respectively, at 250°C. The gate series inductance $L_{gs} = 4.6$ microhenry, the anode supply voltage $V_D = 200V$.

While curves 1, 2, and 3 ($V_{goc} = -20V$, -15V, and -10V) show that turn-off is input circuit dominated, we see that for curves 4 ($V_{goc} = -5V$) lateral series resistance and continuing current injection start to become dominant. However, even though the storage phase becomes significant ($t_s > 2\mu s$) and the fall time starts to increase noticeably ($t_s \sim 0.3\mu s$), the criteria for safe turn-off as defined in Section 7 are still met.

In Figure 3-16 we see the temperature dependence of the same device in the range from 25°C (curves 1) to 125°C (curves 4). The time scale is here expanded to 0.2\mu s/Div, $L_{gs} = 4.6\mu H$, and $V_{goc} = -15V$.

The turn-off at 125°C is excellent. Generally, the behavior is as would be expected, i.e., storage time, fall time, and tail contribution increase with temperature consistent with a lifetime increase. The slope of the gate current during the tail phase increases because the gate breakdown voltage $V_{Gbr}$ becomes larger due to changes in avalanche multiplication. A very qualified statement can be made for the decrease in turn-off gain $\alpha'_{gq}$. With increasing temperature the $\alpha'$s of the component transistor sections become larger. Therefore, it becomes harder
NEGATIVE GATE BIAS \( (V_{goc}) \)

1 = -20V  2 = -15V  3 = -10V  4 = -5V

\( t = 0.5 \mu s / \text{DIV.} \)  \( T = 25^\circ C \)  \( I = 1A / \text{DIV.} \)

Figure 3-15.
Turn-Off Behavior of GTO-Thyristor for Varying Negative Gate Bias \([I_A, I_{gq}] = f(t)\), \( V_{goc} \) Parameter
Device Type 3 (4-mil Cathode)
Figure 3-16.
Turn-Off for GTO-Thyristor dependent on
Temperature [I_A, I_{gq}]=f(t), T Parameter
Device Type 3 (4-mil Cathode)
to force the condition for the loop gain $G_L$ to be less than unity everywhere over the entire device area (see Equation 1-3, pg. 6).

Of interest in the characterization of the GTO turn-off behavior is to see how the gate source voltage effects the fall time for the various geometries, because the switching dissipation is largely determined by this parameter. The fall time $t_f$ is plotted as a function of the negative gate source voltage at 125°C for Device Types 3, 2, and 4. The devices with the 4 mil and 8 mil cathode width could not safely be operated for $V_{goc} < 10V$. Considering the results plotted in this graph and the forward voltage drop $V_T$ (see Table 3-1, pp. 62) Device Type 3, operated at $V_{goc} = -15V$, appears to be a proper choice to achieve optimum performance.

9. Turn-Off For Varying Loads

Figure 3-18 shows the turn-off characteristics of Device 3 for varying anode loads at 125°C. The load resistance was changed over a range from $R_L \sim 100\Omega$ ($I_T = 2A$) to $R_L \sim 16.7\Omega$ ($I_T = 12A$). The anode supply voltage $V_D = 200V$, and the input drive conditions ($V_{goc} = -15V$, $L_s = 4.6\mu H$) were kept constant. The current scale is in this case 2A/Div.

Curves 1 show a circuit determined (forced) current gain ($I_T/I_{gq\ max}$) of unity. Both, turn-off gain and storage time increase with increasing current. The turn-off gain at $I_T = 12A$ is approximately 3.3. At that point, turn-off is still well behaved to assure safe operation. It may be also noticed that the fall time is relatively independent of anode
Figure 3-17.
Fall Time for GTO-Thyristor as Function of (Open Circuit) Gate-Source Voltage
$\tau_f=f(V_{goc})$, $W_k=L_x$ as Parameter
2=Device Type 2 (8-mil Cathode)
3=Device Type 3 (4-mil Cathode)
4=Device Type 4 (2-mil Cathode)
LOAD CURRENT ($I_A$)

1 = 2 A  
2 = 4 A  
3 = 6 A  
4 = 8 A  
5 = 10 A  
6 = 12 A  

$t$ = 0.5 $\mu$s/DIV.  
$T$ = 125°C  
$I$ = 2 A/DIV.

Figure 3-18.  
Turn-Off Characteristics for GTO-Thyristor with  
Varying Load Current. Input Source ($V_{goc}$, $Lgs$  
Kept Constant) [$I_A$, $I_{gq}$]=$t(t)$, $R_L$ Parameter  
Device Type 3 (4-mil Cathode)
current, $t_f \sim 200$ nanoseconds.

Figure 3-19 is a graph characterizing turn-off gain and storage time as a function of load current for the family of curves of Figure 3-18 and conditions given above.

10. **Switching Performance**

The data plotted in the graphs of Figures 3-20, 3-21, and 3-22 characterize the switching behavior for Device 2 (8 mil cathode), Device 3 (4 mil cathode) and Device 4 (2 mil cathode), respectively, over the temperature range from 25°C to 125°C.

Figures 3-20a, 3-21a, and 3-22a show the storage time $t_s$ with $V_{goc}$ as parameter. Device 2 could not be operated at $V_{goc} = -5V$, Device 3 functioned safely up to +65°C for $V_{goc} = -5V$. Device 4 operated safely over the full range for this low negative gate bias.

In Figures 3-20b, 3-21b, and 3-22b the rise time $t_r$ and the fall time $t_f$ are graphed. The current at the "tail break" is also given in (%$I_T$). For instance, Device 3 had an initial tail current of 2%$I_T$, i.e., 160mA @ 65°C.

The rise time is identical for all devices, about 380 nanoseconds at 125°C. At lower temperatures, however, the rise time becomes longer for devices with narrower cathodes.
Figure 3-19.
Turn-Off Gain and Storage Time for GTO Thyristor with Varying Load Current
Input Source ($V_{G0C}$, $L_{GS}$) Kept Constant
Device 3 (4-mil Cathode)
Figure 3-20a. Storage Time $t_s = f(T)$

Figure 3-20b. Rise Time and Fall Time $[t_r, t_f] = f(T)$

Figure 3-20.
Switching Performance of GTO Thyristor as Function of Temperature. Device 2 (8-mil Cathode)
Conditions: $I_T = 8$ A = constant, $V_D = 200$ V, $L_{gs} = 4.6$ $\mu$H
Figure 3-21a. Storage Time $t_s = f(T)$

Figure 3-21b. Rise Time and Fall Time $[t_r, t_f] = f(T)$

Figure 3-21.
Switching Performance of GTO-Thyristor as Function of Temperature. Device 3 (4-mil Cathode)
Conditions: $I_T = 8$ A=constant, $V_D = 200$ V, $L_{gs} = 4.6$ $\mu$H
Figure 3-22a. Storage Time $t_s = f(T)$

Figure 3-22b. Rise Time and Fall Time $[t_r, t_f] = f(T)$

Figure 3-22.
Switching Performance of GTO-Thyristor as Function of Temperature. Device 4 (2-mil Cathode)
Conditions: $I_T = 8$ A $=$ constant, $V_D = 200$ V, $L_{gs} = 4.6 \mu$H

Static Data
- $V_{DRX} = 660$ V
- $V_{GK} = 23$ V
- $I_{gt} = 167$ mA
- $V_T = 3.4$ V @ 10A
- $V_{goc} = -5$ V
- $V_{goc} = -10$ V
- $R_{gs} = 0$ $\Omega$
- $L_{gs} = 4.6 \mu$H
The trend for the fall time is just in the opposite direction. The narrower the cathode width, the shorter \( t_f \) becomes. In Figure 3-22b we notice that for a gate source voltage larger than 10V the fall time becomes practically independent of temperature, the fall time \( t_f = 200 \) nanoseconds @ \( V_{goc} = 20V \).

The peak gate current \( I_{gqm} \) required to obtain the switching times plotted in Figures 3-20 to 3-22 is given in Figure 3-23a for Device 2, in Figure 3-23b for Device 3, and in Figure 3-23c for Device 4, respectively. As can be seen lowest current \( I_{gqm} \approx 1.5A \) is required for Device 4 (2 mil cathode) at \( V_{goc} = -5V \), corresponding to a turn-off gain \( G_{gq} \approx 5.3 \), for a storage time \( t_s \approx 2.7\mu s \) (Figure 3-22a) and a fall time \( t_f \approx 0.42\mu s \) (Figure 3-22b) @ \( T = 125^\circ C \).

Considering now the performance of Device 3 for example, it is noteworthy that simultaneously a fast rise time of \( \approx 0.4\mu s \) was obtained and the gate trigger current of 50mA as well as the on-state voltage of 2.4V could be kept rather low. Usually, a device with such excellent turn-off characteristics would have a rise time of \( \approx 1.5\mu s \), a gate trigger current of \( \approx 300mA \), and an on-state voltage of \( \approx 4V \). The reason for the desirable combination of fast \( t_r \) and \( t_f \), and low \( I_{gt} \) and \( V_T \) can be found if we investigate the spreading resistance profile of such devices more closely by probing the structure along several vertical passes 74-2, 79-4.
Figure 3-23. Peak Gate Current Required for Turning Off a GTO Thyristor as Function of Temperature and Negative Gate Bias
Conditions: \( I_T = 8 \text{ A} \) constant, \( V_D = 200 \text{ V} \), \( L_g = 4.6 \mu\text{H} \)
11. Gold Distribution and Life Time

Figure 3-24 shows the vertical spreading resistance variation of the device taken through the p+-gate toward the anode along CD (see insert). The center junction is located about 36µ from the surface. The resistivity throughout the N−-region is >1000Ωcm. The entire N-base is upconverted from its initial value of approximately 30Ωcm. Thus, we assume that the Au-concentration is about 1.5x10^{14} corresponding to a life time $\tau_n \sim 0.5\mu s$ in the n-base. The p-base in this region will have an even lower life time value.

Now we turn to Figure 3-25 in which the spreading resistance is taken through the N+ cathode, again vertically toward the anode along pass AB. The interesting fact here is that in the vicinity of the center junction, the starting resistivity is preserved (30Ωcm) and upconversion becomes noticeable only about 50µ into the n-base with a pronounced increase in direction of the anode. The difference in this spreading resistance profile from that of Figure 3-24 suggests that Au was gettered by the heavily doped phosphorus emitter above this region. As a consequence the active gold distribution in the device is such that the life time is kept high (>1.0µs) in the p-base and in the n-base adjacent to the center junction while it is low ($\sim 0.5\mu s$) in the vicinity of the anode. The high life time keeps the npn gain reasonably high and accounts for the low $I_{gt}$ and the fast $t_r$. 
The low life time limits the anode emitter efficiency and also causes a rapid recombination of the stored charge in the n-base, the majority of which is located close to the anode junction\textsuperscript{79-3}. Thus, the tail-effect is minimized.

<table>
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<th>Device</th>
<th>A\textsubscript{cath} (mm\textsuperscript{2})</th>
<th>L\textsubscript{x}/L\textsubscript{n}</th>
<th>J\textsubscript{0(max)2d} (A/cm\textsuperscript{2})</th>
<th>#Sites</th>
<th>L\textsubscript{y}/L\textsubscript{n}</th>
<th>J\textsubscript{0(max)3d} (A/cm\textsuperscript{2})</th>
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<td>25.4</td>
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<tr>
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<td>12</td>
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<td>82</td>
<td>10.8</td>
<td>5000</td>
</tr>
</tbody>
</table>

Table 3-2. Peak Current Density for GTO during Turn-off.
- \(J\textsubscript{0(max)2d}\) = two-dimensional; uniform line turn-off
- \(J\textsubscript{0(max)3d}\) = three-dimensional; single spot/site turn-off
- \(J\textsubscript{cath}\r{\sim} 300\ A/cm\textsuperscript{2}, J\textsubscript{(on)}\r{\sim} 65\ A/cm\textsuperscript{2}\) for total chip. Ln\r{\sim} 40\ μ
Figure 3-24.
Two-Point Probe Spreading Resistance Profile (C-D) through P⁺ Gate showing Total Up Conversion of N⁻ Region.
(Insert shows Schematic of Cross Section and Probe Travel Pass)
Figure 3-25.  
Two-Point Probe Spreading Resistance Profile (A-B) through N⁺ Cathode Showing Partial Up Conversion of N⁻ Region in Direction of P⁺ Anode  
(Insert shows Schematic of Cross Section and Probe Travel Pass)
12. **Power Switching Capabilities**

With the results presented in the foregoing sections and discussions on safe operations it is now possible to evaluate the power switching capability of the high speed-high voltage Epi-base structure.

The total energy absorbed per cycle in a device is in general

\[
E_{\text{D tot}} = \int_{0}^{T} I_A(t)V_A(t)dt + V_{T T} \left[ (F_D T) - (t_r + t_{f1}) \right] \\
+ \int_{t_s}^{t_{f1}} I_A(t)V_A(t)dt + \int_{t_{f1}}^{t_{f2}} I_A(t)V_A(t)dt \\
+ \int_{0}^{t_{p(\text{on})}} I_G(t)V_G(t)dt + \int_{t_s}^{t_{p(\text{off})}} I_{gq}(t)V_{gq}(t)dt \\
\]

where \( F_D \) is the duty factor and \( T \) is time of one total period; \( t_{p(\text{on})} \) is the duration of the "On" pulse, and \( t_{p(\text{off})} \) is the duration of the "Off" pulse.

We choose as an example Device 3 at \( T = 125^\circ\text{C} \) and evaluate the integrals in Equation 3-1 with the aid of Figures 3-10b, 3-11, 3-16, and Figure 3-21. Operation is assumed for \( I_p = 8\text{A} \) and \( V_D = 400\text{V} \), the pulse duration for turn-on and turn-off is set for \( t_{p(\text{on})} = t_{p(\text{off})} = 3\mu\text{s} \). The load is assumed to be \( R_L = 50\Omega \), resistive. The turn-on
gate current is $I_{G(on)} = 1.0\text{A}$ and $V_{G(on)} = 1.0\text{V}$. For turn-off $V_{goc} = -1.5\text{V}$ and a series inductance $L_{gs} = 4.6\mu\text{H}$ connects the gate.

The turn-on energy, assuming a quasi linear change of current and voltage in the output, is then

$$E_{t(on)} = E_G(tr) + E_A(tr)$$  \hspace{1cm} (3-2)

$$E_G(tr) = V_{G(on)} I_{G(on)} t_{p(on)}$$  \hspace{1cm} (3-3)

$$E_A(tr) = \frac{1}{4} V_{D} I_{A} t_{r}$$  \hspace{1cm} (3-4)

The turn-off energy is

$$E_{t(off)} = E_G(t_{f1}) + E_G(t_{f2}) + E_A(t_{f1}) + E_A(t_{f2})$$  \hspace{1cm} (3-5)

$$E_G(t_{f1}) + E_G(t_{f2}) = \frac{1}{2} V_{goc} I_{gqm} t_{s} + \frac{1}{2} L_{gs} I_{gqm}^2$$  \hspace{1cm} (3-6)

$$E_A(t_{f1}) = \frac{1}{4} V_{D} I_{A} t_{f1}$$  \hspace{1cm} (3-7)

$$E_A(t_{f2}) = V_{D} k I_{T} \tau_{pA}$$  \hspace{1cm} (3-8)

where $k$ is the ratio of "tail break current" to on state current and $\tau_{pA}$ is the hole life time in the vicinity of the anode.
The resultant components of absorbed energy/cycle are given in Table 3-3.

<table>
<thead>
<tr>
<th>$E_{G(\text{tr})}$</th>
<th>$E_{A(\text{tr})}$</th>
<th>$E_{G(t_f1)}$</th>
<th>$E_{G(t_f2)}$</th>
<th>$E_{A(t_f1)}$</th>
<th>$E_{A(t_f2)}$</th>
<th>$E^*_{\text{on}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>320</td>
<td>27</td>
<td>21</td>
<td>160</td>
<td>96</td>
<td>166</td>
</tr>
</tbody>
</table>

Table 3-3 Components of Dissipated Energy/Cycle in $\mu$Joules for GTO (Device Type 3).

$I_A = 8A$, $V_D = 400V$, $T_j = 125^\circ C$, Res. Load,

*) $f = 50kHZ$, 50% Duty Cycle

Summing up all components, the total energy per cycle is then $E_{\text{tot}} = 793 \mu$Joule. It follows that for 50kHz the power dissipation is approximately 40 watts. The thermal resistance for this device mounted in a TO-3 case is at worst $\Theta = 1.2^\circ C/Watt$. Therefore, the maximum allowable case temperature is 78°C.

Above assumptions and calculations show that this device is capable of switching a load of 1560 Watts at a frequency of $f = 50kHZ$.

Turning back to the discussion about power switching capability with respect to cost (pp. 44), we are now able to fit this device in the graph of Figure 3-2. The result is shown in Figure 3-26. There, a vertical "cost line" is added at the 50 kHz point on the abscissa and we see that in order to reach the projected boundary (broken line) of the GTO-Thyristor region, the cost per device would have to be 25¢.
Figure 3-26. Comparison of Power-Switching Capability with Respect to Cost as a Function of Frequency for Thyristors, GTO's, and transistors (The cost Line at f = 50 kHz indicates where the GTO Type D3 would be in this graph for 400 V, 8 A operation using the data of Table 3-3)
The $1.00 cost intersection is certainly realistic if one is reminded that this graph was generated from a survey taken several years ago (see Footnote, pp. 44).

From the switching times obtained it is certainly possible to operate this device at 100kHz. Therefore, if the case temperature can be held at a maximum temperature of 38°C ($P_D \sim 74\text{W}$) the cost line can be moved up to 100 kHz. It is apparent that for these considerations the GTO is quite compatible with transistors as an economical power switch.
IV. SERIES SCHOTTKY BARRIERS AND DYNAMIC BALLASTING

In this chapter principles for improvements of the state-of-the-art in GTO devices are described in a brief and general manner. Experimental proof is given for new concepts which were introduced by the author. These concepts deal with anode shorts and series Schottky Barriers, and measures to defocus current filaments (Dynamic Ballasting).

A. Anode Shorts and Schottky Barriers

An effective method of improving turn-off characteristics of GTO's is to introduce anode shorts 75-1, 78-1. If these shorts are dimensioned properly and are placed most remote from the gate contact, the excess minority carrier charge in the n-base will be partially removed through those shorting resistances during turn-off. Also, the squeezed plasma will tend to be extinguished in this non-regenerative center section (see Figure 1-3, pp. 10). The anode shorts may be thought of as being by-pass transistors in parallel with the thyristor. Therefore, while turn-off is aided, turn-on is impaired.

1. Device Structure and Geometry

The cross section of a device having an anode short placed opposite the center of the cathode emitter is schematically shown in Figure 4-1. The general effect of an anode short on turn-off was described above. In particular, turn-off gain is increased; fall time, tail current magnitude and tail decay time are decreased. Turn-off characteristics show an improvement similar to that achieved by gold diffusion. Since the lifetime can remain high, a lower on-state voltage drop is obtained 78-1. Further, control problems associated with gold diffusions are
Figure 4-1. GTO Structure showing Anode Short (By-Pass Transistor) and Series Schottky Barrier aligned with Center of Cathode
eliminated.

The drawback for anode shorts becomes clear if we examine such a structure with respect to turn-on and the degree of interdigation (cathode subdivision, to reduce the lateral turn-off distance $L_x$).

Assume in Figure 4-1 the N$^-$ region in the emitter center is ohmically connected to the anode metalization. Then, upon applying a positive bias to the gate-cathode junction, the NPN section is turned on. Initially, current is flowing through the short, setting up a lateral component.

The resulting lateral voltage drop constitutes the negative forward bias of the $P^+N^-$ anode junction. Injection is strongest in the anode region opposit the cathode edge. The diode knee voltage, i.e., \( \sim 0.7 \) volt for silicon, has to be reached before significant hole injection will occur, and only then can the device be triggered into the conduction state. Therefore, narrow cathode stripes and conductivity modulation of the N$^-$ region may prevent turn-on altogether. This effect shows a strong temperature dependence, because the current gains $\alpha_1$ and $\alpha_2$ drop with decreasing temperatures.

The problem is eliminated if the ohmic contact is replaced by a Schottky barrier\(^{79-1}\), as shown in Figure 4-1. In case, the barrier height is equal to that of the silicon PN junction and the diode characteristics in the forward direction are similar, lateral bias is not required. Device turn-on proceeds as for a standard thyristor.
Minority carrier injection in the Schottky barrier region is practically absent, however, and consequently the features aiding turn-off of this non-regenerative section are preserved.

Experiments were carried out to prove the series Schottky barrier concept. Devices with a geometry as shown in Figure 4–2 were chosen as test vehicles. The cathode geometry is the same as that of Device 2 in Figure 3–6 (bottom row, center), except that for this modified version the cathode fingers are portions of a continuous area, and the tips are rounded off. The gate envelopes this entire cathode pattern.

In assembly, a double gate contact clip is soldered to the regions just outside of the small center fingers. The cathode clip is attached in the middle of the cathode bus.

The rectangular center region (appr. 22 mils wide) at the back of the chip does not contain a $P^+$ anode diffusion. It is rendered inactive as a thyristor.

When this device is in the "on" state and a negative gate bias is applied, the electron-hole plasma is pinched toward the center of the individual cathode stripes. Because of the taper, the plasma is driven from the tips into the non-regenerative center region. There it is extinguished. Thus, the center is equivalent to a transistor bypass.

Surface preparation and choice of metalization can be chosen such
Figure 4-2.
Geometry Overlay of Cathode and Anode Surface showing non-regenerative Center Region (Anode Short or Schottky Diode)
that either an ohmic contact is formed with the N-region on the back surface to produce an anode short, or that a Schottky barrier is obtained. The metalization will always form an ohmic contact with the P\textsuperscript{+} anode, however.

For the experiment described here nickel, applied using a special electroless plating process, was used. When sintered at 580\textdegree{}C for 30 min. on a lapped (rough) surface an ohmic contact was obtained, whereas on a chemically polished (smooth) surface the nickelsilicide formed a suitable Schottky barrier. An alternate choice for forming a Schottky barrier is platinumsilicide.

2. Turn-On With and Without Schottky Barrier

The effect of a short versus a Schottky diode on the VI-characteristics for otherwise identical devices is illustrated in Figure 4-3. Junction depth and impurity profiles were very similar to devices, whose spreading resistance is given in Figure 3-8. However, the epi-base resistivity was lowered from \(\sim 0.28\ \Omega \text{cm} \) to \(0.11\ \Omega \text{cm} \), and the gold diffusion was omitted.

On the left hand side in Figure 4-3, the IV-characteristics of the device with an anode short are displayed (G400-1). The family of traces on top shows the device before turn-on. We see essentially an NPN transistor with \(\beta_1\) varying from 0.4 to 0.7 up to 1.06mA. The saturation voltage rises about linearly up to 0.7 volts for a base drive \(I_g = 2\text{mA}\). Thus, we conclude that up to this point the device
Figure 4-3.
VI Characteristics of GTO showing
Difference in Turn-on for Device with
Anode Short (G400-1, Left) and Device
with Series Schottky Barrier (G400-8, Right)
is dominated by by-pass current through the anode short.

As the base drive is increased, and the saturation voltage reaches the "diode knee" of the P⁺N anode emitter, a sudden gain increase and triggering into the on-state is accomplished. We conclude that now the device is dominated by "thyristor action". When the sum of the current gains (α₁ + α₂) reaches unity the device turns on (I_{gt} \sim 3.5mA @ V_D \sim 2V).

On the right hand side of Figure 4-3 the IV-characteristics of the device with a series Schottky barrier are displayed (G400-1). Again, the top family of curves show the device before turn-on. Here we see a distinct offset, as normally observed for a double injection device. Also, the gain is increasing rapidly. Both transistor sections are active as soon as base drive is applied, and the Schottky barrier by-pass current is only a fraction of that observed for the case with the anode short. The device is dominated by thyristor action throughout the entire range of operation. Turn-on occurs now for I_{gt} \sim 1.2mA @ V_D \sim 2V, as can be seen from the IV-traces displayed in the lower right hand side of Figure 4-3.¹

¹Of interest for the determination of α₁ and α₂ in thyristors are the measurement technique and algorithm developed by R. Amantea₉⁻⁵.
3. Turn-On Sensitivity and Turn-Off Capability

In Figure 4-4 we have plotted the turn-on sensitivity as a function of temperature for the two devices discussed in the previous section. The gate trigger current was measured with an anode supply voltage $V_D = 12V$ and a load resistance of $R_L = 30\Omega$.

The inserted table shows the forward voltage drop $V_T$ over a current range from 1.0A to 50A. As may be noticed in that respect, there is no discernible difference between the device with the anode short and the series Schottky diode.

In contrast, the gate trigger currents show a pronounced difference. The Schottky barrier device is considerably more sensitive. Especially at low temperatures (~40°C) the shorted anode device (G400-1) requires $I_{gt} \sim 70mA$, while for the device with the series Schottky barrier (G400-8) $I_{gt} \sim 10mA$ only.

The turn-off capability of both devices is given in Figure 4-5. In this test the GTO's were operated in cathode load configuration, the load being grounded, and the anode being directly connected to the supply voltage $V_D = 12V$. To achieve turn-off a transistor connected to the gate was turned on, pulling the gate close to the ground potential $(\nu + 0.2V)^1$. The peak gate gate current $I_{gqm}$ was

---

^1 A special turn-off circuit employing a small thyristor in parallel with a transistor was developed showing advantages for turn-off. The data given in Figure 4-5 were obtained using just a single transistor, however.
TABLE ON-STATE VOLTAGE $V_T$ VS ANODE CURRENT $I_A$ AT 25°C

<table>
<thead>
<tr>
<th>$I_A$ (A)</th>
<th>1</th>
<th>5</th>
<th>10</th>
<th>15</th>
<th>30</th>
<th>50</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_T$ No1</td>
<td>0.90</td>
<td>1.03</td>
<td>1.16</td>
<td>1.27</td>
<td>1.62</td>
<td>1.87</td>
</tr>
<tr>
<td>$V_T$ No8</td>
<td>0.90</td>
<td>1.06</td>
<td>1.18</td>
<td>1.28</td>
<td>1.54</td>
<td>1.81</td>
</tr>
</tbody>
</table>

Figure 4-4.
Turn-on Sensitivity as Function of Temperature for GTO with Anode Short (dashed line) and Series Schottky Diode (solid line)
Figure 4-5.
Maximum Turn-off Capability for GTO as Function of Temperature
approximately 5A.

As shown in the graph (Figure 4-5) for temperatures below +90°C both device types could turn-off 40A, the test set limit. At 125°C the Schottky barrier sample had only lost 25% of its turn-off capability over the sample with the shorted anode \( I_{T \text{off (max)}} = 24A \) compared to 32A, respectively).

This result demonstrates in a straightforward and explicit manner the effectiveness of the series Schottky barrier. The turn-on sensitivity in GTO's is restored, while the turn-off improvement gained from anode shorts is retained. Using this concept has made it possible to use non-regenerative regions in very narrow cathode geometries 79-1.

B. Dynamic Ballasting (Defocusing)

In the work on high speed device optimization and in experiments with anode shorts there were still failures observed (burn-out spots) which were evidently caused by high current density filaments. A pipe (about 40 to 50 micron in diameter) was molten through the silicon from the front to the back of the chip. The location of these pipes was not random in the cathode, but rather distinctly in an area most remote from the gate contact.

A typical example is shown in Figure 4-6. The entire chip is shown on top (Figure 4-6a). A small hole is visible in the center cathode finger opposite the gate pad. The gate of this device was contacted with a single clip only. The burn-out spot is clearly visible in the
Pipe Molten Through Silicon (magnified below)

Figure 4-6a. Device Chip after Failure (Metal removed).

Figure 4-6b. Magnified View of Damaged Area

Figure 4-6. Turn-off Failure for GTO-SCR at Location most remote from Gate Contact.
magnified microphotograph below (Figure 4–6b).

In order to minimize such burn-out failures a method was thought that would prevent the formation of high current density filaments during the turn-off process. Dynamic Ballasting \textsuperscript{77–l, 80–l} or de-focusing was investigated and proved to be a very effective remedy.

1. Defocusing Principle and Device Structure

Figure 4–7 is the schematic cross-section of an epitaxial GTO structure in which the standard high concentration, phosphorus doped cathode is replaced with a lower concentration, resistive ion-implanted N layer. Also, the center of the cathode is insulated, only the edge is contacted with the metal electrode.

The resistive layer is dimensioned such that for turn-on and the on-state, while modest current densities exist in the device, we can expect normal thyristor behavior; i.e., fast turn-on with high sensitivity and low forward voltage drop.

In the process of turn-off, however, when the electron-hole plasma is being squeezed toward the center high current densities will tend to develop locally beneath the insulated cathode section. Then, the lateral current flow in the resistive region will cause a voltage drop along the PN junction, and the cathode becomes debiased in the direction of the center. Consequently, the current injection will decrease rapidly because of its exponential dependence on the junction bias voltage according to the diode law.
Figure 4-7.
Schematic of Epi-GTO featuring Resistive Cathode with Isolated Center to achieve Dynamic Ballasting (Defocusing)
Devices designed and fabricated for the experiments to investigate the effectiveness of the Dynamic Ballastng concept were of the geometry Type 3 (see Figure 2-8, bottom counter). The epitaxial p-gate layer was about 30 micrometer thick and had a resistivity of 0.12Ωcm. The epitaxial N- region of the wide PNP base was about 50 micrometer thick with a resistivity of 50Ωcm, followed by a 20 micrometer wide, 2.0Ωcm layer to prevent early punchthrough. The 0.01Ωcm boron doped substrate served as the anode.

2. Turn-Off With and Without Dynamic Ballasting

The cathode load response $I_{k} = f(t)$ and the anode current $I_{A} = f(t)$ for devices with dimensions and physical parameters given in the previous section are shown in Figure 4-8. The turn-off circuit and conditions used were the same as those applied in the series Schottky barrier experiments.

The top traces are the turn-off characteristics for a device having a standard, heavily doped cathode of $R_{sk} \approx 0.7Ω/square$. The turn-off gate pulse is initiated at $t = 35$ microseconds. We detect an initial current drop across the load (left), a storage time $t_{s} = 15$ microseconds, and a fall time $t_{f} \approx 4$ microseconds, followed by a 25 microsecond tail period starting at a current of 1A.

The anode current (right) increases sharply when the gate turn-off pulse is applied, because the gate is grounded through the input driver and an additional low impedance path is provided.

---

1For "defocused" devices, Series 97H the Mask M04 (Figure B-1e) was substituted with Mask M05 (Figure B-1g, pp. 152).
Figure 4-8.
Cathode Load Response $I_C(t)$ (Left),
and Anode Current $I_A(t)$ (Right) for Epitaxial
(N)PN- N(P+) GTO-Thyristor with
Std. Diffused Cathode Emitter (Top) and
Resistive, Defocused Cathode Emitter (Bottom)
$T=125^\circ C$, Vert.=2 A/Div, Hor.=10 $\mu s$/Div
During the tail period the anode current has still a considerable magnitude, starting with a value of 5A. The difference between anode current and cathode current is of course the gate current $I_{gq}$.

We see this device has a poor turn-off performance even at 25°C.

The bottom traces of Figure 4-8 are the turn-off characteristics for a device having an ion implanted cathode of $\sim 20 \Omega$/square, metalized at the edge according to the schematic of Figure 2-7. Otherwise, structure and fabrication process were identical to the device above. Circuit conditions for turn-off remained also unchanged. The case temperature$^1$ was here raised to 125°C, however.

We see that in comparison to the non-ballasted device the storage time and fall time have drastically decreased, and the tail current through the load has just about vanished (left). The anode current (right) as well as the gate current pulse, and therefore also the turn-off energy are considerably diminished.

We observe this device has an excellent turn-off capability even at 125°C, which is the generally accepted upper temperature limit for reliable thyristor operation.

Figure 4-9 shows the turn-off portion for resistive cathode

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$^1$In these tests the GTO's were operated at low duty cycles. Therefore, the case temperature is close to the actual center junction temperature.
Figure 4-9. Turn-off Response for Epitaxial (N)PN\textsuperscript{−}N(P\textsuperscript{+}) GTO in Cathode Load Circuit, $I_\text{k}=f(t)$ (Left), $I_\text{A}=f(t)$ (Right). Top Traces are for fully Metallized, Resistive Cathode; Bottom Traces are for Edge Metallized, Defocused Cathode. $T=125^\circ\text{C}$, Vert.$=2\ A/\text{Div}$, Hor.$=2\ \mu\text{s}/\text{Div}$. 

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure49.png}
\end{figure}
emitters on a 5X expanded time scale over the traces in Figure 4-8. The bottom traces are just an expansion of the ones of unit 97/11H in Figure 4-8. The total turn-off time \( t_s + t_f \) is only about 4 micro-second, the tail is indeed negligible, and the switching dissipation is small compared to the case for the standard cathode device (Figure 4-8 top).

The top traces in Figure 4-9 show a device (97/11G) with the identical resistive cathode as the one on the bottom. But here the entire cathode area is metalized. The response is slower and the switching dissipation is higher than for the "insulated cathode center" type. Yet, even in this case the ballasting appears to be rather effective over the standard cathode unit.

The shortened turn-off time, the reduction of the tail current, and increased turn-off capability at elevated temperatures are an indirect indication that for nominal values dynamically ballasted devices can be much safer operated than conventional GTO's

3. **Summary of Results**

The results of the experiments demonstrating the effect of dynamic ballasting are summarized in Table 4-1. Gate trigger current \( I_{gt} \), forward voltage drop \( V_T \), and maximum current turn-off capability are tabulated. The data represent averages of about 25 devices for
<table>
<thead>
<tr>
<th>Geometry</th>
<th>I&lt;sub&gt;gt&lt;/sub&gt; (mA)</th>
<th>V&lt;sub&gt;T&lt;/sub&gt; (V)</th>
<th>Max. I&lt;sub&gt;turn-off&lt;/sub&gt; (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Std. G400</td>
<td>12.0</td>
<td>1.15</td>
<td>25</td>
</tr>
<tr>
<td>R&lt;sub&gt;sk&lt;/sub&gt;~.7Ω/□</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D3, PN−N&lt;sup&gt;+&lt;/sup&gt; Epi</td>
<td>.7</td>
<td>1.22</td>
<td>9</td>
</tr>
<tr>
<td>R&lt;sub&gt;sk&lt;/sub&gt;~.7Ω/□</td>
<td>.75</td>
<td>1.48</td>
<td>15</td>
</tr>
<tr>
<td>D3, PN−N&lt;sup&gt;+&lt;/sup&gt; Epi</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;sk&lt;/sub&gt;~20Ω/□</td>
<td>1.3</td>
<td>1.53</td>
<td>18</td>
</tr>
<tr>
<td>D3, PN−N&lt;sup&gt;+&lt;/sup&gt; Epi</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R&lt;sub&gt;sk&lt;/sub&gt;~20Ω/□ + Defocusing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>+ Defocusing</td>
<td>-40°C</td>
<td>+25°C</td>
<td>+25°C</td>
</tr>
<tr>
<td>+125°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D3, PN−N&lt;sup&gt;+&lt;/sup&gt; Epi</td>
<td>.3</td>
<td>1.28</td>
<td>9.3</td>
</tr>
<tr>
<td>R&lt;sub&gt;sk&lt;/sub&gt;~7Ω/□</td>
<td>.3</td>
<td>1.28</td>
<td>9.3</td>
</tr>
<tr>
<td>+ Defocusing</td>
<td>+25°C</td>
<td>+25°C</td>
<td>+25°C</td>
</tr>
<tr>
<td>+150°C</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4-1. Effect of Resistive Cathode and Dynamic Ballasting (Defocusing) on GTO Temperature Behavior.
each test cell\(^1\), except for the standard G400.

The desired characteristics are of course a small \(I_{gt}\) at low temperatures, a high \(I_{T\,\text{off}}\) \(\text{(max)}\) at high temperatures and a low forward voltage drop \(V_T\).

The first data line shows best results obtained for a conventional, anode shorted device with the geometry shown in Figure 4-2 (G400) and having a standard triple diffused doping profile. Such a device needs 12mA for turn-on @ -40°C, has a forward voltage drop of 1.15 volts @ 10A and 25°C, and it can turn-off 12A @ +125°C.

Compared with these results are the all-epitaxial test devices described in section IV Bl. In particular, the second data line gives results for devices with a standard 0.7Ωcm cathode (Figure 4-8, top). As can be seen, this device is very sensitive (\(I_{gt} \approx 0.7\text{mA} @ -40°C\)) for turn-on, however, it has lost its good turn-off capability at high temperatures (Now \(I_{T\,\text{off}}\) \(\text{(max)}\) \(\approx 2\text{A}\)).

The data shown in the fourth line are for the devices with an ion implanted cathode emitter of 20Ω(square, edge metalized (Figures 4-8, 4-9, bottom). As can be seen \(I_{gt}\) is still only of the order of 1mA @ -40°C while the turn-off capability has increased to 14A at the high

\(^1\)The computer printout of static data for the devices of series 97E (standard 0.7Ω/square cathode) and of series 97H (implanted, defocused 20Ω/square cathode) is added as Appendix C.
temperature. The forward voltage drop has suffered an increase of 0.3 volts, however.

The final data line shows results for devices which were further optimized. The cathode sheet resistance was lowered from \( \sim 20\Omega/\text{square} \) to \( \sim 7.0\Omega/\text{square} \) and the epi-base resistivity was raised from \( \sim 0.12\Omega\text{cm} \) to about \( 0.18\Omega\text{cm} \). A pronounced improvement in overall electrical characteristics was achieved. The temperature range of operation was substantially extended. Turn-on was obtained with \( I_{gt} \sim 0.3\text{mA} @ -60^\circ\text{C} \) and turn-off capability was measured to be \( I_{T\text{ off}} (\text{max}) = 9.3\text{A}, 9.0\text{A}, \) and \( 8.5\text{A} \) for \( 25^\circ\text{C}, 125^\circ\text{C}, \) and \( 150^\circ\text{C} \), respectively. The maximum current that could be turned off was relatively independent of temperature.

The results show rather distinctly that Dynamic Ballasting gave very useful advantages.
V. CONCLUSION

A. High Speed-High Voltage Gate Turn-Off Device

1. The investigations of GTO-structures have shown that high speed-high voltage devices are feasible. It was demonstrated that the turn-off behavior is governed by pronounced two-dimensional effects. A narrow cathode width is of importance. Further, the introduction of an external gate series inductance and operation from a voltage source as input for turn-off will result in a safe return to the blocking state. The criteria being that:

(a) during the fall phase the second derivative of the turn-off gain $d^2I_A/dI_{gq}^2$ remains positive,
(b) the turn-off gain itself becomes less than unity during the tail period.

2. Further, fast turn-on $t_r$ and fast turn-off $t_f$ with a minimum recombination tail were simultaneously obtained through development of a special gold diffusion process. This process was critical such that:

(1) a high lifetime was designed into the active region of the device beneath the cathode emitter, and
(2) a low lifetime was build into the vicinity of the anode emitter.
3. A resultant device demonstrated switching times of 100 to 400 nanosecond and switching power capabilities of 1.55 kw @ 50kHz with 97% device efficiency. This is quite an achievement over the existing state of the art.

B. Anode Shorts and Schottky Barriers

In the available design anode shorts have been used for improvement of turn-off and reliability of the device. These anode shorts, which are placed most remote from the gate terminal, represent a non-regenerative region (or by-pass transistor) which is very effective in extinguishing the final plasma filament during turn-off. They also reduce the recombination tail. However, the turn-on is now in general impaired, especially at low temperatures.

In our research design a Schottky barrier was introduced in series with these anode shorts, which fully restored the turn-on sensitivity, while the improvement in turn-off capability due to the anode shorts was retained.

C. Dynamic Ballasting (Defocusing)

The introduction of a slightly resistive cathode and an isolated center, metalized at the edge only will have the effect of dibiasing the cathode emitter junction while the plasma is squeezed into the "geometrical center of gravity" during turn-off. During normal on-
state operation with nominal current densities a negligible additional forward voltage drop is experienced. During turn-off, however, locally high current density filaments develop because of plasma squeezing. The formation of these filaments is strongly counteracted by a lateral voltage drop in the cathode, and the exponentially dependent decrease of current injection toward the emitter center. Using this principle, the device operation was extended from $-20^\circ\text{C}$ to $+125^\circ\text{C}$ (for a conventional device) to a range of $-60^\circ\text{C}$ to $+150^\circ\text{C}$ for our research devices.
APPENDIX A

COMPUTER PROGRAM FOR PHOTO MASK SET GENERATION

The CAD artwork for the 3x3 array of test geometries (IIC, pp. 53) was generated by an "easy-to-use data-capture language" called PLOTS75-4.

In this method geometric shapes are described as (usually opaque) polygons in a rectilinear coordinate system, either in terms of an absolute vertex location or as relative vertex coordinates in the directions left, right, top, and bottom from the previous vertex.

Thus basically, definitions D are created by a number of statements, consisting of strings of coordinates. These definitions may be placed in certain locations by "Q"-calls and are organized to appear on a specified photo mask M.

The PLOTS programs will then interface with either automatic-drafting equipment and CRT display systems for error checking and testing, or they will through an intermediate conversion serve to control a precision photoplotter for mask set fabrication.

In Figure A-1 is shown a sample PLOTS language statement (top), which is translated into the corresponding computer generated artwork (bottom).
SAMPLE ARTWORK MARK 500X

FIGURE A-1 SAMPLE PLOTS LANGUAGE STATEMENT (TOP) AND COMPUTER GENERATED ARTWORK (BOTTOM). THE "FIGURE" NUMBERS THAT FOLLOW THE PLOTS STATEMENTS (SEPARATED BY SEMICOLONS) CORRESPOND TO NUMBERED SHAPES ON THE ARTWORK (AFTER B.J. Korenjak 74-1)
Figure A-2 is the program defining the photo mask set which was used to fabricate the test devices described in Chapter III, and IVB.

For illustration purposes let us follow the steps that will generate the cathode emitter mask pattern of Device 3 (Figure 3-6, pp. 54 or Figure B-16, pp. 147, bottom left).

First a single site, D24 is defined by the statement

\[ P \text{ XO Y-2.25 (Right 16 Top 1) T2.5 (Left 16 Tl) Bottom 4.5 (line 1940)} \]

Then in D25 (line 1960 to 2040) the first quadrant of the pattern is generated with the center of the (whole) pattern being the origin (fiducial point). Q calls place the single sites into the proper locations, create more of them by "and" statements (ex. line 1990) or rotate them, as done to get the vertical site close to the center (Q24 X4.75Y14 Rotate 3, line 1970).

In D65 the quarter pattern is assigned to its mask level M3 (line 5320-5330) and stacked up with all other quarter patterns belonging to Device 3.

In D73 (line 6130) the cathode pattern is rotated and mirrored simultaneously with its 1st quadrant companions of the other masks such that all 4 quadrants (i.e., the entire pattern now exists).
Finally, the call Q73 (line 6360) will place the cathode sites and all other mask levels into the lower left hand corner of the array of devices (called out as Q68 to Q75 (line 6310 to line 6380).
A-20 CAD PROGRAM, PAGE 1 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-2 CAD PROGRAM, PAGE 2 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTO-MASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-3 CAD PROGRAM, PAGE 3 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-4 CAD PROGRAM, PAGE 4 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES, LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-5 CAD PROGRAM, PAGE 5 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-6 CAD PROGRAM, PAGE 6 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-7 CAD PROGRAM, PAGE 7 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
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A2-8 CAD PROGRAM, PAGE 8 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-9 CAD PROGRAM, PAGE 9 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
### A2-10 CAD PROGRAM, PAGE 10 OF 14

**A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).**
A2-11 CAD PROGRAM, PAGE 11 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A-2  COMPUTER PROGRAM (Plots LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-13 CAD PROGRAM, PAGE 13 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND FIGURE 3-6).
A2-14 CAD PROGRAM, PAGE 14 OF 14

A-2 COMPUTER PROGRAM (PLOTS LANGUAGE) FOR ARTWORK GENERATION TO PRODUCE PHOTOMASK SET FOR 3 x 3 ARRAY OF GTO-DEVICES; LINE 10-8020, 14 PAGES (SEE APPENDIX B AND Figure 3-6).
APPENDIX B

PHOTO MASK SET FOR 3x3 ARRAY OF GTO DEVICES

The mask set for fabrication of the test geometries used for studying the behavior of GTO devices is shown in this appendix Figure B-la to B-1f.
FIGURE B-1a  M01, P^+ GATE CONTACT DIFFUSION

FIGURE B-1  PHOTOMASK SET FOR FABRICATION OF 3 X 3 ARRAY OF GTO TEST GEOMETRIES, CENTER CONTAINS DIAGNOSTICS AND ALIGNMENT PATTERN. (FOR DIMENSIONS AND USE IN PROCESS SEE PP 53-55, AND 56-58, RESPECTIVELY)
FIGURE B-1b MO3, CATHODE EMITTER DIFFUSION
FIGURE B-1c MOG, MESA DEFINITION
FIGURE B-1d  MO8,OXIDE SHELF REMOVAL
FIGURE B-1e MO4, GATE AND CATHODE CONTACT OPEN
FIGURE B-1f  MO7, DEFINE METAL ELECTRODES
FIGURE B-1g  MO5, GATE AND CATHODE CONTACT OPEN (DEFOCUS)
APPENDIX C

STATIC DATA FOR GTO'S WITH STANDARD CATHODE
AND DYNAMICALLY BALLASTED CATHODE

A printout of static data from computer tested gate turn-off thyristors is given in this appendix.

Figure C-1 shows the data for GTO's of Device Type 3 with an all-epitaxial structure and a standard 0.7Ω/square cathode diffusion (series 97E).

Figure C-2 shows the data for GTO's of Device Type 3 having a 20Ω/square resistively ballasted, defocused cathode (series 97H).

The first line in these data tables gives the quantity measured, current or voltage. The second line specifies the voltage or current at which the value for this measured parameter is recorded, except for $I_{gt}$, where it is the maximum trigger current available. The third line indicates the upper limit of the computer range. $R_{GK}$ is a resistor added in parallel to the gate-cathode.
LOT 97-E 11/16/78

TESTED TO

G4000-5 H. BECKE 11/3/77

VDRXMK VDRXMK IDRXMK IDRXMK IDRXMK IDRXMK IDRXMK IDRXMK VKA
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FIGURE C-10 FORWARD BLOCKING VDRXMK, REVERSE LEAKAGE IDRXMK, REVERSE BLOCKING VKA

FIGURE C-1 STATIC DATA OF COMPUTER-TESTED ALL-EPI-THYRISTORS. LOT 97E; STANDARD CATHODE, RS~0.7 Ω/Ω (SEE CHAPTER IV, TABLE 4-1)
**LOT 97-E  11/16/78**

**TESTED TO**

**G4000-5  H. BECKE  11/3/77**

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**FIGURE C-1b**  GATE TRIGGER CURRENT $I_{gt}$

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LOT 97-E 11/16/78
TESTED TO
G4000-5 H. BECKE 11/3/77

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FIGURE C-1c ON-STATE VOLTAGE $V_T = f(I_T)$
FIGURE C-2a  FORWARD BLOCKING $V_{DRXM}$, REVERSE LEAKAGE $I_{DRXM}$, REVERSE BLOCKING $V_{KA}$

FIGURE C-2  STATIC DATA OF COMPUTER-TESTED ALL-EPI TAXIAL GTO-THYRISTORS.
LOT 97H; IMPLANTED, DEFOCUSED CATHODE,
$R_{SK} \sim 20 \, \Omega/d$
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ON-STATE VOLTAGE \( V_T = f(I_T) \)
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**FIGURE C-2c** ON STATE VOLTAGE $V_T=f(I_T)$
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