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Investigation of epitaxial lift-off GaAs and langmuir-blodgett films for optoelectronic device applications

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Investigation of epitaxial lift-off GaAs and Langmuir-Blodgett films for optoelectronic device applications

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New Jersey Institute of Technology, 1992

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INVESTIGATION OF EPITAXIAL LIFT-OFF GaAs AND LANGMUIR-BLODGETT FILMS FOR OPTOELECTRONIC DEVICE APPLICATIONS

BY
DIVYANG M. SHAH

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APPROVAL PAGE

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Abstract

Investigation of Epitaxial Lift-off GaAs and Langmuir-Blodgett Films for Optoelectronic Device Applications

Epitaxial lift-off (ELO), a technique of removing an epitaxially grown GaAs layer from its growth substrate by selective etching of an AlAs sacrificial layer, is described for field-effect transistor fabrication independent of the GaAs growth substrate. Metal Semiconductor Field-Effect Transistors (MESFETs) and High Electron Mobility Transistors (HEMTs) fabricated on silicon and sapphire substrates using ELO are investigated. A 0.1 μm gate length depletion mode MESFET made on silicon exhibited a unity current gain frequency f_t = 34 GHz. Excellent device isolation with subpicoampere leakage currents is obtained. A high input impedance amplifier has been implemented on silicon substrate using ELO GaAs MESFETs. The amplifier had an input RC time constant limited bandwidth of 500 MHz.

Results of investigation of a novel source of cadmium and zinc diffusion for shallow p^+-n junction fabrication in $In_{0.53}Ga_{0.47}As$/InP are also presented. Langmuir-Blodgett (LB) deposited monolayers of Cadmium and Zinc arachidate have been used as a source of Cd and Zn dopants in InGaAs/InP. This new source provides precise control of the dopant dose through the number of LB film monolayers deposited and it is also a safer method of handling toxic Cd. The LB film can be patterned by lift-off for a patterned diffusion without a mask. Highly doped (N_a= 2 -4 x 10^{19} cm^{-3}), shallow (0.1-0.4 μm) p^+-n junctions have been obtained. Junction field-effect transistors(JFETs) and PIN photodetectors have been fabricated as a demonstration of the usefulness of the technique. A PIN photodetector had a 100 pA dark current at -5 V DC bias and a bandwidth of 2 GHz.

A new technique for fabricating optoelectronic integrated circuit (OEIC) photoreceivers for 1.3-1.55 μm wavelength optical communication has also been proposed. The proposed OEIC uses ELO GaAs MESFETs and InGaAs/InP PIN photodetectors.

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2. 'GaAs MESFET and HEMT fabrication on silicon substrate using epitaxial lift-off as an alternative to heteroepitaxy', D. M. Shah, W. K. Chan, C. Caneau, T. Gmitter, and L. Florez, Seventh annual Sarnoff Symposium of the IEEE Princeton section, March 22, 1991.

3. 'InGaAs Shallow junction fabrication using Langmuir-Blodgett film diffusion source', D. M. Shah, W. K. Chan, H. M. Cox, R. Bhat, N. E. Schlotter, and C. C. Chang, Applied Physics Letters, Vol. 56, pp. 2132-2134, 1990.

4 'GaAs MESFETs on Silicon Using Epitaxial Lift-Off', W. K. Chan, D. M. Shah, T. Gmitter, L. T. Florez, B. P. Van der Gaag, and J. P. Harbison, proceedings of the SOTAPOCS XII, 177th Electrochemical society meeting, May '90.

5. 'DC and RF performance of a GaAs MESFET on silicon substrate', D. M. Shah, W. K. Chan, T. Gmitter, L. Florez, H. Schumacher, and B. P. Van der Gaag, IEE Electronics Letters, Vol. 24, pp. 1865-66, 1990.

6. 'Epitaxial lift-off GaAs for electronics', D.M. Shah, W. K. Chan, C. Caneau, T. Gmitter, and W.-P. Hong. To be submitted for publication.

This thesis dedicated

To

My Parents and Grandparents

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I have done all of my doctoral dissertation research at the Navesink Engineering and Research Center of Bellcore, located in Red Bank, NJ. I would like to thank Dr. Bob Leheny, Dr. Eli Kapon, and Dr. Harold Craighead (now at Cornell University) for providing me with the opportunity to work at Bellcore.

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CHAPTER 1

Introduction

Results of investigation of epitaxial lift-off GaAs and Langmuir-Blodgett thin films for optoelectronic device application are presented in this thesis. All the experimental work for this dissertation was done at Navesink Engineering and Research Center of Bell Communications Research (Bellcore), located in Red Bank, NJ. The lightwave communication project described in the following chapters involved close cooperation of several members of technical staff of Electronics Science and Technology Research Laboratory of Applied Research Area.

Lightwave communication technology is important for very high bandwidth transmission. Optical signals can propagate over a silica fiber with very low loss (< 0.5 dB/km) and dispersion between 1.3 - 1.6 μm. The signal attenuation is minimum at 1.55 μm and the dispersion goes to zero at 1.3 μm wavelength. While the signal transmission over the fibers is in lightwaves, the communication equipment at the transmitting and the receiving ends is still electronic, capable of processing only electrical signals. The need for electrical-to-optical and optical-to-electrical conversion has resulted in the development of optoelectronic transmitters and receivers. All of the transmitters and receivers in use at present are made from hybrid integration of electronic and optical components. One has to rely on hybrid integration of components because high speed transistors are made using GaAs or Si which cannot lase or detect light at 1.3-1.55 μm, the wavelength range coinciding with the lowest signal loss and dispersion in the silica optical fibers. The lasers and the photodetectors are made in $In_xGa_{1-x}As_yP_{1-y}/InP$ which can lase in the 1.3-1.55 μm wavelength range and also can exhibit high absorption in the same range. Energy band gap of $In_xGa_{1-x}As_yP_{1-y}/InP$ can easily be engineered by changing its composition.

The bandwidths of hybrid transmitters and receivers are limited by parasitics introduced by the interconnects used for integrating electronic and light emitting/detecting components. The hybrids are also expensive because of high cost of their assembly. For present day transmitters and receivers operating at several hundred megabits per second, the use of hybrid integration of electronic and optical components is permissible. However, multigigabit per second telephone networks of the future will require the use of monolithic optoelectronic components. This is the driving force behind much current interest in optoelectronic integrated circuits (OEIC).

OEIC receivers in InGaAs/InP have evolved from just one transistor and one photodetector[1] to small and medium scale integrated circuits over a period of one decade from its inception. There is still much room for improvement in the OEIC fabrication technology as well as in their performance because the state of the art OEICs have not achieved the bandwidths and the sensitivities predicted from theory or that obtained by hybrids. This thesis is an attempt to close the gap between the two. It involves an unconventional approach for solving the problems with OEIC photoreceivers. The idea is a simple extension of the principle behind the hybrid photoreceivers presently used but with an added advantage of monolithic integration. As discussed in the Chapter 4, the fabrication of FETs in GaAs and photodetectors in InGaAs/InP would be an important achievement. It would enable manufacturers to take advantage of the mature material and device technologies of GaAs and InGaAs/InP for transistors and photodetectors, respectively.

For the proposed OEIC, fabrication of GaAs FETs independent of GaAs growth substrate is necessary. Chapter 2 is a detailed account of the comprehensive and systematic investigation of epitaxial lift-off (ELO) GaAs Metal Semiconductor Field-Effect Transistor (MESFET) and AlGaAs/GaAs High Electron Mobility Field-Effect Transistor (HEMT) fabrication independent of GaAs substrate. It is the goal of this study to investigate feasibility of using ELO GaAs as an alternative to heteroepitaxy of GaAs on crystalline or noncrystalline substrates.

The use of ELO GaAs requires that the new host be free of surface roughness on a microscopic scale. As mentioned earlier, we are planning to use InGaAs/InP PIN photodetectors for OEIC. The conventional PIN photodetectors made by epitaxial growth are mesa type having nonplanar wafer surface at the end of fabrication cycle. It is difficult to planarize such surface, especially for bonding ELO GaAs which requires almost mirror smooth surface. PIN photodetectors can be fabricated by local impurity diffusion or ion implantation of acceptors to avoid the mesa structure and the large leakage currents from the exposed p-n junction at the mesa edge. However, both of these techniques have problems associated with them. Diffusion in a closed ampoule is popular but it cannot be used for large samples required for integrated circuit fabrication. Radiation induced damage to the semiconductor crystal lattice cannot be completely removed when ion implantation is used for introducing dopants. Unavailability of a satisfactory dopant source for making large area, highly doped p^+-n junctions in InGaAs/InP was a reason for investigating Langmuir-Blodgett (LB) films. It is the purpose of LB film study to investigate feasibility of using

LB deposited cadmium arachidate and zinc arachidate monolayers as dopant sources in InGaAs/InP. This new diffusion source, described in Chapter 3, can solve all of the above problems without increasing the complexity of processing. PIN photodetectors and junction field-effect transistors (JFETs) have been fabricated using Cd diffusion from the LB film. Electrical characteristics of the photodetectors and the JFETs are also presented in Chapter 3.

The results of ELO GaAs FETs and LB film diffusion source are summarized in Chapter 5. This chapter also contains conclusions and suggestions for future work.

To avoid repetition and maintain continuity of the presentation, standard fabrication processes used during this investigation are described in the Appendix. These processes are n and p type ohmic contacts for GaAs, InGaAs and InP; Schottky contacts for n-GaAs; wet chemical etching and ion beam assisted etching of GaAs, InGaAs/InP and AlGaAs/GaAs; reactive ion etching of spin-on glass; plasma etching of silicon nitride; plasma enhanced chemical vapor deposition of silicon dioxide and nitride. These processes are simply referred at the point of use without giving details as if the reader is conversant with it. Any exceptions to the processes are mentioned explicitly.

CHAPTER 2

Epitaxial Lift-off GaAs for Electronics

2.1 Introduction

A novel technique of GaAs MESFET and HEMT fabrication that is independent of growth substrate is described in this chpter along with their DC and RF characteristics. This new technique uses epitaxial lift-off (ELO) for removing the epitaxial layer structure of GaAs MESFET or HEMT from its growth substrate. The new technique has been developed with a specific application in sight, i.e., integrability of the FETs for making an integrated circuit (IC). The requirement of integrability has forced a choice of simpler FET material structure accompanied with an unconventional fabrication process that guarantees reasonable DC and RF performance with uniformity of electrical characteristics over a large area.

This chapter is divided in six parts. Reasons for investigating ELO GaAs FET technology are given in section 2.1. Section 2.2 is an overview of GaAs FET technology from a device technologist's point of view. Previous work on ELO of GaAs is reviewed in section 2.3. Section 2.4 describes ELO GaAs MESFET and AlGaAs/GaAs HEMT development, along with their DC and RF performance characteristics. A statistical study of DC parameter distribution across an ELO and on-wafer HEMT samples appears in section 2.5. Stability assessment of ELO HEMT under continuous DC bias is presented in section 2.5.3. The ELO FET experiments are summarized in section 2.6.

The work on ELO GaAs FETs described in this chapter would not have been possible without collaborations with Dr. Catherine Caneau for Organometallic Chemical Vapor Deposition (OMCVD) growth of GaAs and AlGaAs/GaAs epitaxial layers and that with Tom J. Gmitter for epitaxial lift-off of GaAs.

Heteroepitaxial growth of GaAs on silicon[2] and InP[3] substrates has been motivated by the possibility of combining the advantages of each of these materials. However, material grown in this manner has very high dislocation densities at the GaAs/Si and GaAs/InP interfaces due to a large lattice mismatch and requires a thick (~2-3 μm) buffer layer to obtain device quality material. Also, stress resulting from a large difference in the thermal expansion coefficients of GaAs, InP and silicon, leads to undesirable substrate bowing as the sample is cooled from the growth temperature. A new technique of fabricating GaAs

MESFETs on polished semiconductor or non-semiconductor substrates described in the following sections overcomes these problems.

Heteroepitaxy of GaAs on silicon and InP requires direct growth on high dielectric constant semiconductor buffer layer to ensure single crystal GaAs growth. Buffer layer resistivity in excess of 10^6 Ω-cm is required for good device isolation. It is difficult to obtain a very high resistivity buffer layer even in an extremely clean epitaxial growth reactor because of the presence of residues from previous growths. Degradation of high frequency performance of the GaAs FETs owing to signal loss and capacitive coupling to the conducting substrate is an unavoidable consequence of it. Epitaxial lift-off is used to graft GaAs onto a new substrate covered with a thick, low dielectric constant buffer layer to realize the full advantage of high speed GaAs devices. The ability of choosing a buffer independent of the epitaxial growth system is a key to reducing parasitics associated with conducting substrates. Since the buffer deposition can be done outside of the epitaxial growth reactor, it can be chosen from a wide variety of available insulators that is most compatible with a particular application.

During the heteroepitaxy of GaAs on silicon, prolonged high temperature processing degrades the threshold voltages of the silicon MOSFETs.[4] In contrast, ELO GaAs FET fabrication is a low temperature process except only one short, high temperature (420°C) ohmic contact alloying step that is well below any temperature capable of causing a threshold shift in the silicon devices. Because of the low temperature processing, thermal expansion mismatch induced stresses are also minimum.

One reason for development of GaAs MESFETs on silicon is integration of high complexity, low power CMOS integrated circuits with high speed GaAs circuits. Although we have fabricated MESFETs only on unprocessed silicon wafers, this technique is expected to work equally well with wafers containing functional silicon circuits. Another possible application of ELO GaAs on silicon is monolithic integration of light emitting devices such as GaAs LEDs and laser diodes with high complexity silicon driver circuits.[5] The GaAs MESFETs on sapphire (section 2.4.1.2.4) can be readily used for monolithic millimeter wave integrated circuits (MMICs) with appropriate changes in fabrication sequence. A novel use of ELO GaAs on InP, as described in the chapter on ELO applications is the integration of GaAs MESFETs with InGaAs/InP PIN photodetectors for making an optoelectronic integrated circuit (OEIC). The proposed OEIC takes advantage of the mature GaAs FET and InGaAs/InP photodetector technologies.

2.2 Background on GaAs FET Design Principles and Technology

GaAs FET development is driven by the promise of superior high frequency performance and radiation hardness over its counterpart in silicon, namely, metal-oxide semiconductor field-effect transistors (MOSFETs). Good device and fabrication process designs are required for realization of these advantages. A brief overview of a GaAs MESFET design is given in this section. A high electron mobility field-effect transistor (HEMT) described in the later part of this chapter can also be designed following the same general guidelines with the exceptions of relations for saturated drain current and channel pinch-off voltage. A more rigorous treatment of the subject can be found in the recent texts by Sze[6] and Ali, et al.[7] An n-Channel MESFET design is discussed here but a p-channel MESFET can also be designed following the same relations with appropriate changes in voltage polarity and charge carrier velocity.

The MESFET design starts with specification of the saturated drain current and channel pinch-off voltage. The saturated drain current is given by

$$I_{dss} = q\, v_S\, N\, a = 192\, N\, a \qquad (2.1)$$

and the channel pinch-off voltage (gate voltage where drain current goes to zero) is determined by Poisson's equation

$$|V_P| = \frac{qN\,a^2}{2\varepsilon_S} = 7\ N\ a^2 \qquad (2.2)$$

where N is the channel doping in 10^{16} cm^{-3}, a is the channel thickness in μm, ε_S is dielectric constant of GaAs, I_{dss} is mA/mm, and v_S is electron saturation velocity in cm/s. The channel thickness and the doping are determined by solving the equations 2.1 and 2.2 simultaneously. For FETs with short < 2 μm gate lengths, electron transport under the gate is with saturation velocity v_S. The frequency at which current gain of an FET becomes unity is defined as unity current gain frequency f_t. The f_t is an important figure of merit for FETs operating at high frequency because it determines the upper limit of operating digital circuits. The required gate length for a given unity current gain frequency f_t is obtained from the relations:

$$f_t = \frac{1}{2\pi\tau} \qquad (2.3)$$

and

$$\tau = \frac{L}{v_s} \qquad (2.4)$$

where L is the gate length in cm and τ is the electron transit time under the gate in seconds. The relation for f_t can also be stated as:

$$f_t = \frac{g_m}{2\pi C_G} \approx \frac{g_m}{2\pi C_{GS}} \qquad (2.5)$$

where C_G is the total gate capacitance in Farads, and g_m is the extrinsic transconductance of FET in siemens (S). The gate capacitance includes the gate-source capacitance C_{GS} and the gate-drain capacitance C_{GD}. The gate capacitance C_G can be approximated by the gate-source capacitance C_{GS} because under the normal biasing conditions, the $C_{GD} << C_{GS}$. The extrinsic transconductance g_{me} (as seen at the FET terminals, often referred to as g_m) is an important figure of merit of an FET determining its gain, is related to the intrinsic transconductance g_{mi} by

$$g_{me} = \frac{g_{mi}}{1 + R_S g_{mi}} \qquad (2.6)$$

where R_S is the source resistance. From 2.3 and 2.5

$$g_{mi} = \frac{C_{GS}}{\tau} \qquad (2.7)$$

Another useful relation for the intrinsic transconductance is given by

$$g_{mi} = v_s Z \frac{q N \varepsilon_s}{2(V_{bi} - V_{GS})} \qquad (2.8)$$

where Z is the gate width in cm, ε_s is the permittivity of GaAs, q is the electronic charge in coulombs, N is channel doping in cm^{-3} and V_{bi} is the built-in voltage of the gate-channel Schottky diode. The equation 2.8 predicts that the intrinsic transconductance is maximum near zero gate bias.

The maximum frequency at which an FET can amplify the signal power is an important figure of merit for microwave amplifiers and is given by:

$$f_{max} = \frac{f_t}{2[G_o(R_G+R_S)+2\pi f_t C_{DG} R_G]^{0.5}} \qquad (2.9)$$

where C_{GD} is the gate-drain capacitance in Farads and G_o is the output conductance of the FET in siemens (S). As seen in equation 2.9, f_{max} includes parasitic elements of the FET, so it may be considered as a better indicator of the high frequency capability of the FET.

A quick look at the analytical relationships describing the high frequency figures of merits of an FET reveals that parasitic resistances and capacitances are detrimental to the high frequency performance. The f_t can be increased by increasing the transconductance which in turn can be improved by increasing channel doping. An increase in the channel doping is accompanied by an increased gate capacitance. Thus, the overall ratio of g_m and C_{GS} remains unaffected. So, the gate length must be reduced for increasing the unity current gain frequency f_t. The f_{max} can be improved by reducing the parasitics such as source and drain resistances as well as gate-source and gate-drain capacitances. The source and the drain resistances have two components: the contact resistance R_c between the ohmic metal and the semiconductor, and the sheet resistance R_s of the semiconductor. An ohmic contact to a heavily doped layer of GaAs on a lower doped channel layer can reduce both to give low source resistance. As shown in Figure 2.4(d), the heavily doped contact layer must be removed before putting down the Schottky gate metal. The process of removing heavily doped contact layer is termed as 'gate recess etch'. In a gate recess etch, the gate is first defined with photolithography and the highly conducting ohmic contact layer is etched using one of the etchants described in the Appendix with the source-drain current I_{ds} as an etch depth monitor. This is the most conventional epitaxial FET fabrication technique. Other approaches include FETs with refractory gates and self aligned, ion implanted source-drain ohmic contact regions, non-alloyed ohmic contacts with recessed gates,[8-9-10] and alloyed ohmic contacts without gate recess. A comprehensive review of GaAs MESFET gate fabrication technology is done by Weitzel, et al.[11] Each of these techniques with the exception of the self aligned gates have been tried in the course of this work.

The FETs can either be operated in enhancement mode or depletion mode. A depletion mode FET has a conducting channel present at a zero gate bias and with application of negative gate bias, the channel can be gradually pinched-off. The enhancement mode FETs have much thinner channel compared to the depletion mode FETs. The channel is completely depleted of electrons at zero gate bias because of the built-in field of the gate-channel Schottky diode and the FET is normally off. With application of small positive gate voltage, sufficient to forward bias the gate-channel Schottky diode, the FET is turned on. The enhancement mode devices are particularly useful for low power digital circuits.

2.2.1 Evaluation of FET Parasitic Resistances

FET parasitic resistances include source resistance R_S, gate resistance R_G and drain resistance R_D. The gate resistance is the resistance of the gate metal. The source/drain resistance includes the contact resistance between the ohmic metal and the semiconductor layer (R_c) as well as the sheet resistance (R_{sh}) of the semiconductor layer.[12] The sheet resistance has two components: R_{sh1}, sheet resistance of the semiconductor directly under the contact, and R_{sh2}, sheet resistance of the semiconductor between the two contacts.

The total contact resistance is given by

$$R = 2\,R_c + \frac{R_{sh2}\,L}{W} = \frac{2\,R_{sh1}\,Lt}{W} + \frac{R_{sh2}\,L}{W} \qquad (2.10)$$

where R_c is contact resistance, W is contact width, L is contact length and Lt is contact transfer length. The R_c can either be evaluated by measurements on a planar transmission line pattern[13-14] or a vertical Kelvin resistor.[15-16-17] A transmission line pattern consists of several ohmic contacts to a semiconductor bar with different spacings between them (Figure 2.1(a)).

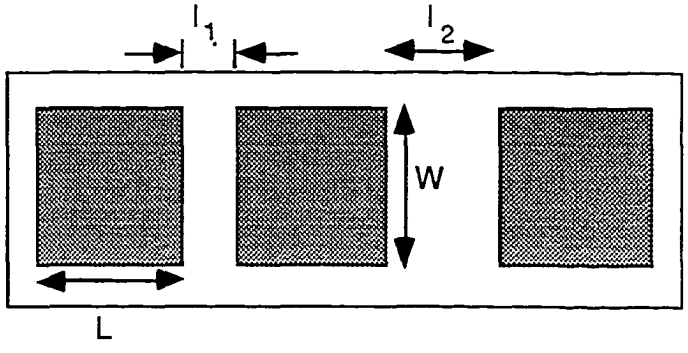


Figure 2.1(a): A transmission line pattern for ohmic contact resistance evaluation

Resistance between two adjacent pair of contacts is measured and plotted against the contact spacing. Extrapolation of straight line to the zero contact spacing gives twice the value of R_C and the slope of the line gives the sheet resistance R_{sh} of the semiconductor (Figure 2.1(b)). The contact resistivity ρ_c is given by

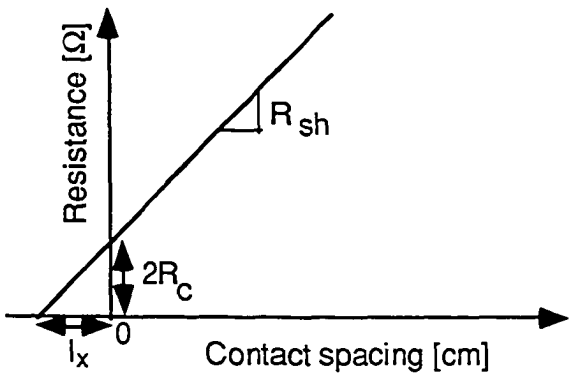


Figure 2.1(b): Contact resistance evaluation by transmission line technique

$$\rho_c = \frac{1}{2} R_C W l_x \qquad (2.11)$$

where l_x is as shown in figure 2.1(b), related to contact transfer length L_t by the following relation:

$$l_x = \frac{2 R_c W}{R_{sh2}} = \frac{2 R_{sh1} L_t}{R_{sh2}} \qquad (2.12)$$

The contact resistance evaluation by the TLM technique is quick when $L_t << L$ but not very accurate because of the uncertainty in measurement of the small gap between the ohmic contact pads shown in Figure 2.1(a). The contact resistance thus obtained is of limited use because the TLM does not accurately represent actual conditions in an FET. The TLMs are made on highly doped layer where surface depletion effect can be neglected, whereas in an actual FET, the gate is placed in a recess (Figure 2.4(e)) on a lower doped channel. So, the effect of surface depletion is considerable and the source/drain resistance obtained from TLM can be significantly different from the actual R_S and R_D. The technique described in the following paragraph can be used to obtain the source and the drain resistances fairly accurately.

The setups for R_{GS} and R_{GD} measurement are shown in Figures 2.2(a) and (b), respectively, with equivalent circuits. As shown in the setups, a constant current is injected into the gate and the potential drop across drain-source terminals is measured. The gate current must be high enough to forward bias the gate-channel Schottky diode. With this technique absolute values of the source and the drain resistances cannot be obtained because $0.5R_{ch}$ is included in the measurements.

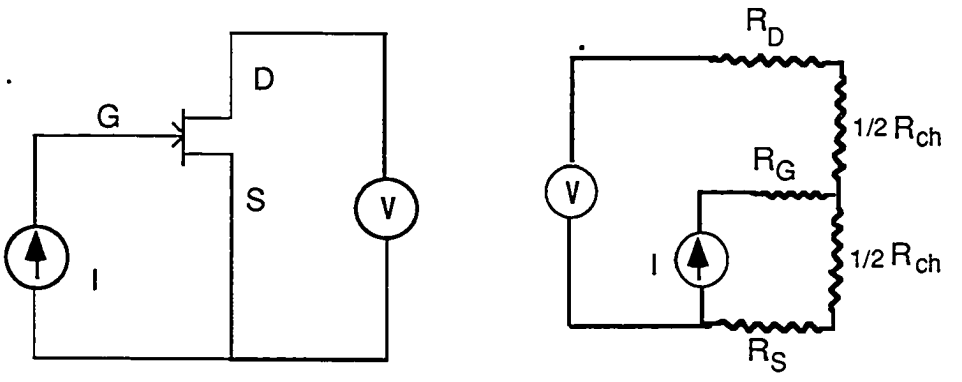


Figure 2.2 (a): A schematic and equivalent circuit of a measurement setup for R_{GS} extraction

Extraction of the absolute source and drain resistances requires R_{GS} and R_{GD} measurements on a set of FETs with different gate lengths. Next, the measured resistances are plotted as a function of gate length and the Y-axis intercept gives true source or drain resistance.[18]

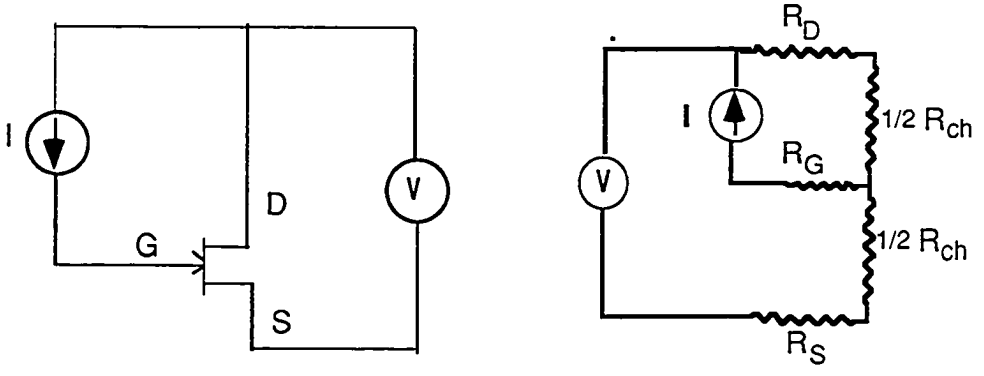


Figure 2.2 (b): A schematic and equivalent circuit of a measurement setup for R_{GD} extraction

2.3 Review Of ELO Technology

Promise of reusing a growth substrate for low cost, thin film GaAs solar cells[19] was initially the reason for developing ELO technology. It was soon followed by the first ELO GaAs MESFET[20] operating at microwave frequency, made on a glass substrate by selective etching[21] of the growth substrate from epitaxial layers of MESFET. For historic purpose, it should be noted here that the concept of removing growth GaAs substrate by selective etching of a sacrificial layer of Ga_{1-x} Al_x As ($x > 0.6$) was first described by Stern, et al, in 1974.[22] The first ever published account of removing an epitaxially grown

GaAs layer by selective etching of AlGaAs and bonding it onto a glass substrate for making a photocathode appeared in 1975.[23] However, it took almost one and a half decade to optimize[24] the ELO technique. The credit for optimized lift-off also belongs to improvement in the epitaxial growth techniques enabling growth of high purity, thin, AlAs sacrificial layer. A reason for the renewed interest in the ELO is the possibility of integrating photodetectors[25] and lasers with glass or lithium niobate wave guides for optoelectronic integrated circuits. The most attractive feature of the ELO is its promise of grafting semiconductors on an arbitrary host without regards for compatibility of crystal structure and lattice matching. Most of the work on ELO with the exception of Chan, et al,[26] has been centered around preprocessing the devices and then lifting-off to a new host with minimum or no processing after lift-off.[27- 28] Preprocessing lends itself to the use of well established GaAs processing techniques. High temperature processing also does not pose any problem unlike the postprocessing. On the otherhand, postprocessing of lift-off GaAs film as described by Chan, et al., facilitates photolithographic accuracy in alignment of the grafted devices to the substrate features. It will be shown later that excellent device isolation with negligible sidegating is obtained with postprocessing of ELO GaAs MESFETs.[29] A similar isolation characteristics can be obtained with the preprocessed devices at the expense of considerable increase in processing.

2.4 Investigation of ELO GaAs FETs

To accomplish the goals of this thesis, a comprehensive study of ELO GaAs for MESFET and HEMT fabrication independent of GaAs substrate was undertaken. This section describes this study which was aimed at developing ELO FETs with reproducible and uniform characteristics suitable for small scale integrated circuits.

2.4.1 ELO GaAs MESFETs

ELO MESFET fabrication was initially done following a conventional fabrication process that is used for making on-wafer FETs. As mentioned in the introduction, this standard process has been modified following systematic experimental studies to suit the requirements of integrated circuit. Three different fabrication processes accompanied by appropriate epitaxial layer structures were investigated in this thesis, namely: MESFETs with alloyed contacts and recessed gates, with non-alloyed contacts and recessed gates, and with alloyed contacts but without recessed gates. Each of them has been described in the following sections along with their DC and RF characteristics.

2.4.1.1 Fabrication of GaAs MESFETs With Alloyed Ohmic Contacts and Recessed Gates

As mentioned in section two, gate recess enables us to keep the parasitic source and drain resistances to a low level in the FETs with n^+ GaAs layer for ohmic contacts. MESFETs with recessed gates were fabricated either on a silicon substrate covered with SiO_2 or SiN dielectric buffer or on polished sapphire substrate following an identical procedure. MESFETs were also fabricated on GaAs wafer following an identical fabrication process for studying effect of ELO on MESFET characteristics.

A MESFET structure consisting of a 100 nm thick n^+ cap, 200 nm n = 1 x 10^{17} cm^{-3} channel and 50 nm undoped AlAs sacrificial layer was grown on a semiinsulating GaAs substrate using MBE. On-wafer MESFETs were fabricated using an epitaxial layer structure consisting of a 100 nm n^+ = 2-3 x 10^{18} cm^{-3} ohmic contact layer, 500 nm n = 1 x 10^{17} cm^{-3} channel and 50 nm undoped AlAs sacrificial layer (if ELO was required), on a semiinsulating GaAs wafer by organo-metallic chemical vapor deposition (OMCVD).

The epitaxially grown MESFET layer structure was lifted-off from the GaAs substrate by selectively etching the AlAs sacrificial layer and transferred onto a sapphire substrate or a 5 Ω-cm resistivity, p-type, <100> oriented, Si substrate, typical of those used for NMOS/CMOS circuits, that has been covered either with ~250 nm of plasma enhanced chemical vapor deposited Si_3N_4 or with 1.5 μm of thermal oxide. The lifted-off film typically measured 0.5 cm x 1 cm and was held on the silicon substrate by Van der Waals forces. Figure 2.3 shows the ELO process sequence.

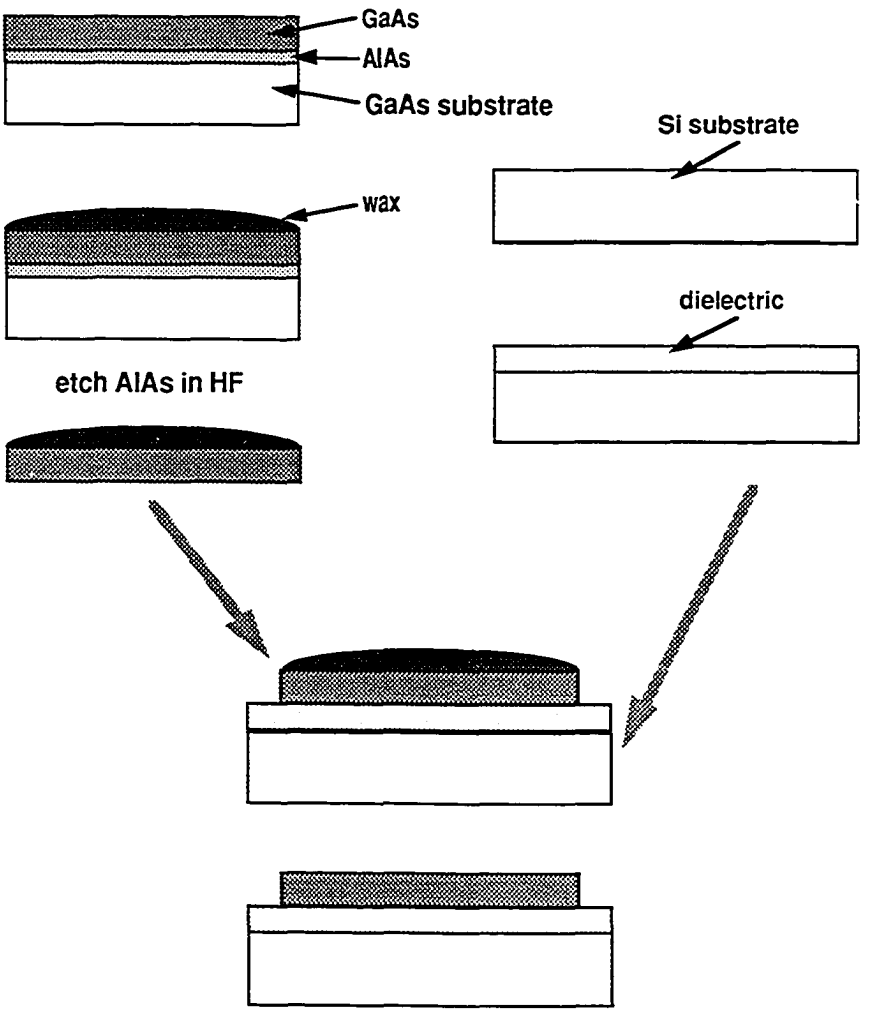


Figure 2.3 : ELO process sequence

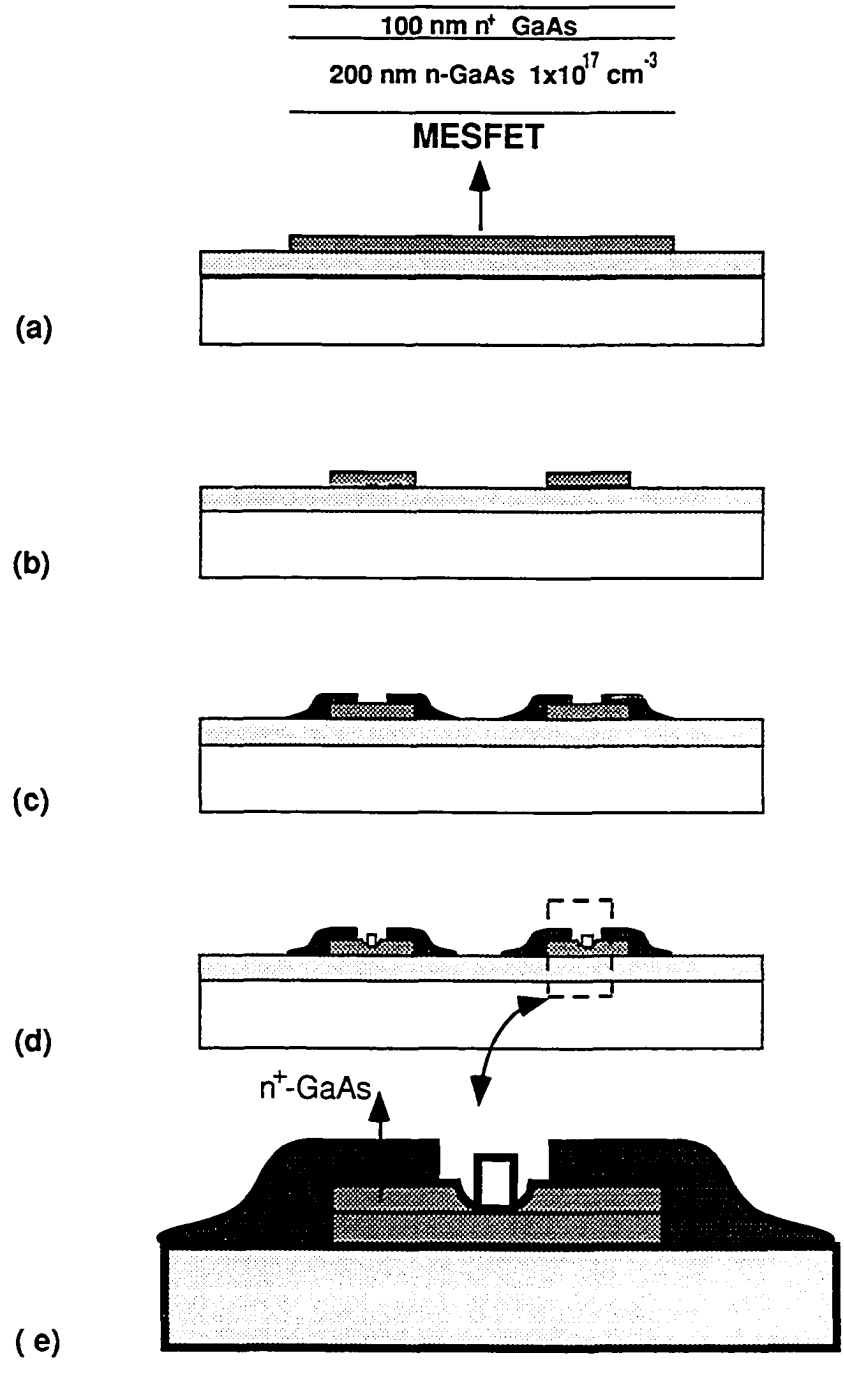


Figure 2.4: ELO GaAs FET process sequence
(a) ELO GaAs FET layer bonding to SiO_2/Si (b) Mesa isolation
(c) Ohmic contacts (d) Gate formation (e) Magnified view of the details of gate recess shown in (d)

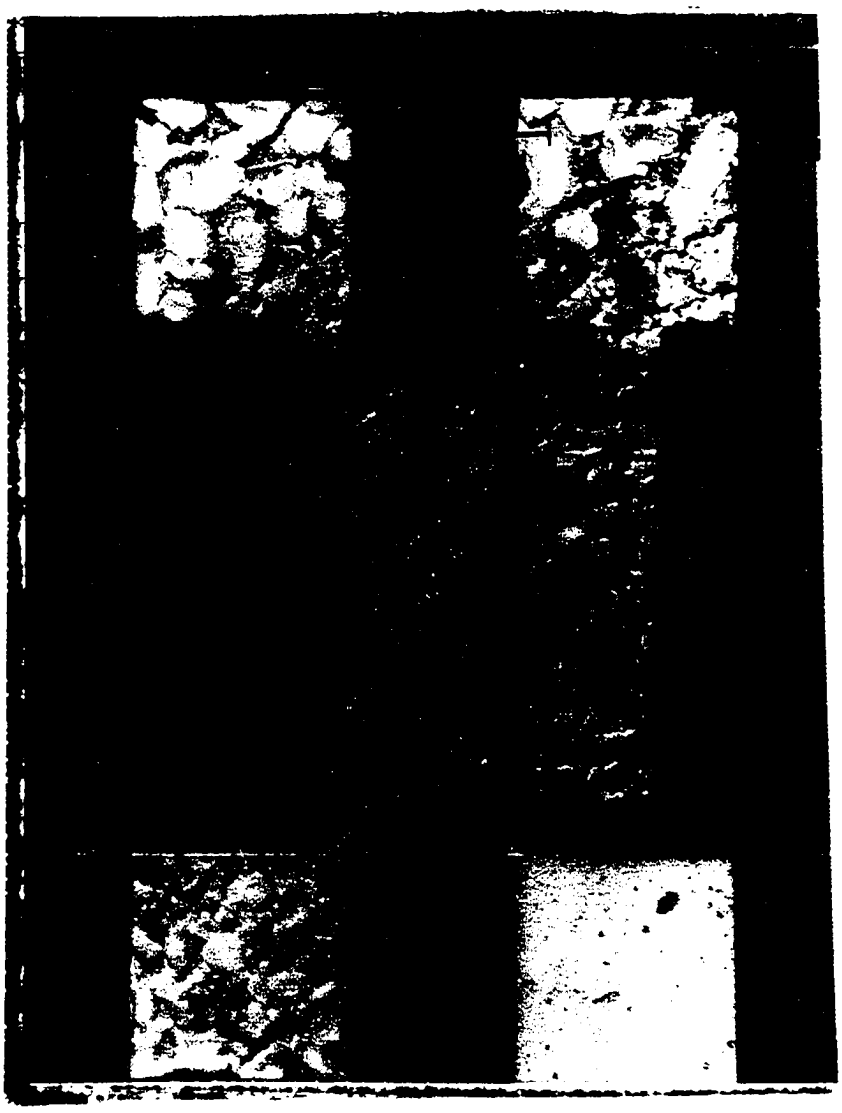


Figure 2.5: A photomicrograph of an ELO GaAs MESFET on Si with gate length of 1 μm and gate width of 100 μm

The MESFETs were fabricated following a standard procedure (Figure 2.4) comprising of mesa etch in a solution of 1 H_2SO_4 :8 H_2O_2 :500 H_2O for isolation; NiAuGe source-drain ohmic contact formation by photolithography, evaporation and lift-off; contact alloy at 420°C for 20 seconds under flowing argon; gate recess etch for I_{dss} adjustment; and Ti/Au Schottky gate metallization. A photomicrograph of a typical ELO MESFET is shown in Figure 2.5.

2.4.1.2 DC and RF Characteristics of MESFETs With Alloyed Contacts and Recessed Gates

DC parameters of the MESFETs on silicon, sapphire and GaAs substrates were obtained with an HP 4145 parameter analyzer. Current gain and power gain (maximum available gain, MAG) of the MESFETs at radio frequency (RF) were obtained using a Cascade prober and HP 8510 network analyzer.

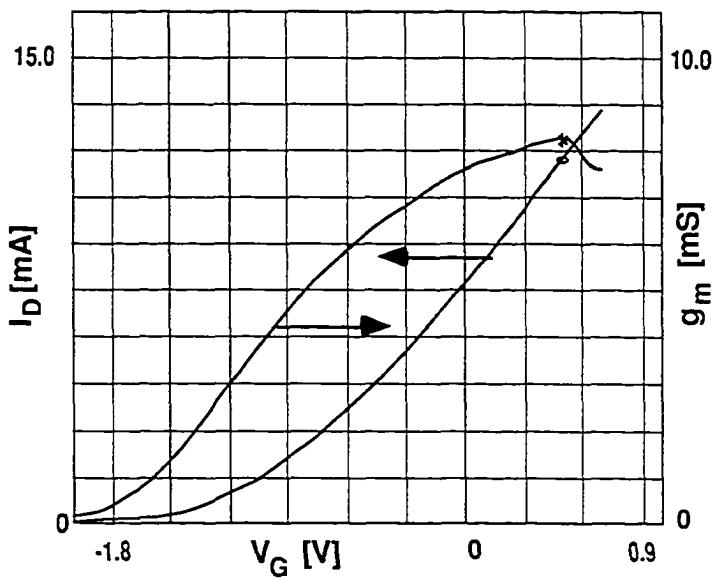


Figure 2.6(a) DC Transfer characteristics of an on-wafer GaAs MESFET with W_g = 100 μm, I_{dss} = 75 mA/mm, $g_{m\text{-}max}$ = 82 mS/mm, and V_P = -2V

2.4.1.2.1 DC and RF Characteristics Of On-wafer MESFETs

An on-wafer MESFET had a saturated drain current I_{dss} = 75 mA/mm, a maximum transconductance g_m = 82 mS/mm at V_{GS} = 0.5 V, and a pinch-off voltage V_P = -2 V (Figure 2.6(a)). The MESFET had a gate-source resistance R_{GS} = 3.2 Ω-mm, gate-drain resistance R_{GD} = 4.2 Ω-mm and contact resistance R_c = 0.75 Ω-mm. Figure 2.6(b) shows an unity current gain frequency f_t = 13 GHz and a maximum frequency of oscillation, f_{max} = 16 GHz for a 1.1 μm gate length MESFET. These are typical for GaAs MESFETs with this gate length.

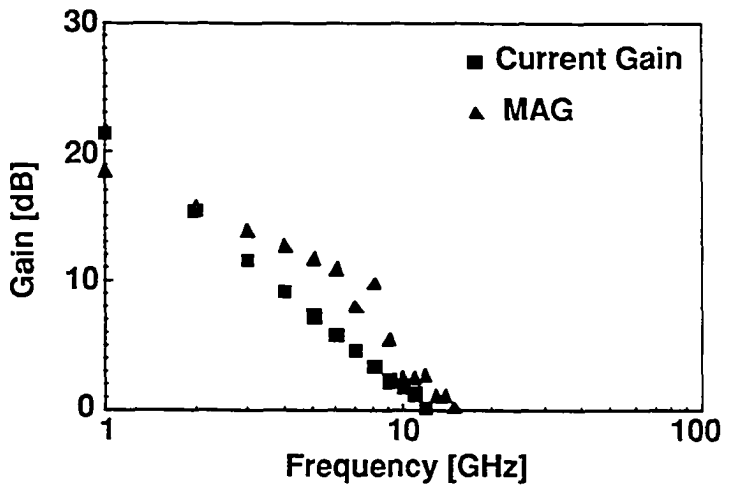


Figure 2.6(b) RF characteristics of on-wafer GaAs MESFET with gate length L_g = 1.1 μm, f_t = 13 GHz, f_{max} = 16 GHz

2.4.1.2.2 ELO MESFETs on 1.5 μm Thick Thermal Oxide

The MESFETs had a source-drain spacing of 4 μm and a gate-source spacing of ~0.5 to 1.0 μm with a gate length of 1.5 μm. The contact resistance as measured from transmission line testers ranged from 0.075 Ω-mm to 0.22 Ω-mm. The MESFETs had a saturated drain current I_{dss} of 130 mA/mm, a maximum extrinsic transconductance g_m = 135 mS/mm at V_{GS} = 0 V and a pinch-off voltage V_P of -1.6 V (Figure 2.7). The avalanche breakdown of the channel occurred at V_{DS} = 3 V, a relatively low voltage, and is attributed to a highly doped (2 x 10^{19} cm^{-3}) n^+ layer for ohmic contacts. Devices fabricated later with lower doping in the ohmic contact layer had a substantially higher channel breakdown voltage.

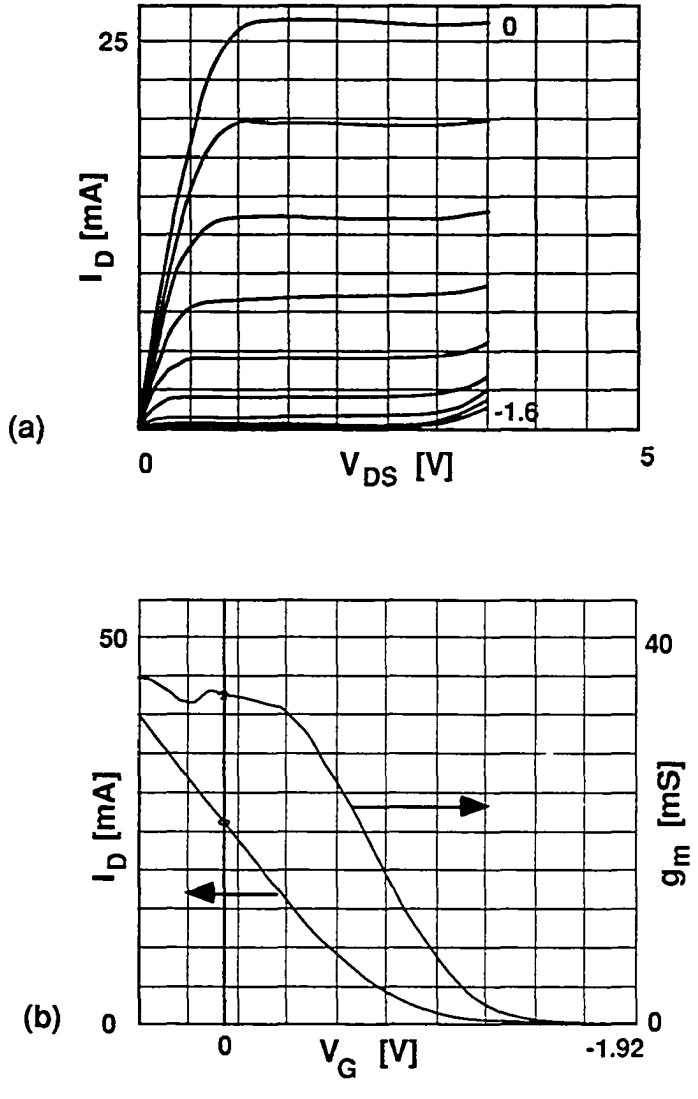


Figure 2.7 (a): Typical drain I-V characteristics and (b) DC transfer characteristics of an ELO MESFET with 250 μm gatewidth on 1.5 μm SiO_2/Si with alloyed contacts and recessed gates. I_{dss} = 130 mA/mm, $g_{m\text{-}max}$ = 135 mS/mm.

Figure 2.8 shows an unity current gain frequency f_t of 12 GHz and a maximum frequency of oscillation f_{max} of 14 GHz for a MESFET with a 1.3 μm long and 100 μm wide gate, typical frequencies for a GaAs MESFET of these dimensions fabricated on a GaAs substrate.

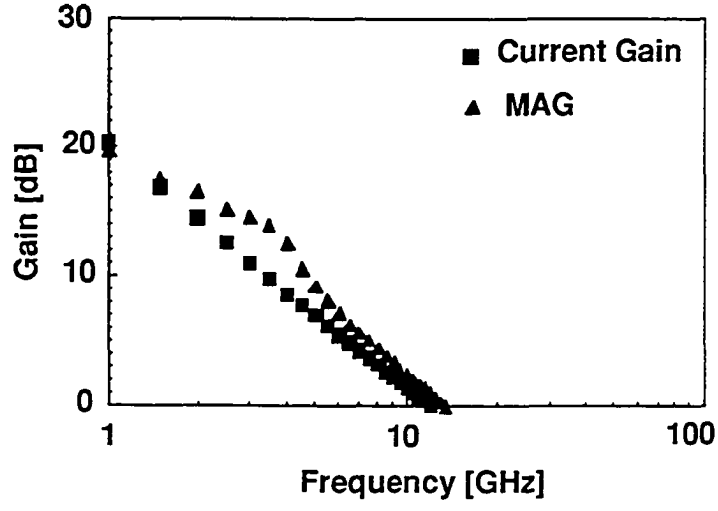


Figure 2.8: RF characteristics of an ELO MESFET on SiO_2/Si with L_g = 1.3 μm. f_t = 12 GHz, f_{max} = 14 GHz.

With the thick thermal oxide, the parasitic gate pad capacitance to the p-type silicon substrate becomes negligible and the speed is dominated by the intrinsic gate capacitance. It will be seen in the next section that the dielectric buffer layer thickness plays a dominant role in the high frequency operation of ELO FETs.

The RF output conductance was obtained by fitting the measured S-parameters to an equivalent circuit model and was ~1 mS for a 100 μm wide device from 0.5 to 10 GHz, typical for GaAs MESFETs on GaAs substrates. In MESFETs made on the GaAs substrate, injection of hot electrons from the channel into the substrate is an important source of output conductance, but in our case, this is eliminated by the large SiO_2 barrier of ~7-9 eV under the channel that confines electrons in the channel under normal biasing conditions. Traps in the semiconductor or at the semiconductor/dielectric buffer, therefore, are believed to contribute to the output conductance. Further study is required to determine the exact conduction mechanism.

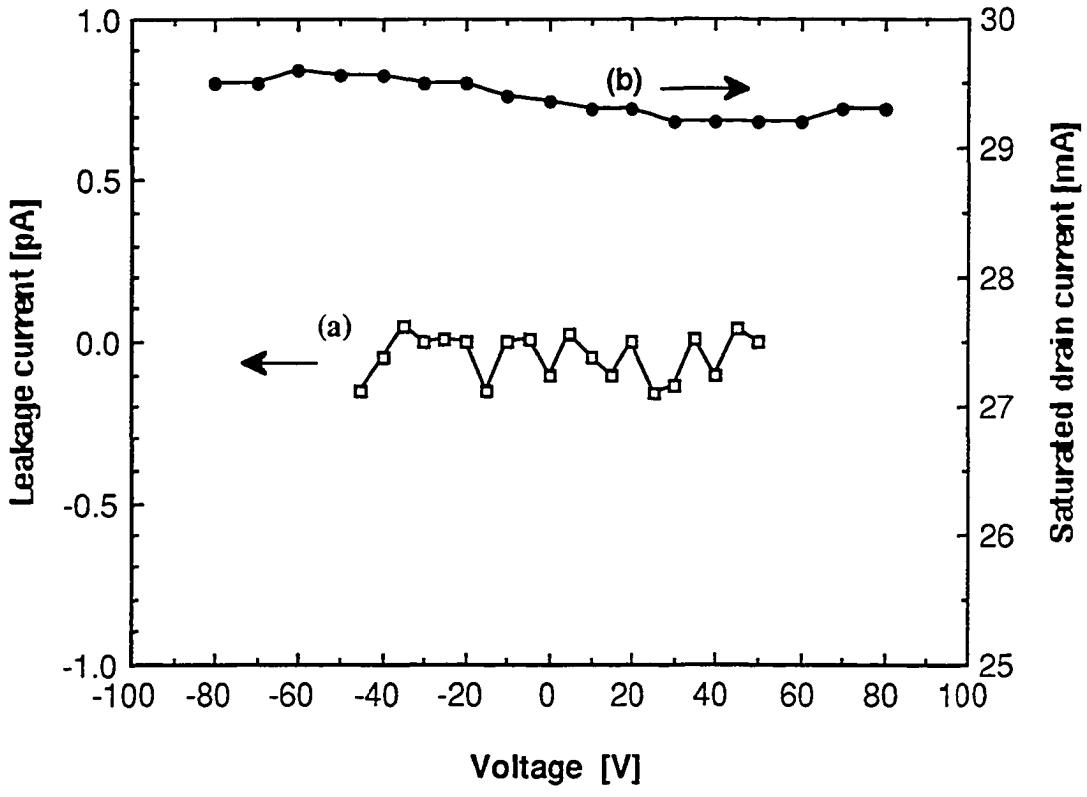


Figure 2.9: (a) Leakage current between two pads 200 μm wide and 20 μm apart (b) Sidegating characteristics of an ELO MESFET showing < 1% change in I_{dss} over ±80 V on a side gate located 50 μm away from FET

As seen in Figure 2.4, the devices are fabricated on completely isolated mesas of GaAs, which has resulted in an extremely low sidegating and excellent electrical isolation between devices because of the insulating buffer layer. Figure 2.9(a) shows subpicoampere leakage current, which was noise limited, between two pads 200 μm wide and 20 μm apart for an applied bias of ± 50 V. For comparison, typical leakage currents on a GaAs substrate are a nanoampere or more at substantially lower biases. For MESFETs fabricated on the semiinsulating GaAs substrates, drain current modulation or sidegating, caused by surface leakage currents resulting from traps at the substrate surface[30] gives rise to cross talk between neighboring devices. This is largely eliminated as well since the application of ±80 V to a side gate 50 μm away from the gate of an FET produced < 1% change in I_{dss} (Figure 2.9(b)). Dielectric breakdown of the 200 nm silicon nitride buffer at 80 V limited

the measurement to this voltage. Residual drain current modulation may be from capacitive coupling to the conducting Si substrate.

2.4.1.2.3 Submicron Gate ELO GaAs MESFETs on Thin Silicon Nitride

The epitaxial layer structure for the MESFETs consisted of a 100 nm thick, n^+ (2 x 10^{18} cm^{-3}) cap and a 200 nm thick n = 2 x 10^{17} cm^{-3} GaAs channel. This layer structure is identical to the previous one except the doping in the cap layer. The doping level in the cap layer was reduced by an order to improve the channel breakdown voltage. MESFETs with 0.1, 0.2 and 0.4 μm gate lengths were fabricated after transferring the MESFET layers onto a silicon substrate covered with ~0.25 μm thick, plasma enhanced chemical vapor deposited silicon nitride buffer layer. Fabrication procedure was identical to that described in the previous section except the gate lithography. The submicron gates were defined by electron beam lithography and remaining process was identical to the photolithographically defined gates.

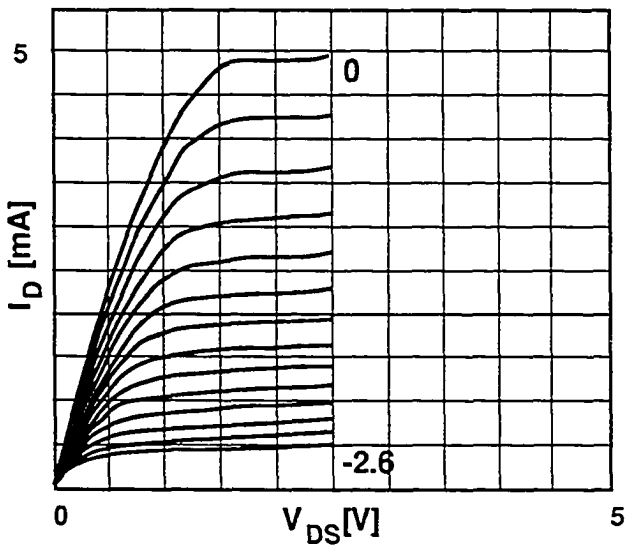


Figure 2.10: Drain I-V characteristics of a 0.1 μm gate length ELO MESFET on 0.25 μm thick SiN/Si with W_g = 50 μm, I_{dss} = 98.2 mA/mm, $g_{m\text{-}max}$ =75 mS/mm. V_G; -0.2 V/step

A MESFET with 0.1 μm gate length and 50 μm gate width, operated in depletion mode, had an I_{dss} = 98.2 mA/mm, a maximum transconductance g_m = 75 mS/mm at V_{GS} = 0 V. The channel was not completely pinched off at -2.6 V (Figure 2.10). The gates tend to burn-out at higher gate biases due to excessive heating. MESFETs with 0.4 μm gate length could be completely pinched-off.

Figure 2.11 shows a unity current gain frequency f_t of 34 GHz and a maximum frequency of oscillation f_{max} = 23 GHz for a 0.1 μm gate length device. The f_t has not scaled up in proportion with the ten fold scaling down of gate length because of parasitic capacitance between the gate pad and the conducting silicon substrate.

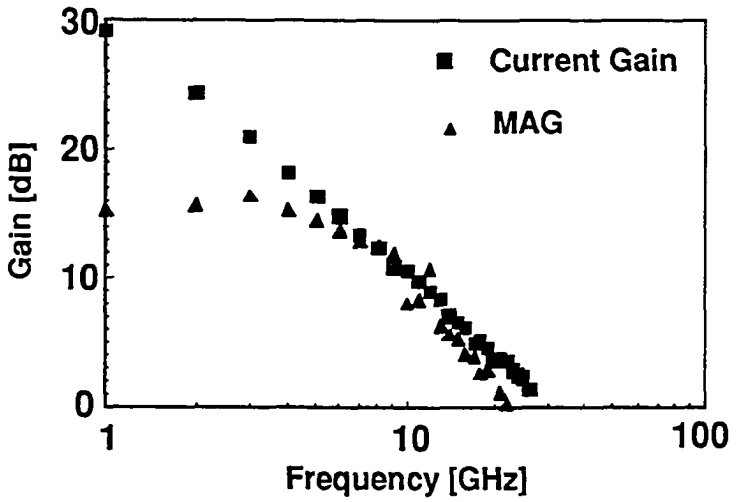


Figure 2.11 : RF characteristics of 0.1 μm gate length ELO MESFET on 0.25 μm SiN/Si showing f_t = 34 GHz and f_{max} = 23 GHz.

These results do not reflect true performance of a submicron gate device because the distance between the source and the drain (4 μm) electrodes was not reduced with the gate length reduction. So the extrinsic transconductance has suffered from the high parasitic source resistance. Nevertheless, this is an impressive rf performance for an ELO MESFET.

2.4.1.2.4 ELO GaAs MESFETs on Sapphire

Sapphire is a popular substrate for millimeter wave integrated circuits because of low signal loss in the sapphire substrate at these frequencies. Because of the large mismatch in the lattice constants of the two and differences of their crystal structures, the GaAs layers grown directly on sapphire have large number of dislocations. Single crystal GaAs FET layers can be bonded to sapphire substrate using ELO to obtain superior device performance as compared to the directly grown FETs. ELO GaAs MESFETs described in this sections were developed with the above considerations.

The epitaxial layer structure used for these devices was same as the one used for submicron gate MESFETs described in the previous section. MESFET fabrication was also done following the procedure identical to the one described earlier for the ELO MESFETs on thermal oxide.

An enhancement mode MESFET with 1.3 μm long and 100 μm wide gate had drain current I_{ds} = 108 mA/mm at V_{GS} = 1 V, pinch-off voltage V_p = -0.4 V and a maximum transconductance g_m = 100 mS/mm at V_{GS} = 0.6 V (Figure 2.12).

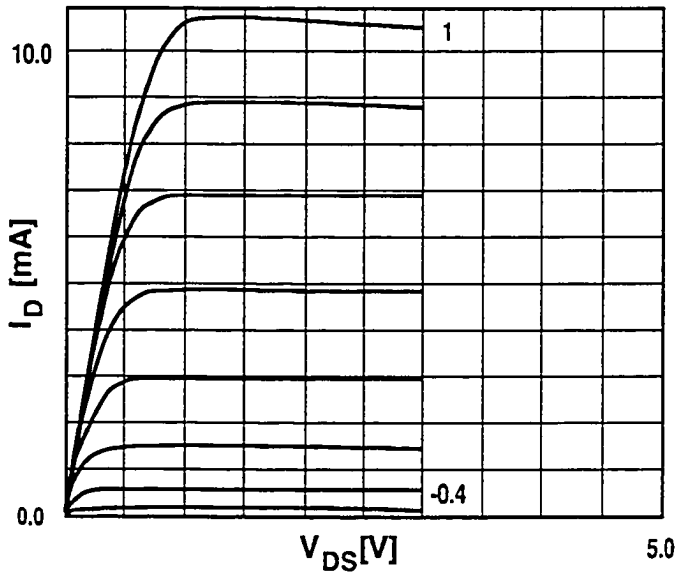


Figure 2.12: Drain I-V characteristics of an enhancement mode ELO GaAs MESFET on sapphire. W_g = 100 μm, I_{ds} = 108 mA/mm, $g_{m\text{-}max}$ = 100 mS/mm

Figure 2.13 shows an unity current gain frequency f_t = 8.5 GHz and a maximum frequency of oscillation f_{max} = 17 GHz for a 1.1 μm gate length MESFET. The reason for lower f_t is not known. A significantly higher f_{max} value may be from lower output conductance and lower signal loss in the sapphire substrate at microwave frequencies as compared to the conducting silicon substrate.

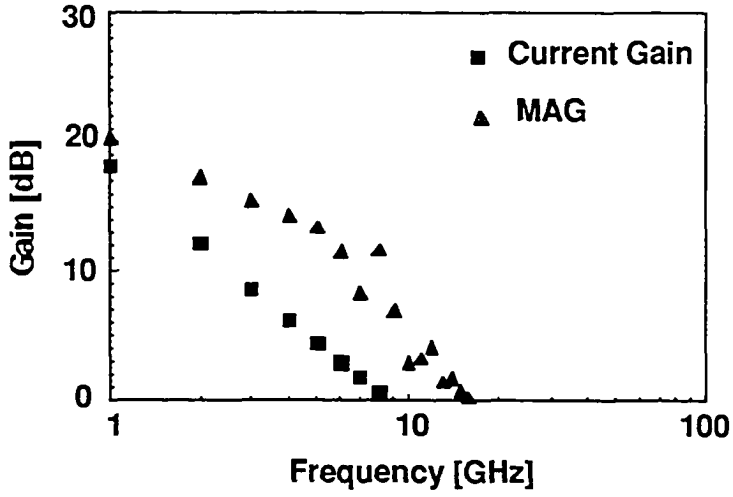


Figure 2.13: RF characteristics of an enhancement mode ELO MESFET on sapphire L_g = 1.1 μm, W_g = 100 μm, f_t = 8.5 GHz, f_{max} = 17 GHz

2.4.2 Problems Encountered While Processing ELO GaAs MESFETs

Two problems significantly limiting the yield of ELO GaAs MESFETs are blistering of the ELO GaAs during the ohmic contact annealing and adhesion of the ELO GaAs to the new host. These problems and their possible solutions are discussed in this section.

Blistering of GaAs film during high temperature ohmic contact annealing step due to vaporization of volatile impurities trapped at the substrate-film interface is a problem significantly affecting the yield of devices.[31] In our process, removal of most of the GaAs film in mesa etching step significantly reduces the number of sites for impurity trapping. It also confines the blistering induced damage to a considerably smaller mesa area (typical mesa dimensions are: 100 μm x 25-40 μm) as opposed to the whole ELO film. So, the number of devices affected by blistering are significantly lower. Figure 2.14 shows a 4 mm x 6 mm area ELO FET wafer with only local blistering.

Another problem encountered while working with the ELO GaAs is the adhesion of the ELO GaAs to the new host. It was found that the Van der Waals bonding of the ELO GaAs film to the new host is not always sufficient for holding the film to the substrate through the whole processing sequence which can involve several photolithographic, etch and metallization steps. This problem was solved by altering the conventional FET fabrication sequence. The mesas were 'tacked' down to the buffer layer with ohmic metal before their isolation[32] (Figure 2.15). As a result, a significant improvement in the testable

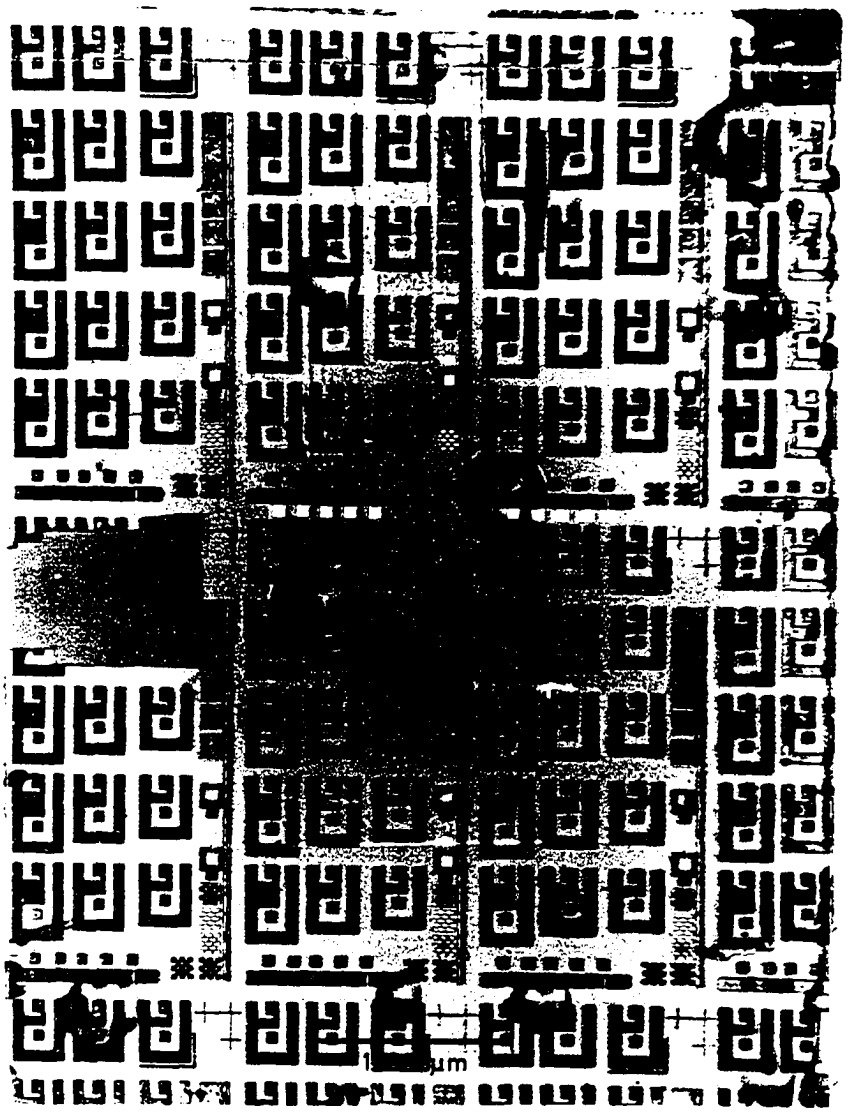


Figure 2.14: A photomicrograph of a 4 mm x 6 mm area ELO FET wafer showing only local blistering

device yield was obtained. Top and cross section views of the altered process are shown in Figures 2.15 and 2.16, respectively.

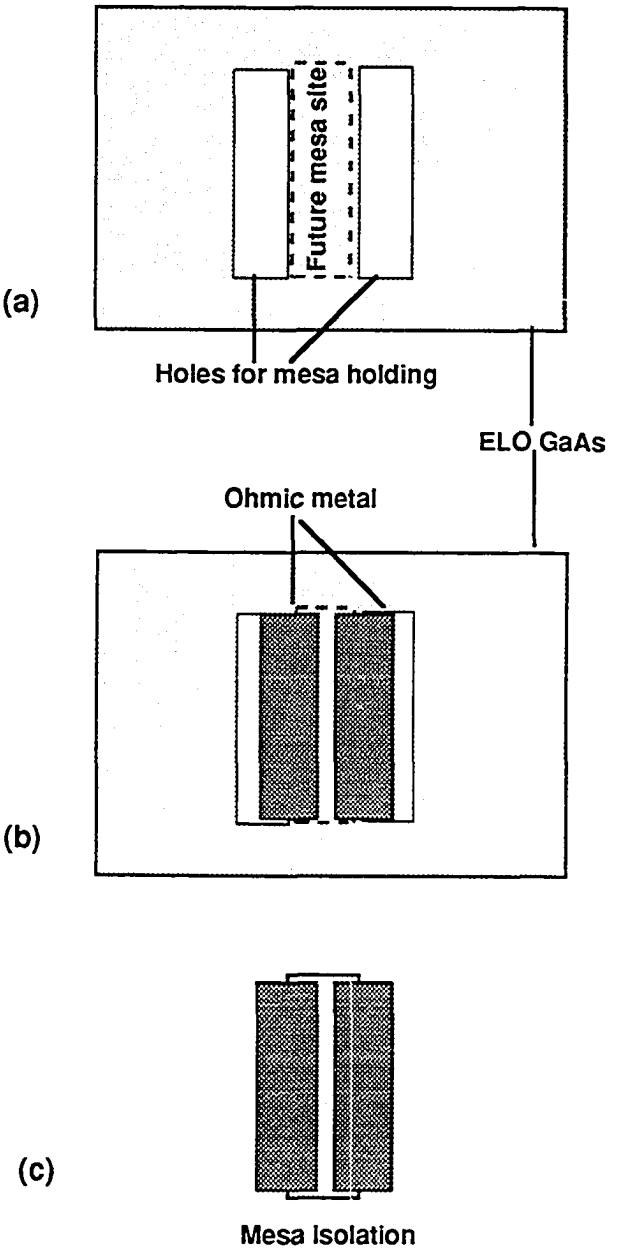


Figure 2.15: Top view of altered FET process with equal amount of ohmic metal on GaAs mesa and dielectric buffer

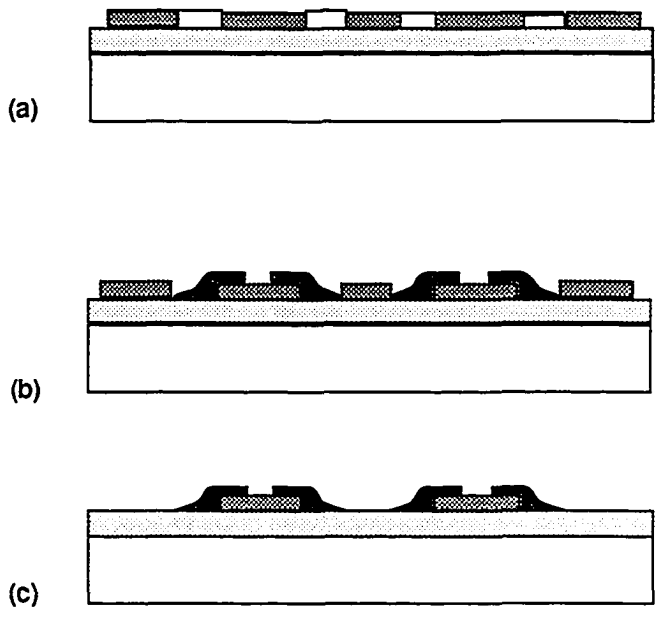


Figure 2.16: Cross sectional view of the altered FET process shown in Figure 2.15
(a) Hole etch next to 'future mesa' site (b) Ohmic metal deposition (c) Mesa isolation

In the previous section on ELO MESFET fabrication, the conventional NiAuGe ohmic contact metal was used to obtain low contact resistance. When the same contact metallization was used for contacting extremely narrow stripes of MESFET mesas in an amplifier circuit (to be discussed in the chapter 4), it was observed that the eutectic formed by AuGe alloy at the annealing temperature (typically 420°C) reacts with the ELO GaAs film and flows laterally in the space between the source and the drain contacts, causing an electrical short (Figure 2.17(B-2)). Energy dispersive X-ray analysis (EDX) on the alloyed samples confirmed presence of gold in the channel. AuGe contact alloy is known for its large vertical as well as lateral penetration in the GaAs substrate but the lateral flow over several μm is unusual. It was found that the alloy flow is directly related to the ratio of the insulating buffer area under ohmic metal to the area covered on GaAs mesa. The problem was most severe when the SiO_2 buffer and GaAs mesa area under the ohmic metal were comparable (Figure 2.15). A new mask designed later had about 10-15% ohmic metal on buffer without causing alloy flow (Figure 2.18).

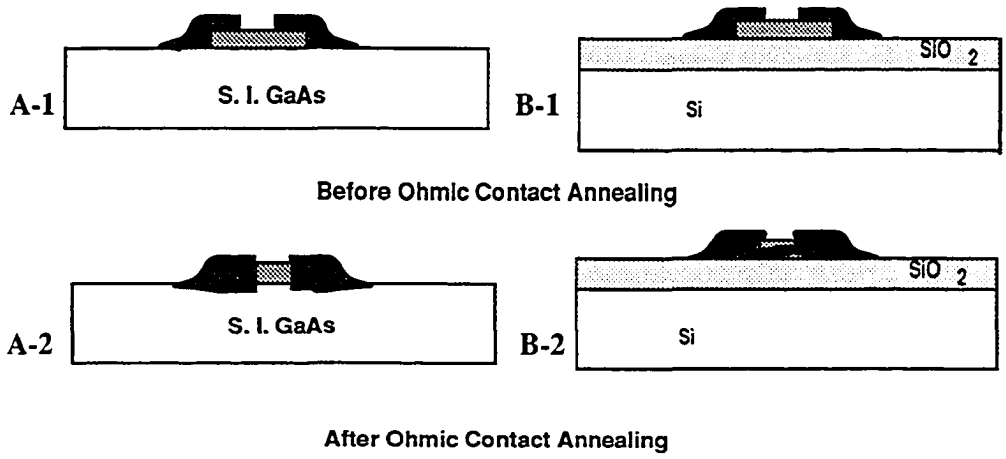


Figure 2.17: Illustration of AuGe ohmic contact alloy flow

A-1, A-2: AuGe Ohmic contact to FET on GaAs wafer,

B-1, B-2: AuGe Ohmic contact to ELO FET on SiO_2/Si

Alloy flow problem is unique to the ELO films grafted to the substrates covered with dense dielectrics. On annealing, the contact alloy first penetrates vertically into the film (as it would have in on-wafer contacts of Figure 2.17(A-2)) and when it reaches the virtually impervious dielectric buffer, it flows laterally and shorts the drain and the source contacts. Non-alloyed ohmic contacts described in the next section were developed to eliminate ELO GaAs blistering as well as alloy flow during annealing. Another problem with ELO GaAs processing is nonuniform wet chemical etching which is described in section 2.4.4.

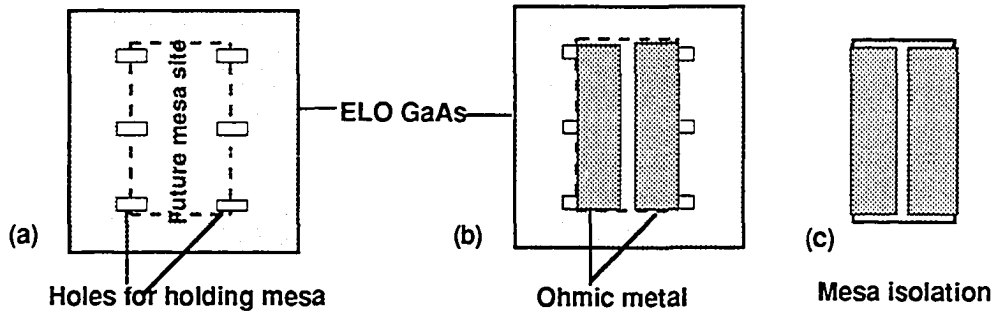


Figure 2.18: New FET process with only 15-20% ohmic metal on dielectric buffer

2.4.3 Development of Non-alloyed Ohmic Contacts

Two different contacting schemes were considered to address the need for a non-alloyed, shallow ohmic contact. The first one involved use of Pd/Ge solid phase reaction contacts.[33] These contacts are thermally stable over a wide temperature range of 250 to 550°C, are non-penetrating and have contact resistance similar to that obtained with the alloyed NiAuGe contacts when annealed at 400°C. The Pd/Ge contacts were not pursued further because the blistering of the ELO GaAs film at the annealing temperatures has not been completely eliminated. Several preliminary experiments also indicated that it would have required considerable amount of effort to reproduce the published results consistently in our laboratory at Bellcore.

The second contacting scheme uses a thin, heavily doped, graded, psuedomorphic layer of $In_xGa_{1-x}As$ on n^+ GaAs in the MESFET layer structure of the previous section. This contact was first proposed by Woodall, et al.[34] At room temperature, the surface Fermi level of InAs is pinned in the conduction band, so it provides low resistance path for electron flow, irrespective of the top metallization (Figure 2.19(a)). A graded layer of $In_xGa_{1-x}As$ is required for smooth transition of large (~0.66 ev) discontinuity in the conduction bands of the InAs and GaAs (Figure 2.19(b)). Without this graded layer the current flow will be limited by the large barrier at the InAs/GaAs interface. With a high n-doping in the InAs and GaAs layers and the compositional grading of the $In_xGa_{1-x}As$ layer, $\Phi_b < 0$ can be obtained as shown in Figure 2.19(c).

A test layer structure consisting of 25 nm n^+ In_x $Ga_{1-x}As$ (x = 0.13, 0.4, 0.7, and 1, each 6 nm thick), 200 nm n^+ GaAs (2×10^{18} cm^{-3}) and 400 nm n-GaAs ($n = 1 \times 10^{17}$ cm^{-3}), was grown on a semiinsulating GaAs substrate using OMCVD (Figure 2.20(a)). The $In_xGa_{1-x}As$ thickness was below the critical thickness that causes misfit dislocations. A transmission line pattern was fabricated by ion milling of mesas down to the semi insulating substrate, a subsequent evaporation of 5 nm Ti/300 nm Au in an electron beam evaporator and lift-off. Contact resistance was evaluated by four probe measurement technique on the transmission line pattern. As shown in Figure 2.20(b), Y-axis intercept of the linear extrapolation of the resistance as a function of contact spacing gives a contact resistance of 0.06 Ω-mm and a specific contact resistivity of 7.5×10^{-7} Ω–cm^2. This is comparable to the best reported results in literature.[8-9-10]

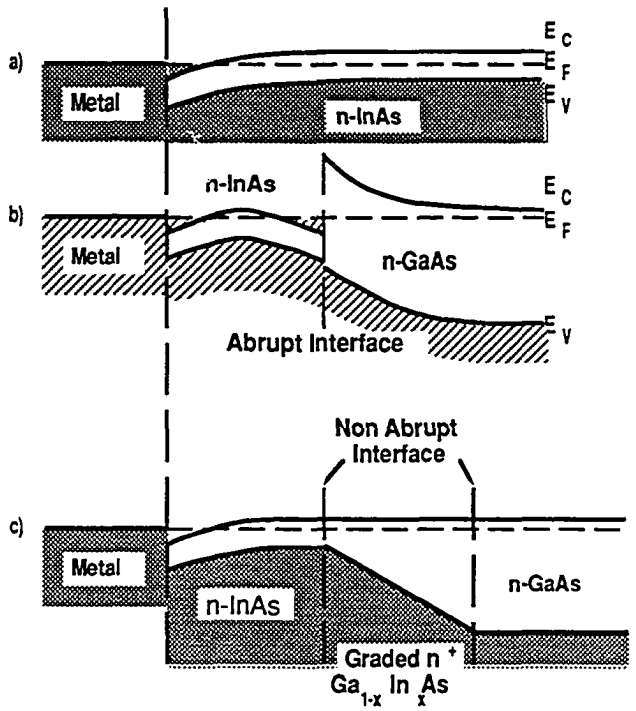


Figure 2.19: Band diagram of a non-alloyed ohmic contact to n-GaAs (a) Shows that any metal can make ohmic contact to n-InAs (b) Abrupt interface of n-InAs/n-GaAs due to conduction band discontinuity (c) A graded n-$In_xGa_{1-x}As$ layer makes ohmic contact to n-GaAs

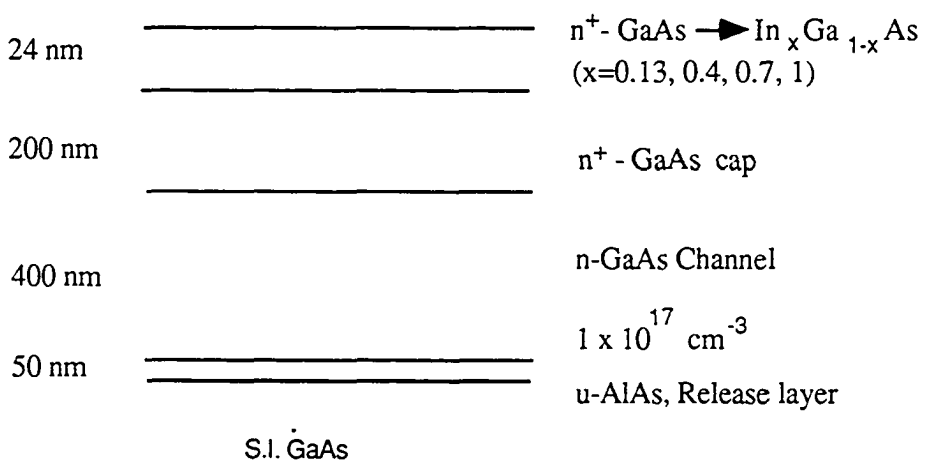


Figure2.20: (a) Epitaxial layer structure for MESFET with non-alloyed ohmic contact

A contact layer structure grown later with indium (In) content of up to 70% and without final layer of InAs had a similar contact resistance. Beyond ~70% In content in InGaAs, the Fermi level is pinned at the surface, so any further increase in In content does not improve the contact resistance.[35] Reduced indium content also helps improving the

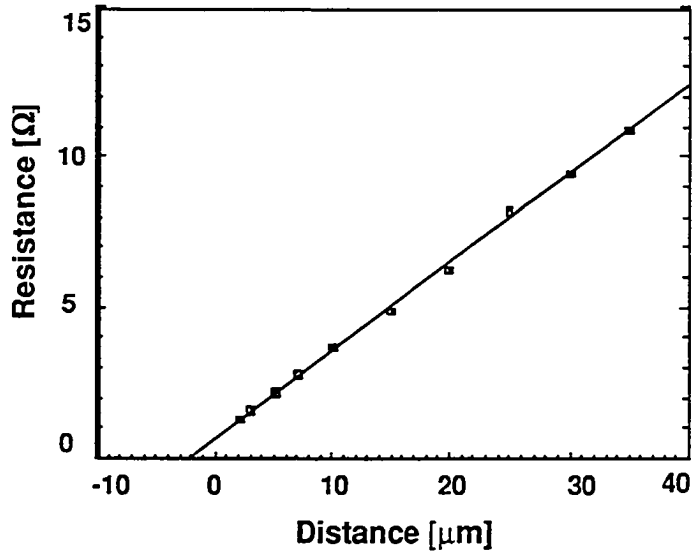


Figure 2.20: (b) Contact resistance characteristics obtained from four probe measurements on a transmission line fabricated in the epitaxial layer structure shown in Figure 2.20(a). Contact width 100 μm. R_c = 0.06 Ω–mm, $\rho_c = 7.5 \times 10^{-7}$ Ω–cm^{-2}

surface morphology of the strained layer which in turn improves uniformity of wet chemical etching. It should be noted here that in our scheme of non-alloyed contacts, the n^+-GaAs to n^+-GaInAs was step graded as opposed to the more popular continuous grading. With the step grading of the In content, material growth is simplified without significant increase in the contact resistance.

2.4.3.1 Fabrication of MESFETs With Non-alloyed Ohmic Contacts

Enhancement and depletion mode MESFETs were made on GaAs wafer as well as ELO GaAs on silicon substrate using the epitaxial layer structure described in the previous section. MESFET fabrication was done following a standard fabrication procedure involving mesa etch down to semiinsulating GaAs or silicon dioxide dielectric buffer layer by ion milling, 5 nm Ti/ 200 nm Au ohmic contacts by electron beam evaporation and lift-

off, 10 nm Ti/ 14 nm Au gate metal evaporation and lift-off following gate definition by photolithography and recess etch in 1 H_3PO_4 : 1 H_2O_2 : 38 H_2O and 1 H_2SO_4 : 8 H_2O_2 : 500 H_2O solutions.

2.4.3.2 DC Characteristics of an ELO MESFET With Non-alloyed Contacts

A depletion mode ELO MESFET with 1.5 μm long gate had I_{ds} = 180 mA/mm, maximum extrinsic transconductance g_m of 180 mS/mm at V_G = 0.8 V and pinch-off voltage V_p = -1.6 V as shown in Figure 2.21. Contact resistance R_C and specific contact resistivity as obtained from four terminal measurements on a transmission line tester were 0.15 Ω-mm and 5.25 x 10^{-6} Ω-cm^2 respectively.

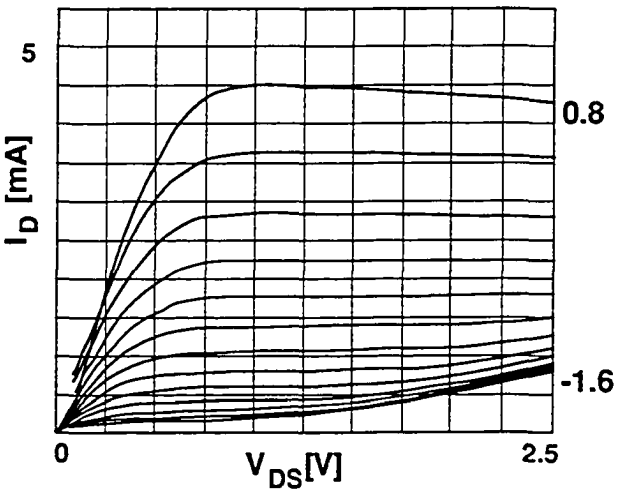


Figure 2.21: Drain I-V characteristics of an ELO GaAs MESFET with non- alloyed contacts. Gate width W_g = 25 μm. I_{ds} = 180 mA/mm, $g_{m\text{-}max}$ = 180 mS/mm. Scale:V_{GS}, -0.2 V/step.

An enhancement mode MESFET made on a GaAs wafer with 1 μm long gate had I_{ds} = 77 mA/mm, maximum extrinsic g_m = 100 mS/mm at V_G = 0 V and pinch-off voltage V_P = -0.2 V.

2.4.3.3 RF Characteristics of an ELO MESFET With Non-alloyed Contacts

Figure 2.22(a) shows a transfer characteristics of an enhancement mode MESFET with the non-alloyed ohmic contacts. Current gain and maximum available gain as a function of frequency for the same MESFET are shown in Figure 2.22(b). A unity current gain frequency f_t = 12.5 GHz and a maximum frequency of oscillation f_{max} = 7.5 GHz is obtained for the 1 μm gate length MESFET operated in enhancement mode at V_{GS} = 0.5 V. The MESFET had a maximum transconductance g_m = 201 mS/mm, gate source resistance R_{GS} = 0.55 Ω-mm, and gate-drain resistance R_{GD} = 1.1 Ω-mm.

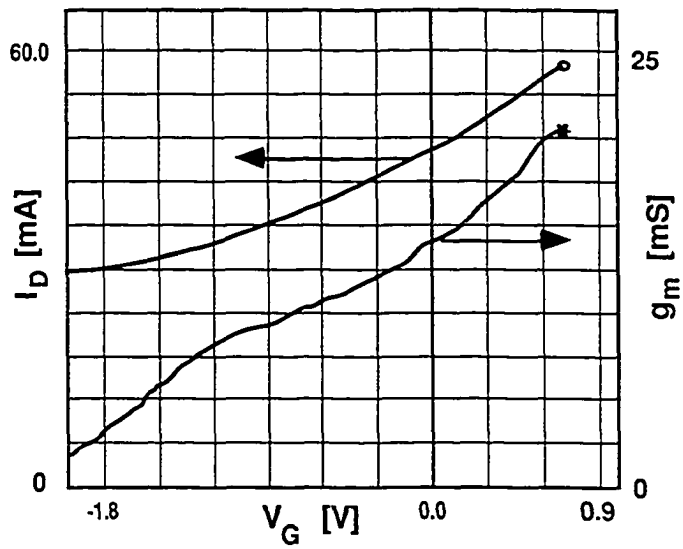


Figure 2.22(a): DC Transfer characteristics of an ELO MESFET on SiO_2/Si with non-alloyed contact. $g_{m\text{-}max}$ = 201 mS/mm. Gate width W_g = 100 μm

2.4.4 Development of MESFETs and HEMTs Without Recessed Gates

The DC and RF characteristics of the MESFETs described in the previous two sections are as good or in some instances even better, as compared to those made on the GaAs wafer. However, the single processing step significantly limiting the yield of FETs with uniform electrical characteristics across a wafer is the gate recess etch. This can be a serious limitation to the usefulness of the ELO FETs, especially for integrated circuits which require tight tolerance on device parameters. Various gate recess etches were tried, namely, 1 H_2SO_4 : 8 H_2O_2 : 500 H_2O, H_2O_2 : NH_4OH at pH 7.2, 1 H_3PO_4 : 1 H_2O_2 : 38 H_2O and ion milling. For the wet chemical etchants, nonuniformity in etch depth across a large area on a wafer is well known but for ELO GaAs films, it is more pronounced. For

example, when FET gates were recessed with the wet chemical etchants listed above, variation in saturated drain current across a 0.5 cm^2 area ELO sample was 50% or higher.

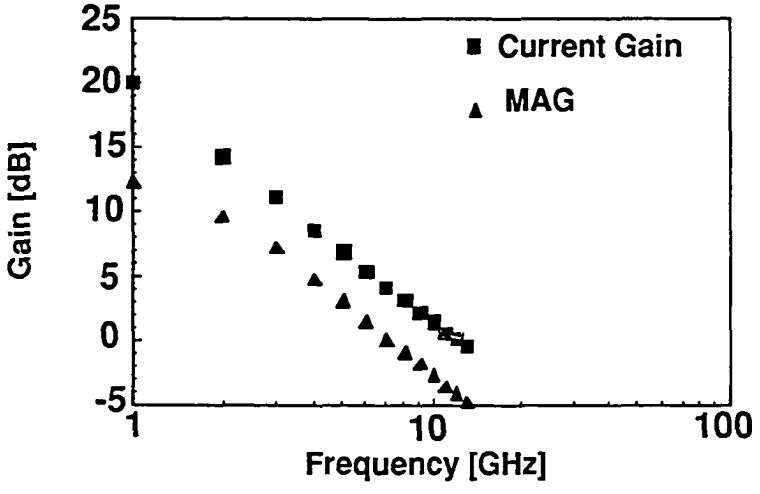


Figure 2.22: (b) RF characteristics of an ELO GaAs MESFET on SiO_2/Si with non alloyed contacts. L_g = 1 μm, f_t = 12.5 GHz, f_{max} = 7.5 GHz

Dry etching, as an alternative to the wet chemical etching for gate recess, was considered because very uniform etching over a large area and precise control of etch depth is possible with it. Reactive ion etching (RIE) and ion beam assisted etching (a more popular term is ion milling) are two alternatives available at present. Ion milling was preferred over RIE because of quicker turnaround in our lab at Bellcore. Ion milling (as described in the Appendix) was used on a MESFET layer structure with a 0.2 μm thick n^+ contact layer and 0.4 μm thick channel layer with a $N_D = 1 \times 10^{17}$ cm^{-3} so that for I_{dss} ~250 mA/mm the total recess depth was ~0.4 μm. The top 0.3 μm GaAs was removed by ion milling and the remaining 0.1 μm with wet chemical etching to remove damage induced by high energy ions because direct gate metallization on ion milled GaAs results into highly leaky Schottky barrier. It must be mentioned here that the RIE induced damage is comparable to the ion milling induced damage. The requirement of following the dry etching with a wet etch defeats the original purpose of using the dry etching for uniform gate recess. Therefore, it was not pursued further. ELO FETs without gate recess have been developed with these considerations.

2.4.4.1 Fabrication and Electrical Characteristics of MESFETs Without Recesed Gates

A MESFET layer structure consisted of a 300 nm thick 1 x 10^{17} cm^{-3}, n-type GaAs channel and a 50 nm thick undoped AlAs sacrificial layer grown on semiinsulating GaAs using OMCVD. The channel layer thickness is chosen such that the carrier loss due to back side depletion is compensated. The GaAs channel layer was lifted-off and bonded to a silicon substrate following the process described earlier. MESFETs were fabricated following the process described in section on FETs with recessed gates, but without the gate recess etch.

The MESFETs had I_{dss} = 260 mA/mm, $g_{m\text{-}max}$ = 41.5 mS/mm, gate-source resistance R_{GS} = 2.3 Ω-mm, and a gate-drain resistance R_{GD} = 6.7 Ω-mm. A DC transfer characteristics of the MESFET is shown in Figure 2.23 (a). A unity current gain frequency f_t = 10 GHz and a maximum frequency of oscillation f_{max} = 8.5 GHz is obtained for the same device (Figure 2.23 (b)).

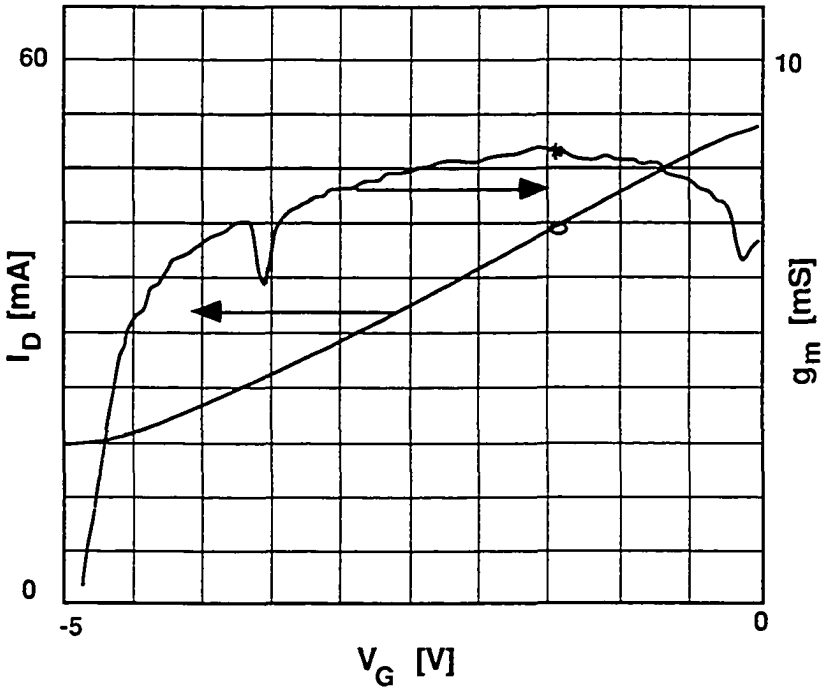


Figure 2.23(a): DC transfer characteristics of an ELO GaAs MESFET on SiO_2/Si with alloyed contacts and without recessed gate. I_{dss} = 260 mA/mm, $g_{m\text{-}max}$ = 41.5 mS/mm. Gate width W_g = 200 μm.

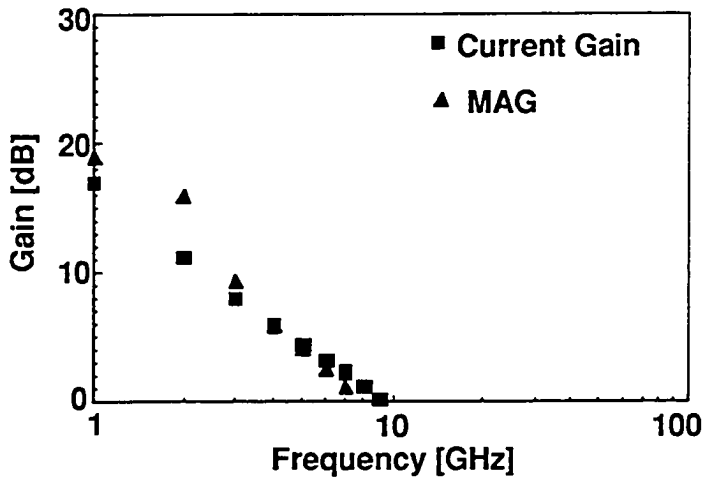


Figure 2.23(b): RF characteristics of an ELO MESFET on Si with alloyed contacts and gate without recess. L_g = 1.2 μm, f_t = 10 GHz, f_{max} = 8.5 GHz

This is consistent with the calculated value of the f_t from the measured gate-source capacitance C_{GS} = 0.7 pF/mm at V_{GS} = -3 V. The MESFET had a gate length of 1.2 μm. Higher parasitic resistances R_{GS} and R_{GD}, a consequence of direct ohmic contact to the channel layer, and gate pad parasitic capacitance are responsible for the lower value of f_{max}.

2.4.4.2 Electron Transport Study in ELO AlGaAs/GaAs Heterostructure

Hall measurements were made on ELO and on-wafer $Al_{0.3}Ga_{0.7}As$/GaAs modulation doped heterostructure to study the effect of ELO on electron transport properties. An OMCVD grown layer structure for Hall measurements consisted of a 5 nm n-GaAs, n = 3 x 10^{17} cm^{-3}, 35 nm n^+ $Al_{0.3}Ga_{0.7}As$ donor layer, 5 nm undoped $Al_{0.3}Ga_{0.7}As$ spacer and 2 μm thick undoped GaAs channel, and a 55 nm undoped AlAs sacrificial layer on semiinsulating GaAs. The n-GaAs layer on top provides a lower contact resistance compared to an ohmic contact made directly to the n^+-AlGaAs donor layer. The same material was used for the HEMTs described in next two sections.

The AlGaAs is doped n^+ and the GaAs buffer is undoped. So, at thermal equilibrium, for the Fermi level to be continuous across the heterojunction, electrons from the heavily doped, wider bandgap AlGaAs transfer to the lower bandgap, undoped GaAs. These electrons, separated from the parent donors are confined in a narrow potential well at the heterointerface due to a 0.25 eV discontinuity in their conduction bands. The electrons separated from the donors form a thin (~10 nm) sheet of charge known as a two

dimensional electron gas or 2-DEG. The electrons in a 2-DEG have mobility several times higher compared to that in uniformly doped GaAs because of the low coulomb scattering from the ionized donors. At low temperatures the only mechanism affecting electron mobility in the 2-DEG is the electron scattering by ionized donors from background doping of the GaAs buffer and other defects. In contrast, in uniformly doped GaAs the dominant reduction in electron mobility is from ever present ionized donors. We have chosen the AlGaAs/GaAs heterostructure instead of a uniformly doped GaAs because electron transport properties are more sensitive to the heterostructure film quality as compared to that of the homostructure GaAs. Also, the mechanisms affecting electron transport properties can be more easily identified as compared to that in uniformly doped GaAs.

Hall measurements were made at 290 K and 4 K on an ELO and on-wafer samples. The ELO and on-wafer samples were prepared following identical procedure and mounted side by side in a Hall measurement system on a temperature controlled sample holder. The results of transport measurements are shown in Table 2.1. As seen in the table, the measured sheet carrier concentration in the ELO sample was ~10% lower compared to that in on-wafer sample. This may be due to depletion of the 2-DEG from the back side.

Sample thickness μm	Temp. K	Carrier conc. cm^{-2}		Electron Mobility		Change in mobility %	Change in carrier conc. %
		On-wafer	ELO	On-wafer	ELO		
0.44	290	9.4×10^{11}	8.7×10^{11}	12960	10329	20.3	10.2
	4	8.95×10^{11}	8.2×10^{11}	79300	63865	19.5	9.1
1.05	290	11.7×10^{11}	10.5×10^{11}	7328	5965	18.6	7.4
	4	9.9×10^{11}	9×10^{11}	47730	40467	15.2	8.4

Table 2.1: Summary of electron transport measurements on ELO AlGaAs/GaAs

It was also observed that the mobility of the electrons in the 2-DEG is lowered by 15-20% at both 290 K and 4 K. The mobility reduction may be due to inhomogeneities in electronic bandstructure from stresses[36] of ELO film and decreased electron screening[37] effect. The changes in the mobilities and the sheet carrier concentrations are measured with respect to on-wafer samples.

2.4.4.3 Fabrication of ELO HEMTs Without Gate Recess

HEMTs have potentially higher g_m due to a large carrier concentration very close to gate electrode. It also exhibits higher f_t compared to MESFETs. So, HEMTs were investigated with the aim of making amplifier with large gain and bandwidth.

Both, ELO and on-wafer HEMTs were made following a process identical to that used for MESFETs without recessed gates. On-wafer HEMTs were made on a sample chosen from the same area of the growth wafer as that used for making ELO HEMTs. To avoid a large step from gate pad to mesa edge, mesas were not completely isolated down to the silicon dioxide buffer layer or semiinsulating GaAs substrate, respectively, for ELO or on-wafer HEMTs.

2.4.4.4 DC and RF Performance of On-wafer HEMTs Without Gate Recess

An on-wafer HEMT with gate length L_g = 1 μm and gate width W_g = 100 μm, operated in depletion mode, had a saturated drain current I_{dss} = 210 mA/mm, a

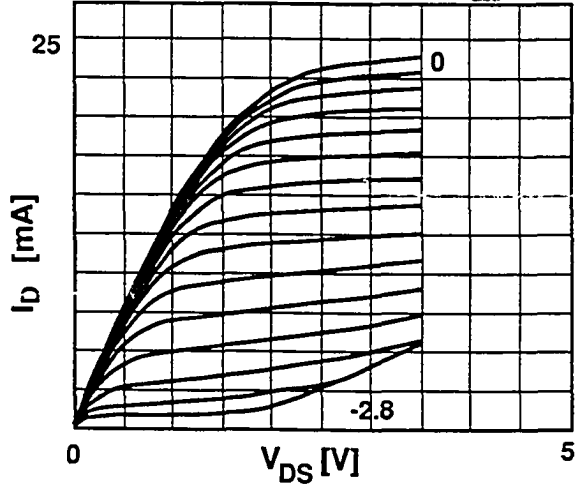


Figure 2.24(a): Drain I-V characteristics of an on-wafer HEMT with alloyed contacts and without recessed gates. Gate width W_g = 100 μm. V_G = -0.2 V/step

maximum transconductance g_m = 108 mS/mm at V_{GS} = -1.6 V, gate source resistance R_{GS} = 3.1 Ω-mm, and gate-drain resistance R_{GD} = 5 Ω-mm. A drain I-V and a DC transfer characteristics of the HEMT are shown in the Figures 2.24 (a) and (b), respectively. Contact resistance R_c = 0.35 Ω-mm and a specific contact resistance ρ_c = 1.4 x 10^{-6} Ω-cm^2 were obtained by four probe measurements on a transmission line tester fabricated on the same wafer, so most of the source resistance was from the sheet resistance of the HEMT layers.

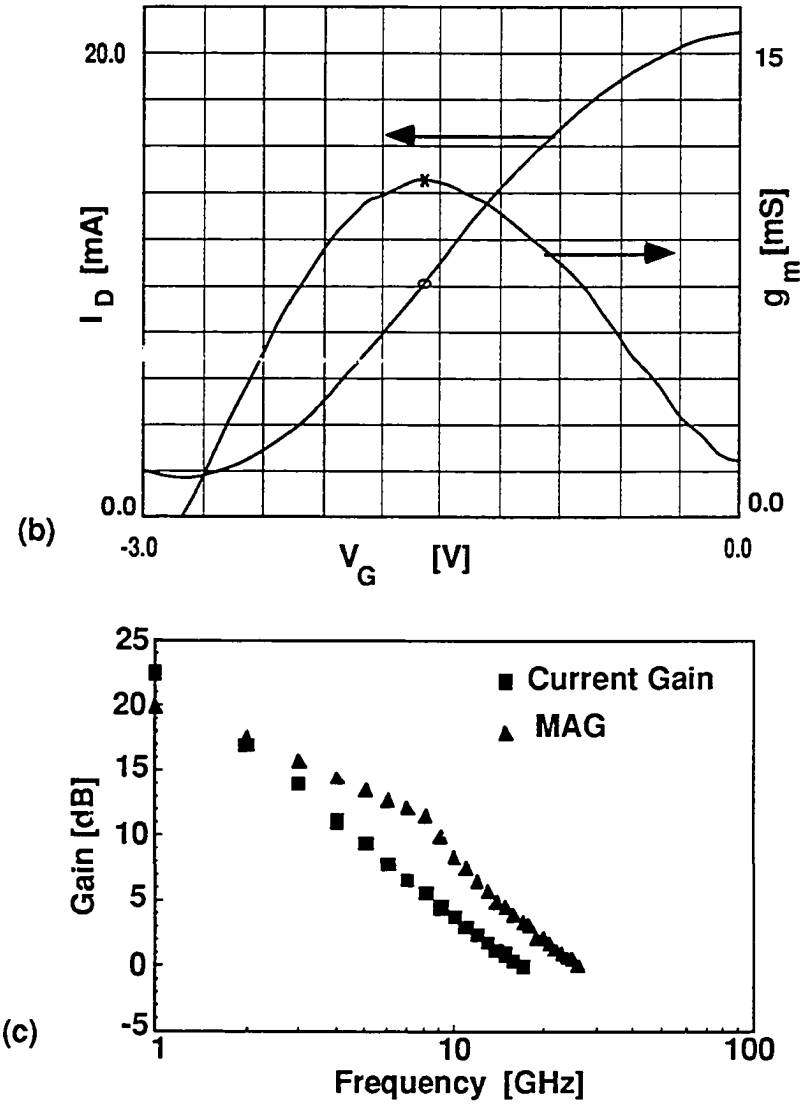


Figure 2.24 (b): DC transfer and (c) RF characteristics of an on-wafer HEMT with L_g = 1 μm, I_{dss} = 210 mA/mm, $g_{m\text{-}max}$ = 108 mS/mm f_t = 17 GHz, and f_{max} = 26 GHz

Figure 2.24 (c) shows rf current and power gains of the above mentioned HEMT. As seen in the figure, the HEMT had a unity current gain frequency f_t = 17 GHz and a maximum frequency of oscillation f_{max} = 26 GHz when operated in depletion mode with V_{GS} = -1.75 V and V_{DS} = 2 V.

2.4.4.5 DC and RF Performance of ELO HEMTs Without Gate Recess

A source-drain I-V and a transfer characteristics of a depletion mode ELO HEMT with 1.1 μm gate length and 100 μm gate width are shown in Figures 2.25(a) and (b), respectively. As shown in the Figure 2.25 (b), the HEMT had a saturated drain current I_{dss} = 200 mA/mm and a maximum transconductance g_m = 124 mS/mm at V_{GS} = -1.8 V.

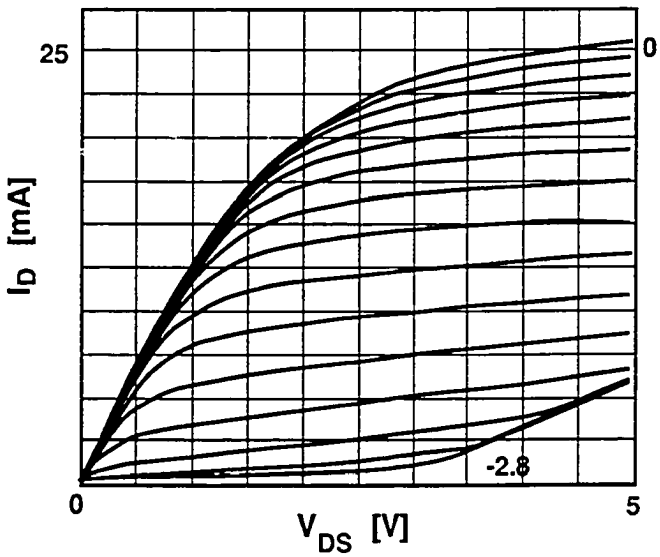


Figure 2.25 (a): Drain I-V characteristics of an ELO HEMTon SiO_2/Si

with gate width W_g = 100 μm. Scale: V_{GS}, -0.2 V/step

The measured gate source and gate drain resistances were R_{GS} = 3.1 Ω-mm and R_{GD} = 4.25 Ω-mm. Contact resistance obtained from transmission line measurements was R_c = 0.55 Ω-mm and specific contact resistivity $\rho_c = 4.1 \times 10^{-6}$ Ω-cm^2. These values are two to three times larger than those obtained with a thick n^+ GaAs layer and recessed gates.

The lower g_m value is due to a thicker spacer layer and higher source resistance. A unity current gain frequency f_t = 14 GHz and a maximum frequency of oscillation f_{max} = 12.5 GHz were obtained for the same device biased at V_{GS} = -1.75 V and V_{DS} = 2 V (Figure

2.25(c)). The lower f_t compared to the on-wafer HEMT is due to a longer gate length. The reduced f_{max} compared to the on-wafer HEMT may be from higher parasitic gate pad capacitance.

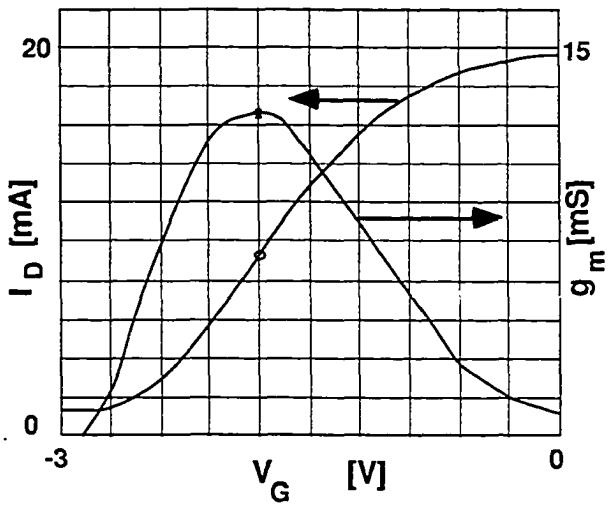


Figure 2.25 (b): DC transfer characteristics of an ELO HEMT on SiO_2/Si with I_{dss} = 200 mA/mm, $g_{m\text{-}max}$ = 124 mS/mm and V_P = -2.7 V.

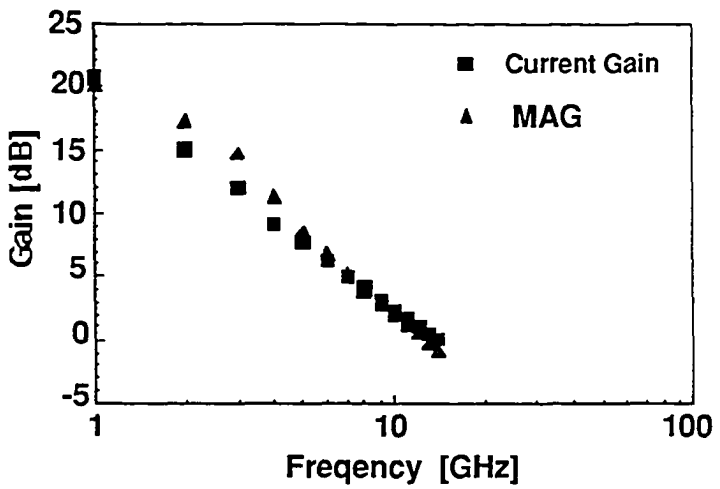


Figure 2.25 (c): RF characteristics of an ELO HEMT with gate length L_g = 1.1 μm, f_t = 14 GHz, f_{max} = 12.5 GHz

2.5 Feasibility Study of ELO GaAs FETs for Small Scale Integrated Circuit

Integrated circuit fabrication requires uniform electrical characteristics of FETs over large areas. It also requires that the FETs be stable when operated continuously over a period of long time. Assessment of the stability and the drain current and the transconductance distributions across an ELO HEMT wafer were done with this purpose. A statistical study of key device parameter distribution in on-wafer and ELO FETs is also required for validating the claim of ELO FETs being as good as on-wafer FETs. HEMTs described in the previous section were chosen for the purpose. The ELO and the on-wafer HEMTs were made on samples chosen from the same part of an OMCVD grown epitaxial material and processed following identical procedure. All the HEMTs compared had 100 μm wide and 1.5 μm long unrecessed gates with a source-drain spacing of 6.5 μm.

2.5.1 Drain Current Distribution in ELO HEMTs and On-wafer HEMTs

Drain currents in the on-wafer and the ELO HEMTs were measured with 2 V across their drain-source terminals and zero gate bias. The drain current distributions across an on-wafer and ELO HEMT samples are shown in Figures 2.26(a) and (b), respectively. The distributions are similar with mean I_{dss} = 206±12.5 mA/mm for ELO HEMT sample and I_{dss} = 189±14 mA/mm for on-wafer HEMT sample.

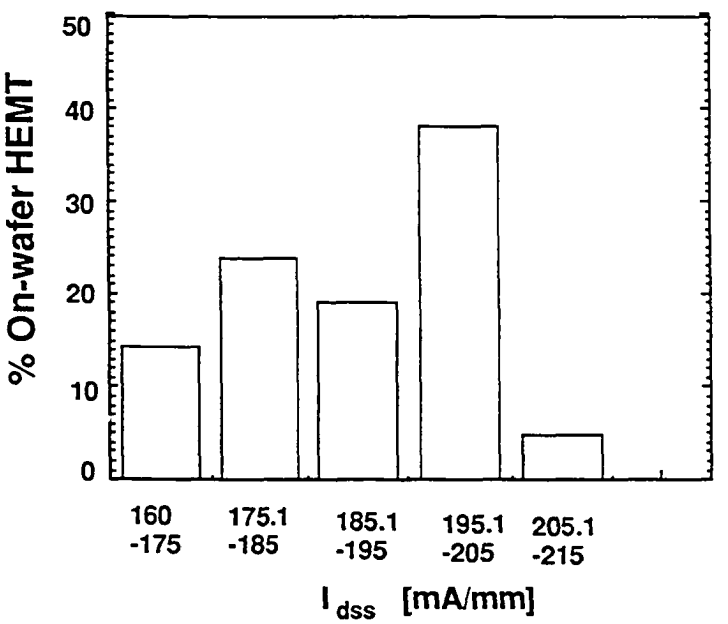


Figure 2.26(a): Saturated drain current distribution in an on-wafer HEMT sample

Total 15 ELO and 21 on-wafer HEMTs were used for this study.

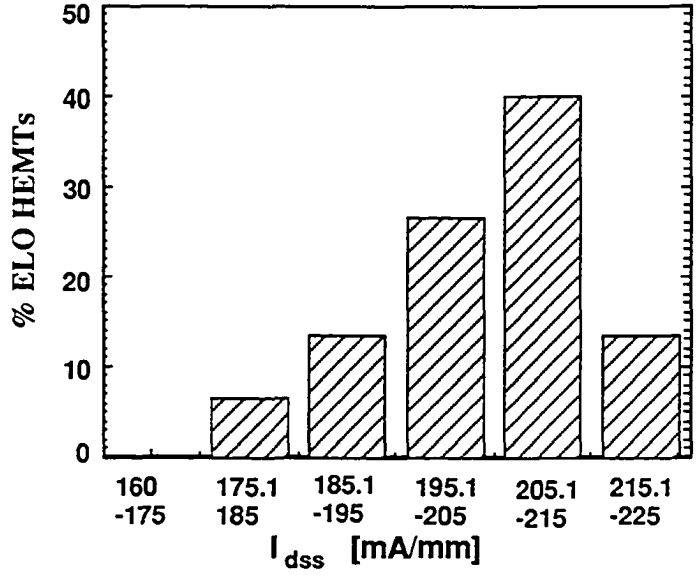


Figure 2.26 (b): Saturated drain current distribution in ELO HEMT sample

2.5.2 Intrinsic Transconductance Distribution in ELO and On-wafer HEMTs

We have chosen to study variation in a maximum intrinsic transconductance g_{mi} because it is a key FET parameter determining its high frequency performance and gain. Any degradation of carrier density because of ELO will be reflected in the transconductance g_m since it is a figure of merit directly affected by material quality. Intrinsic transconductance g_{mi} is used as opposed to the extrinsic transconductance g_{me} because it represents the true capability of the devices. Whereas extrinsic transconductance g_{me} is a process dependent parameter, very sensitive to the source resistance which in turn depends on the gate-source spacing. All the HEMTs used for this study, did not have equal gate-source spacings, hence different extrinsic transconductances.

Figures 2.27 (a) and (b) show distributions of intrinsic g_{mi} across 7 mm x 10 mm area of on-wafer and 4 mm x 8 mm area samples of ELO HEMTs, respectively. Both distributions are broad. On-wafer HEMTs had mean intrinsic transconductance of 177±21 mS/mm and the ELO HEMT had mean intrinsic transconductance of 180± 22 mS/mm. Twenty two on-wafer HEMTs and fifteen ELO HEMTs were used for this analysis. The analysis shows that there is no significant difference between the two populations. In other words, ELO HEMTs are as good as on-wafer HEMTs.

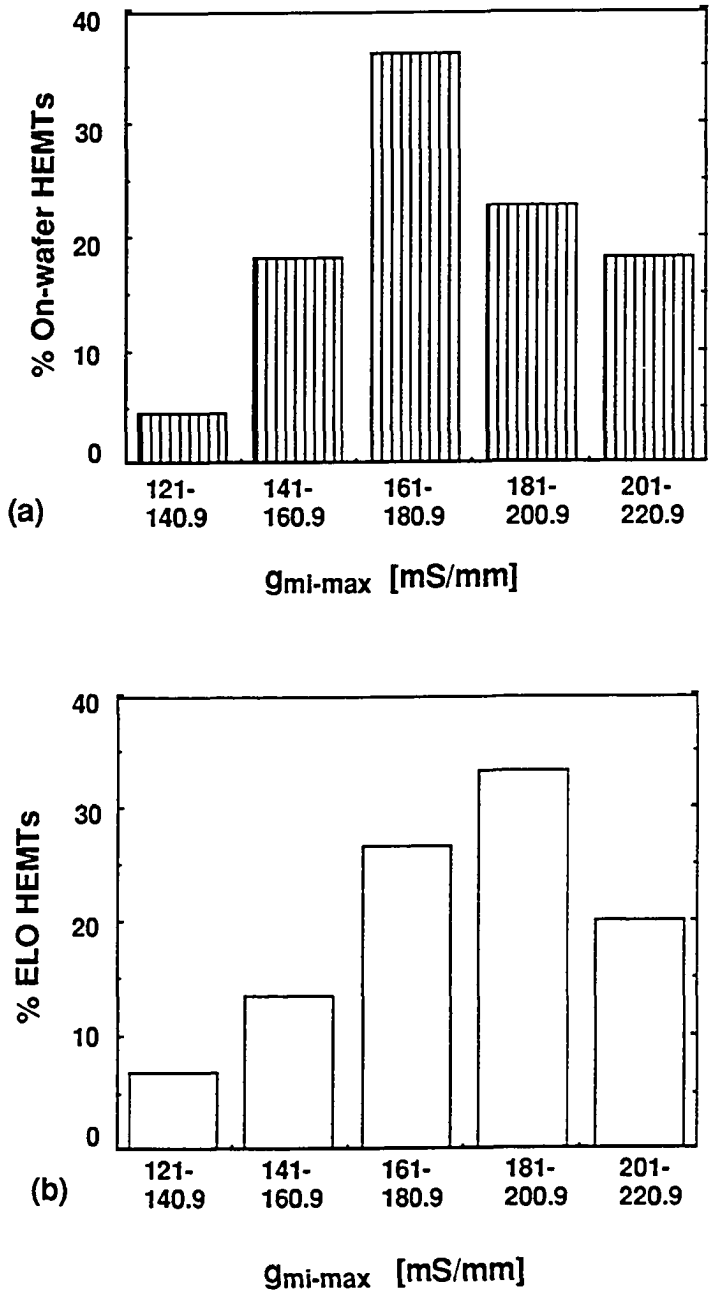


Figure 2.27: Distributions of intrinsic transconductance across (a) an on-wafer HEMT and (b) an ELO HEMT sample

2.5.3 Stability Assessment of ELO HEMTs

An ELO HEMT with 1.5 μm gate length and 100 μm gate width was operated continuously at room temperature for 115 hours with V_{DS} = 2 V, I_{DS} = 15 mA, and V_{GS} = -1 V. Figures 2.28 (a) and (b) show the DC transfer characteristics of the HEMT before and after ageing. As seen in the figure, no significant difference in the characteristics is observed. Increased gate leakage from ageing would result in increased drain current near pinch-off. A comparison of the Figures 2.28 (a) and (b) suggests that the gate leakage has not changed significantly. The pinch-off voltages before and after ageing are -2.4 V and -2.35 V, respectively. This shows that the ELO HEMTs are stable for continuous operation over short period of time. However, no predictions about device reliability can be made from these observations. Long term device reliability assessment requires accelerated test procedures such as application of temperature and bias stresses as well as variation in humidity.

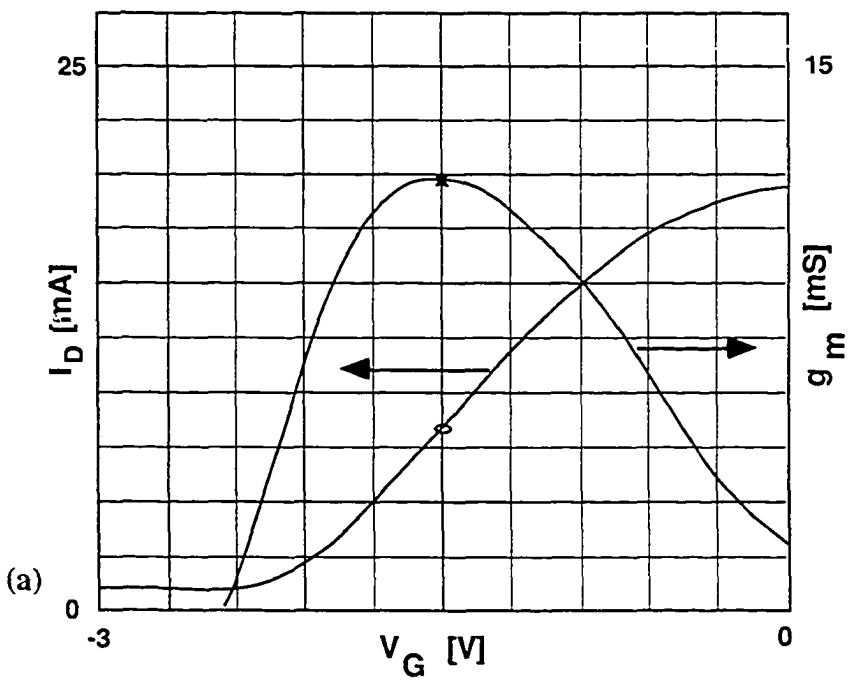


Figure 2.28 (a) : DC transfer characteristics of an ELO HEMT before 115 hour continuous operation under DC bias.

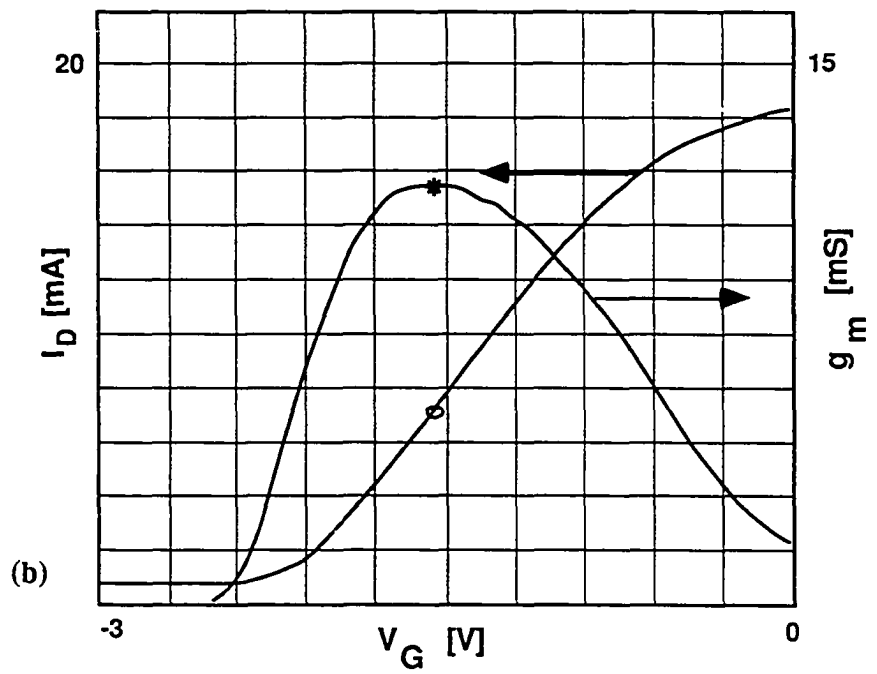


Figure 2.28 (b) : DC transfer characteristics of an ELO HEMT after 115 hour continuous operation under DC bias.

2.6 Summary

The experiments with ELO GaAs MESFET and HEMT development are summarized in the Table 2.2. As seen in the table, DC and RF characteristics of ELO and on-wafer devices are not significantly different. For the most ELO FETs, the high frequency figure of merit f_{max} is slightly lower than the f_t. It may be owing to parasitic capacitance of the gate. These results suggest that the ELO preserves electrical characteristics of FETs with substantial improvement in electrical isolation and sidegating over the on-wafer devices. Nevertheless, the problems to be solved before the strength of ELO can be fully exploited are not trivial. One of the challenges of working with the ELO material is Van der Waals bonding of the film to the new host. From my experience, Van der Waals forces alone are not always sufficient to hold the ELO film in place. As shown in section 2.4.2 some kind of external reinforcement, such as tacking the mesas down by ohmic metal before mesa isolation, is required. For making FETs on conducting substrates, choice of a low dielectric constant buffer layer with appropriate thickness is important to preserve the high frequency response. Non-uniformity in wet chemical etching of the ELO GaAs film lead to the development of FETs without recessed gates. Increased parasitic resistance and reduction in transconductance are direct consequences of it.

To summarize: in spite of its shortcomings, ELO presents a potential alternative to the hybrid integration of GaAs FETs on insulating substrates for microwave applications.

FET Type	Substrate	Operating Mode	Comment	Gate Length, μm	$g_{me\text{-}max}$, mS/mm	$g_{mi\text{-}max}$, mS/mm	f_t, GHz	f_{max}, GHz
MESFET	On GaAs wafer	Depletion	Alloyed AuGe contacts Recessed gate	1.1	75	90	13	16
	ELO on 1.3 μm SiO_2/Si	Depletion	Alloyed AuGe contacts Recessed gate	1.3	135	-	12	14
	ELO on 0.25 μm SiN/Si	Depletion	Alloyed AuGe contacts Recessed gate	0.1	75	-	34	23
	ELO on sapphire	Enhancement	Alloyed AuGe contacts Recessed gate	1.1	100	-	8.5	17
	ELO on 1.3 μm SiO_2/Si	Enhancement	Nonalloyed contacts Recessed gate	1.0	201	225.9	12.5	7.5
	ELO on 1.3 μm SiO_2/Si	Depletion	Alloyed AuGe contacts No gate recess	1.2	41.5	45.9	10	8.5
HEMT	On GaAs wafer	Depletion	Alloyed AuGe contacts No gate recess	1.1	108	161.8	17	26
	ELO on 1.3 μm SiO_2/Si	Depletion	Alloyed AuGe contacts No gate recess	1.1 - 1.2	124	201	14	12.5

Table 2.2: Summary of ELO FET experiments

CHAPTER 3

Langmuir-Blodgett Thin Films For Optoelectronic Device Applications

3.1 Introduction

Thin films of cadmium and zinc salts of arachidic acid have been deposited using the Langmuir-Blodgett (LB) technique. The study of diffusion behavior of cadmium and zinc from this novel source in $In_{0.53}Ga_{0.47}As$/InP is a subject of this chapter. Highly doped (N_A = 2-4 x 10^{19} cm^{-3}) shallow (x_j ~0.1 to 0.4 μm), p^+-n junctions are obtained. PIN photodetectors and Junction Field Effect Transistors (JFETs) are fabricated as demonstration of the usefulness of the new technique. The JFET had a saturated drain current I_{dss} = 50 mA/mm, and transconductance $g_{m\text{-}max}$ = 80 mS/mm. The 40 μm diameter PIN photodetector with a 2.3 μm thick absorbing layer had internal quantum efficiency η_i = 84 %, responsivity R = 0.88 A/W, and bandwidth B = 2 GHz.

Section one is a general introduction to the properties of InGaAs/InP. Historical background of LB films is described in section two. Section three is a review of shallow p^+-n junction fabrication techniques in InGaAs/InP. LB film deposition system, characterization techniques, and its application to Cd and Zn diffusion are described in section four. LB film application to JFETs and PIN photodetectors are described in section five. Results are summarized in section six.

The development of a new diffusion source using LB films has benefited by the expertise of Dr. Nick Schlotter in characterizing LB films as well as diagnosing problems with the LB deposition. Thanks are also due to Dr. C. C. Chang for Auger Electron Spectroscopy (AES) on LB films and Dr. Steve Schwarz for Secondary Ion Mass Spectrometery (SIMS) profiling of Cd and Zn diffused InGaAs/InP layers. Dr. Raj Bhat provided InGaAs/InP for Cd and Zn diffusion study as well as for PIN photodetector and JFET fabrication.

$In_{0.53}Ga_{0.47}As$ (referred to as InGaAs) lattice matched to InP has a high low-field electron mobility and a high electron saturation velocity as well as a large separation between Γ and L valleys of the conduction band. Moreover, its absorption coefficient is high in the 1.3-1.55 μm wavelength range, which coincides with the lowest loss in the silica optical fibers used for lightwave communications. These properties make InGaAs desirable material for

high speed FETs and photodetectors, hence, optoelectronic integrated circuits (OEIC) for optical communication. PIN photodetectors fabricated in InGaAs/InP have been in use for a long time and its technology is quite mature.[38-39] Because of its narrow ~0.75 eV bandgap, low leakage current Schottky barriers, useful for efficient drain current modulation, are difficult to form. HEMTs in InAlAs/InGaAs/InP with excellent DC and high frequency performance have been fabricated, but their integration with InGaAs/InP PIN photodetectors is difficult due to differences in their processing. JFETs are potential candidates for integration with PIN photodetectors for OEICs because of similarities of their fabrication processes. This will become clear toward the end of this chapter where fabrication processes of both of them are described. For high performance n-channel JFETs, highly doped p^+, shallow and short (≤ 1 μm) gates are a must. Shallow p^+-n junctions are also required for high speed PIN photodetectors. Cadmium or zinc diffusion from a LB film can meet the challenge of highly doped, shallow p^+-n junction formation.

3.2 Historical Background of LB Films

Deposition of thin, organic films from a water based trough is well known. Historical references of spreading oil on rough sea for its calming effect dates back to Aristotle. In modern times, Benjamin Franklin was the first one to show that when a small amount of oil is spread over a large area of water, a continuous film of few nanometer thickness is formed at the surface. However, credit for making systematic study of monolayers of amphiphilic compounds at the air-water interface of a trough belongs to Irving Langmuir.[40] The first paper on multilayer deposition of carboxylic acid on a solid substrate from an air-water interface was published by Langmuir's colleague Katherine Blodgett.[41] Therefore, the deposition technique is referred to as a Langmuir-Blodgett film deposition method. The simple LB trough has evolved into a sophisticated, computer controlled deposition system over a period of several decades. LB films also have come long way from being of purely academic interest to the modern electronic and optoelectronic device applications. Electronic devices incorporating LB film as their integral part include solar cells,[42] memories,[43] MISS switches,[44] field-effect transistors,[45] MISIM photodetectors,[46] MISFETs[47] and HEMTs.[48] These applications deal with only one aspect of the LB films, namely, its insulating nature. As-deposited or oxygen plasma (referred to as oxyplasma) treated LB films are employed in all of the above device applications. The oxyplasma treatment of the LB films results in the decomposition of the fatty acid salt into a metallic oxide, hydroxide or carbonate.[46-47-48] This is discussed in detail in the section on LB film

characterization. The devices incorporating as-deposited LB films have been observed to degrade with the passage of time owing to degradation of the organic part of the LB film. However, the devices with oxyplasma treated LB films are expected to be more stable because of the removal of most of the hydrocarbons during device processing. It may be possible to use metal ions as a dopant source in semiconductor after hydrocarbon removal[46-49] from the LB deposited fatty acid salts. This hypothesis has been investigated in detail in this chapter.

3.3 Cadmium and Zinc Diffusion from Conventional Sources

Cadmium and zinc incorporation in InGaAs/InP from conventional sources such as doped spin-on glass, ion implantation and solid state diffusion is reviewed briefly in this section to put the work on proposed novel source in proper perspective.

Various methods of acceptor incorporation for shallow junction fabrication in III-V compound semiconductors have been used, such as diffusion from a solid impurity source in a closed ampoule[50] ion-implantation[51] diffusion from doped, spun-on SiO_2[52] and ZrO_2[53] films, and diffusion from an electroplated and re-evaporated layer of zinc on GaAs.[54] Each of these techniques have problems associated with them. It is hard to scale-up the closed ampoule diffusion for large samples and accurate control of total dopant dose as well as junction depth is difficult. Co-implantation[51] of phosphorus and beryllium in InP done at 100 and 20 KeV, respectively, gives a fairly shallow junction but radiation damage to the crystal lattice from such high energies may not be completely removed without substantial diffusion of the dopant. When Si_3N_4 is used as a protective cap for diffusion, zinc from a spin-on source sometimes reacts with the cap at the diffusion temperature and forms a compound which is difficult to remove.[52]

A new source for controlled acceptor diffusion from LB deposited films of cadmium (or zinc) arachidate (Cd(Zn)-Ar), the cadmium(zinc) salt of arachidic acid [$H_3C(CH_2)_{18}$ COOH] described in the next section avoids the problems associated with the other sources. This new source offers the following advantages over the conventional sources.

1. The LB film can be easily patterned by lift-off for selective area diffusion.

2. The total acceptor dose is determined by the number of LB film monolayers, each of which has a fixed density of Cd(Zn) atoms (2×10^{14} cm^{-2}); even lower densities may be obtained by diluting the Cd(Zn) in the LB film.

3. This simple, room temperature technique presents a safer method of handling potentially toxic materials such as Cd.

4. It can also be used as a dopant source of any other material capable of forming a fatty acid salt at the air-water interface of the trough.

5. Unlike closed ampoule diffusion, the size of the substrate is not limited by ampoule volume. Virtually, any size substrate can be used with appropriate trough depth and surface area.

3.4 Cadmium and Zinc Diffusion in InGaAs/InP from LB Film

Deposition of LB film monolayers containing Cd and Zn is described in this section along with their characterization techniques.

3.4.1 LB Film Deposition System and Technique

Monolayer and multilayer deposition of fatty acids and salts of fatty acids using an LB trough is well developed.[55-56] The LB deposition system used in this work is based on a Joyce-Loebl computer controlled trough with a constant temperature bath. Top and cross sectional views of the LB trough are shown in Figures 3.1. Approximate dimensions of the trough are 50 cm x 20 cm. The trough is ~8 cm deep where the sample is dipped and ~3 cm deep everywhere else. As shown in the Figure 3.1 the trough is surrounded by a movable barrier of Teflon tape and kept on an air cushioned table for isolating it from vibrations. The deposition system is housed in a dust free chamber with filtered air supply under slightly positive air pressure. The trough is filled with a buffered aqueous sub-phase of 2.5×10^{-4} M $CdCl_2$ ($ZnCl_2$) and 1×10^{-4} M $NaHCO_3$. The pH of the buffer solution must be maintained constant, slightly acidic, because Cd and Zn ions precipitate out of the solution under basic pH (>7) conditions. The choice of $CdCl_2$ or $ZnCl_2$ depends on the

required dopant. Fifty microliters of 1.45 x 10^{-2} M arachidic acid in chloroform is spread over the trough forming a monolayer of the arachidic acid upon evaporation of the chloroform. The H^+ ion in the carboxylic acid group (-COOH) of arachidic acid (Figure 3.2(a)) is displaced by Cd^{+2} (Zn^{+2}) ion from the sub-phase to form Cd(Zn)-Ar, a complex consisting of cadmium(zinc) and two fatty acid molecules at the air-water interface (Figure 3.2(b)).

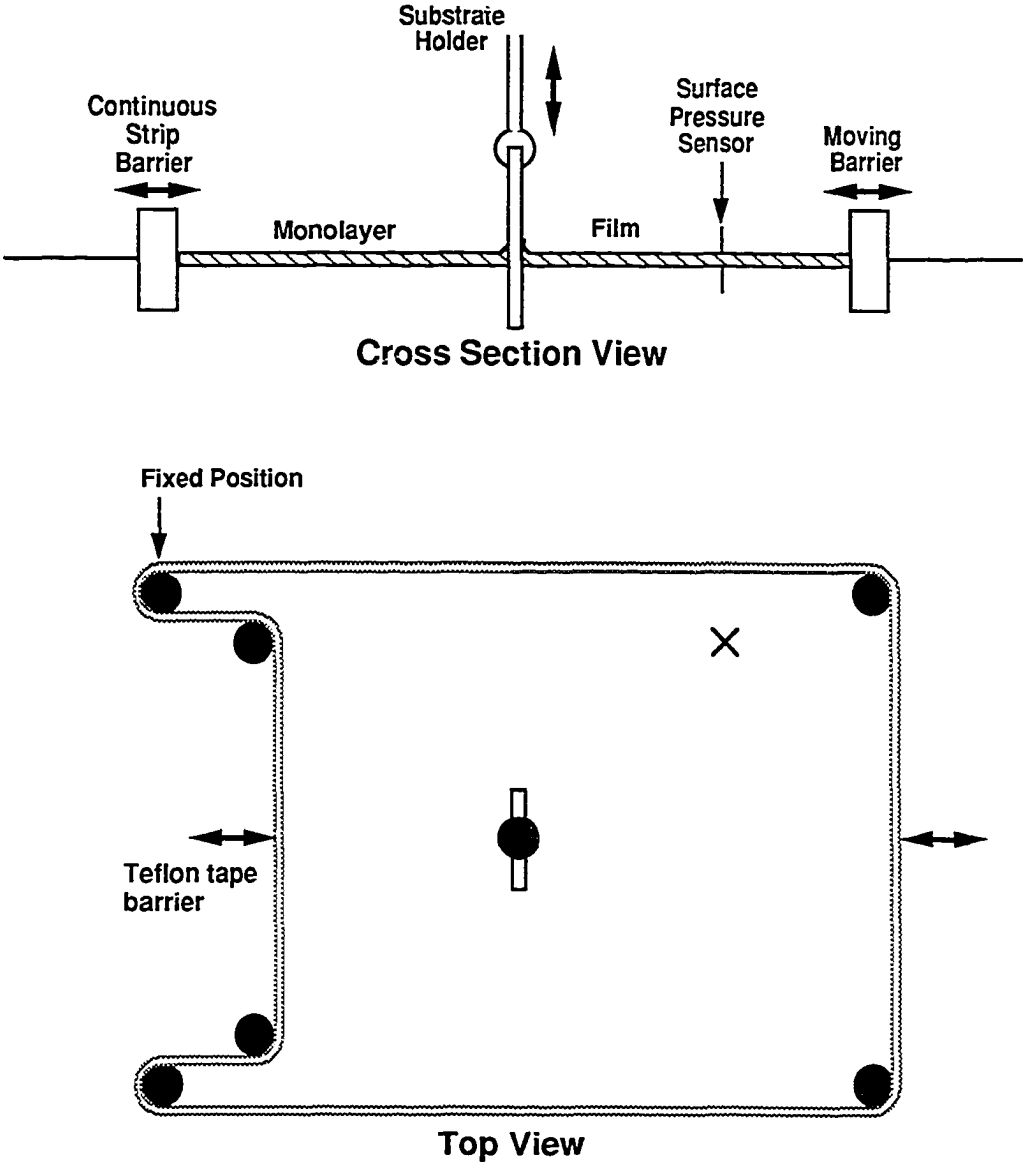
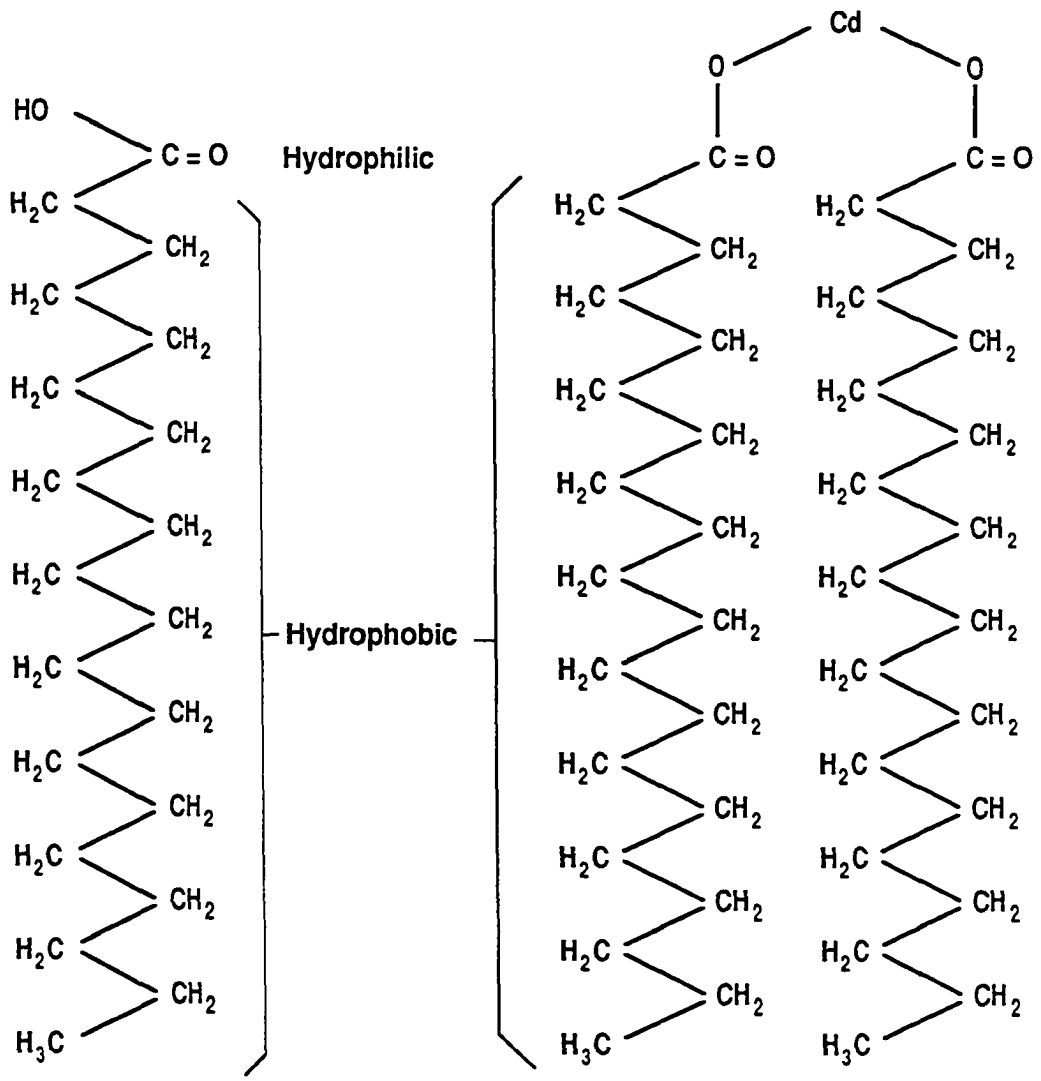


Figure 3.1: (a) Top view and (b) cross sectional view of the LB trough

Deposition of LB film onto a hydrophilic semiconductor substrate, held vertically to the film surface, is accomplished by slowly lowering in and raising it out of the trough at a constant speed with a computer controlled arm, pausing for 10 seconds at the end of each pass to allow water trapped in the deposited Cd(Zn)-Ar film to drain and to let the surface monolayer of the LB film relax and attain equilibrium. A monolayer of Cd(Zn)-Ar is transferred from the trough surface to the substrate with each pass in or out of the trough (Figure3.3(a),(b)).



(A) Arachidic Acid, $CH_3(CH_2)_{18}COOH$ **(B) Cadmium Arachidate**

Figure 3.2: (a) A molecule of arachidic acid at air-water interface just before the acidic(-COOH) group reacts with Cd^+ ions from buffer. (b) Cadmium arachidate at the air-water interface of the LB trough

For a continuous, uniform, domain-free film, the surface pressure, monitored by a Wilhelmy plate and a micro-force balance, must be held constant during the entire deposition process. This is accomplished by displacing the movable Teflon barrier surrounding the surface monolayer of Cd(Zn)-Ar to compensate for the molecules transferred to the substrate. Typical parameters for a LB deposition experiment are: surface pressure of 30 mN/m, barrier compression rate of 2 cm^2 /min, buffer pH of 6-6.6, substrate dipping rate of 8 mm/min and buffer temperature of 18°C. The result of the LB deposition is a continuous Cd(Zn)-Ar film whose thickness can be precisely controlled by the number of layers deposited.

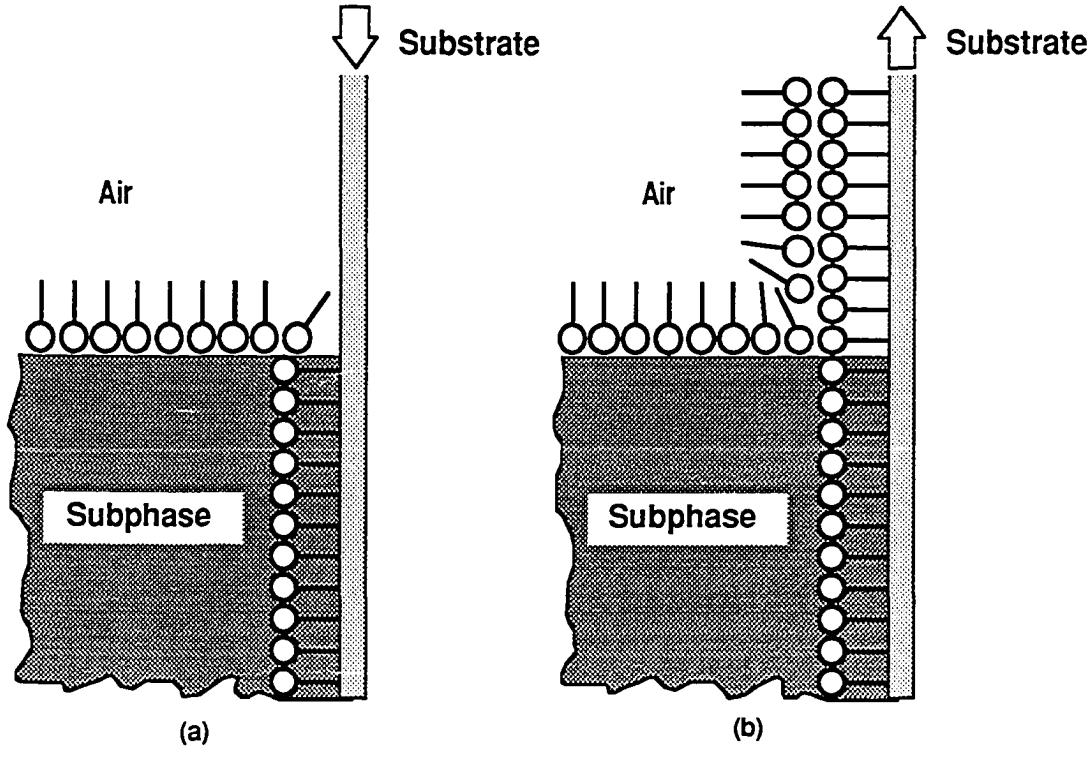


Figure 3.3: LB film deposition on a hydrophillic substrate. One monolayer of LB film is transferred to the substrate with each pass in (a) and out (b) of the trough

3.4.2 Diffusion Procedure

Eight monolayers of Cd(Zn)-Ar were deposited on 0.5 μm thick $In_{0.53}Ga_{0.47}As$ with two different background dopings n = 3 x 10^{14} cm^{-3} and n = 6 x 10^{16} cm^{-3} grown by organo-metallic chemical vapor deposition (OMCVD) on semi-insulating InP substrates. After the deposition, the organic part of the film was removed by an oxyplasma treatment. Auger analysis indicated[57] that approximately one LB monolayer worth of Cd-Ar is lost during this processing, so the resulting surface concentration of Cd(Zn) is 1.4 x 10^{15} cm^{-2}. Both sides of the substrate were then capped with 80 nm of either SiO_2 or Si_3N_4, deposited by plasma enhanced chemical vapor deposition (PECVD); unless otherwise stated, the cap was SiO_2. Cadmium diffusion was done under flowing argon on a graphite plate heated by quartz lamps for various time periods (2 to 40 minutes) and temperatures (550 to 625°C). The temperature of the graphite plate can be ramped up or down rapidly, facilitating tighter control of junction depth as opposed to conventional furnaces requiring ramp up/down time of the order of diffusion times, in case of a short diffusion. Zinc was diffused at 600°C for 4 to 16 minutes. Zinc diffusion could be done at as low as 450°C. No surface degradation of the substrates from the diffusion was observed under an optical microscope.

3.4.2.1 Patterned Diffusion Without a Mask

Stresses at the diffusion mask edge is a major problem in patterned diffusion from the conventional sources, causing a sharp curvature in the junction which lowers the junction breakdown voltage. The biggest strength of the LB film diffusion source is in its capability of patterned diffusion without using a diffusion mask. A mask-less patterned diffusion procedure is shown in Figure 3.4.

Because the diffused regions cannot be distinguished from the regions with no diffusion, the first two steps are used to put down alignment marks for later processing steps. A thin (~100 nm) layer of Si_3N_4 is deposited on substrate using PECVD. Next, the Si_3 N_4 is removed from every where except near the edges (Figure 3.4(b)). A desirable pattern is now defined on the substrate and in Si_3N_4 using photoresist (Figure 3.4(c)). The pattern in the Si_3N_4 serves as alignment mark for future processing. The LB film is deposited next and treated with oxyplasma. The photoresist is now dissolved with acetone, leaving a patterned film of Cd or Zn on the substrate. Next, the substrate is capped with protective silicon dioxide on both sides and diffused at high temperature. Since, no mask is present during high temperature diffusion there are no stresses from the mask at high temperature

due to large difference in the thermal expansion coefficients of the mask and the semiconductor.

The mask-less diffusion procedure described above requires one extra mask level. Since we used an existing mask set for our preliminary experiments, we could not do the mask-less diffusion process described above and had to use a silicon nitride mask for patterned diffusion which resulted in lower junction breakdown voltage. This will be seen in the section on JFET and PIN photodetector fabrication using LB film.

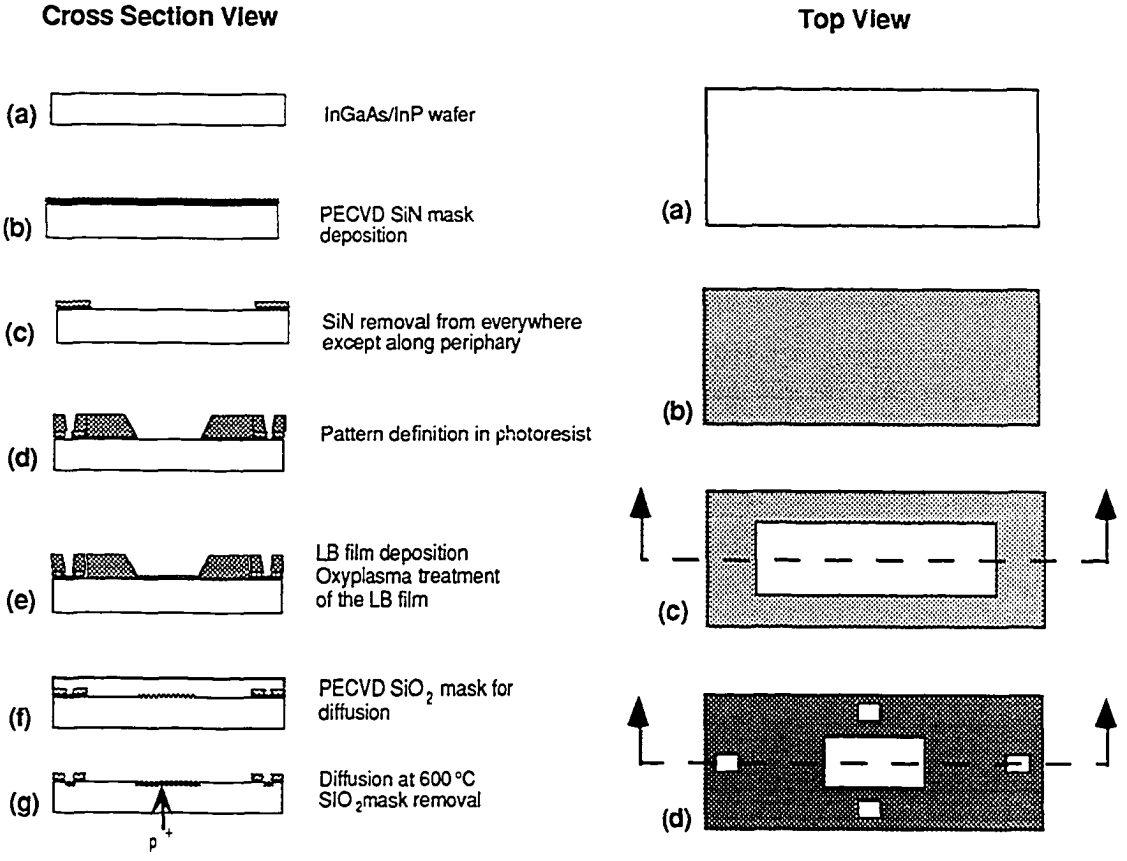


Figure 3.4 : Patterned diffusion scheme without a mask using LB film diffusion source

3.4.3 Characterization of As-deposited and Oxyplasma Treated LB Films

During the above-mentioned processing sequence, the LB film deposited substrates were characterized at various stages using Grazing Incidence Infrared (GIIR) spectroscopy and Auger Electron Spectroscopy (AES).

GIIR spectroscopy was performed to determine whether the LB film was deposited as free acid (arachidic acid) or as a fatty acid salt Cd-Ar. The grazing angle permits the measurement of the absorbance spectrum for a polarization normal to the substrate. The spectra were taken with a BOMEM DA-3 FTIR (Fourier Transform Infrared) spectrometer using a mercury cadmium telluride detector. The LB films for GIIR studies were prepared by LB deposition on gold surfaces. The metal surfaces were prepared by evaporating 5 nm of titanium or nickel followed by 150 nm of gold on a glass microscope slide. The GIIR spectrum of 10 monolayers of Cd-Ar is shown in Figure 3.5(b). The cadmium carboxylate structure has symmetric and anti-symmetric modes that are observed in the GIIR spectrum at 1432 cm^{-1} and 1542 cm^{-1}, respectively.[58] A GIIR spectrum of a bulk sample of arachidic acid taken from Ref.[58] is shown in Figure 3.5(a). The doublet at 1695 cm^{-1} and 1705 cm^{-1} in the spectrum of bulk arachidic acid is associated with the acidic head group -COOH. The absence of this doublet and the presence of strong metal carboxylate peaks at 1432 cm^{-1} and 1542 cm^{-1} in the spectrum of the as-deposited film indicate that the film is primarily the cadmium salt with negligible free acid content.

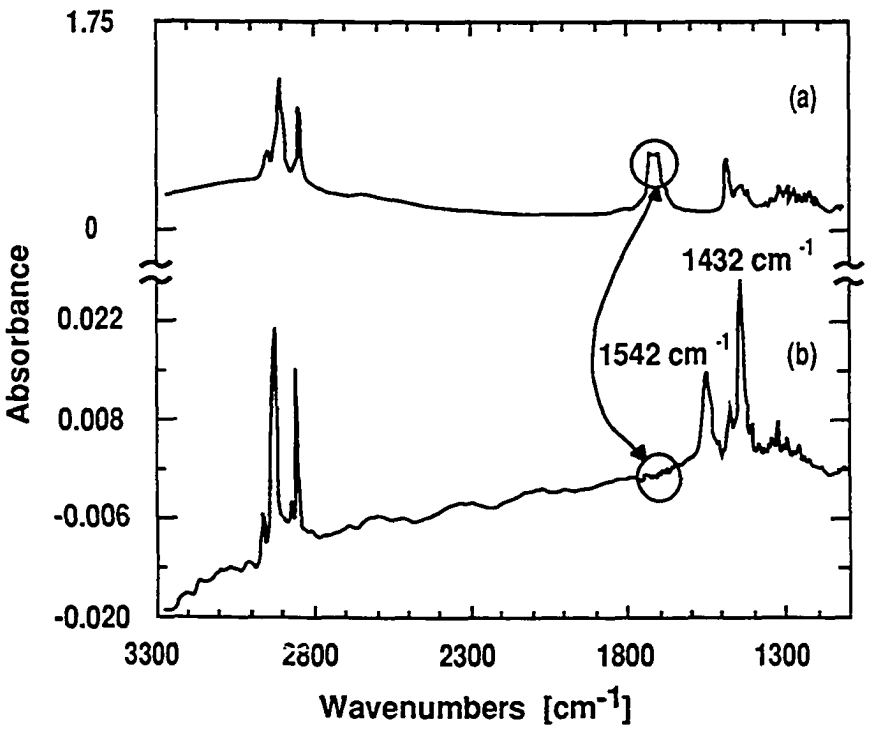


Figure 3.5: (a) A GIIR of bulk arachidic acid in KBr pallet. Notice the doublet at 1695 cm^{-1} and 1705 cm^{-1} (circled) indicating the presence of acidic group (-COOH). (b) A GIIR of as-deposited Cd-Ar on glass. The absence of doublet indicates that the LB film contains fatty acid salt (Cd-Ar) and negligible free acid.

GIIR also gives us information about the orientation of the Cd-Ar molecules with respect to the substrate. The spectrum obtained has the electric field component of the IR radiation

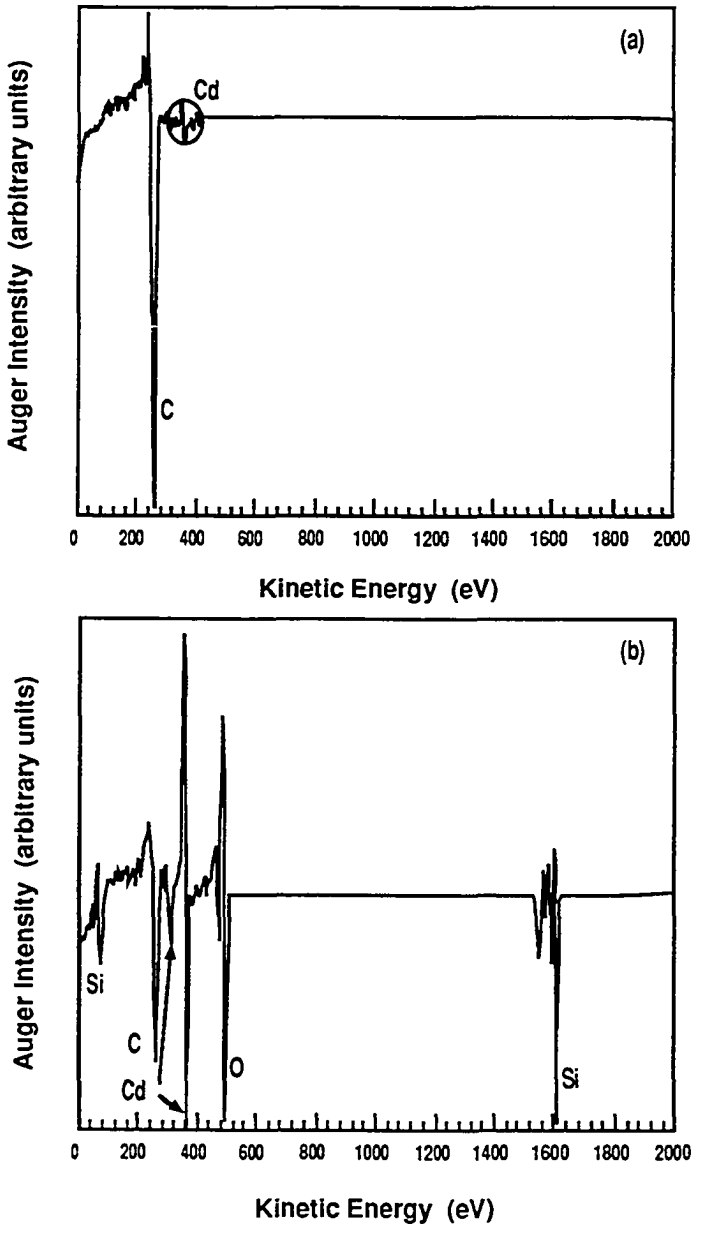


Figure 3.6: (a) Auger spectrum of as-deposited Cd-Ar on Si showing a low concentration of cadmium as compared to carbon. (b) Auger spectrum of oxyplasma processed LB film showing much larger intensity of cadmium peak as compared to carbon, plotted on a more sensitive scale.

perpendicular to the substrate surface; the stronger intensity of the 1432 cm^{-1} relative to the 1542 cm^{-1} peak indicates that the molecules are oriented approximately perpendicular to the substrate.[58]

AES showed that the oxyplasma treatment reduces the amount of hydrocarbons to a low level while leaving most of the Cd in the film.
The Auger spectra of as-deposited and oxyplasma processed Cd-Ar on Si are shown in Figure 3.6 (a) and (b), respectively. It should be noted that the Auger spectrum of the oxyplasma processed LB film is plotted at a higher sensitivity. In these spectra, the peaks at 320 and 380 eV are associated with Cd. Metallic cadmium however, exhibits[59] distinct Auger peaks at 321, 367, 376 and 382 eV. The shift to lower energies by 1-2 eV in the spectra of the as-deposited and oxyplasma treated LB films indicates the presence of cadmium in the form of compounds such as cadmium oxide, hydroxide or carbonate. A more detailed study is required to identify the compounds unambiguously. In the spectra of as-deposited and oxyplasma treated films, the peak at 273 eV is associated with carbon.

Auger spectra of as-deposited and oxyplasma treated monolayers of Zn-Ar on silicon substrate are shown in Figures 3.7(a) and 3.7(b), respectively. Peaks between 835 and 1040 eV are associated with zinc in the spectra of as-deposited as well as oxyplasma treated films. These peaks are shifted[58] to lower energies by 1-2 eV, from those of pure metallic Zn, similar to the Cd case, indicating presence of Zn in form of compounds such as zinc oxide, hydroxide, carbonate or some combination of these.

A comparison of the relative intensities of the zinc, cadmium and carbon in the spectra of as-deposited and oxyplasma processed LB films clearly demonstrate that the oxyplasma treatment significantly lowers the hydrocarbon content in the LB films. The intensity of the Cd peaks is consistent with a surface concentration of 1.4×10^{15} cm^{-2}.

3.4.4 Characterization of Cadmium and Zinc Diffused InGaAs Layers

Cadmium-diffused samples were profiled using SIMS and differential Hall techniques. In the differential Hall technique a conventional Hall measurement was performed on the sample with a Van der Pauw geometry after repeatedly etching a thin layer (~10 nm) of material using either a selective chemical etchant (1 H_3PO_4 :1 H_2O_2 : 38 H_2O, etch rate ~2 nm/sec) or anodizing etch (0.1 M KOH in deionized H_2O, etch depth ~2.5 nm/volt). The

sheet carrier density from the Hall measurements was numerically differentiated to obtain the carrier concentration profile. Differential Hall profiles of the samples diffused at 600°C

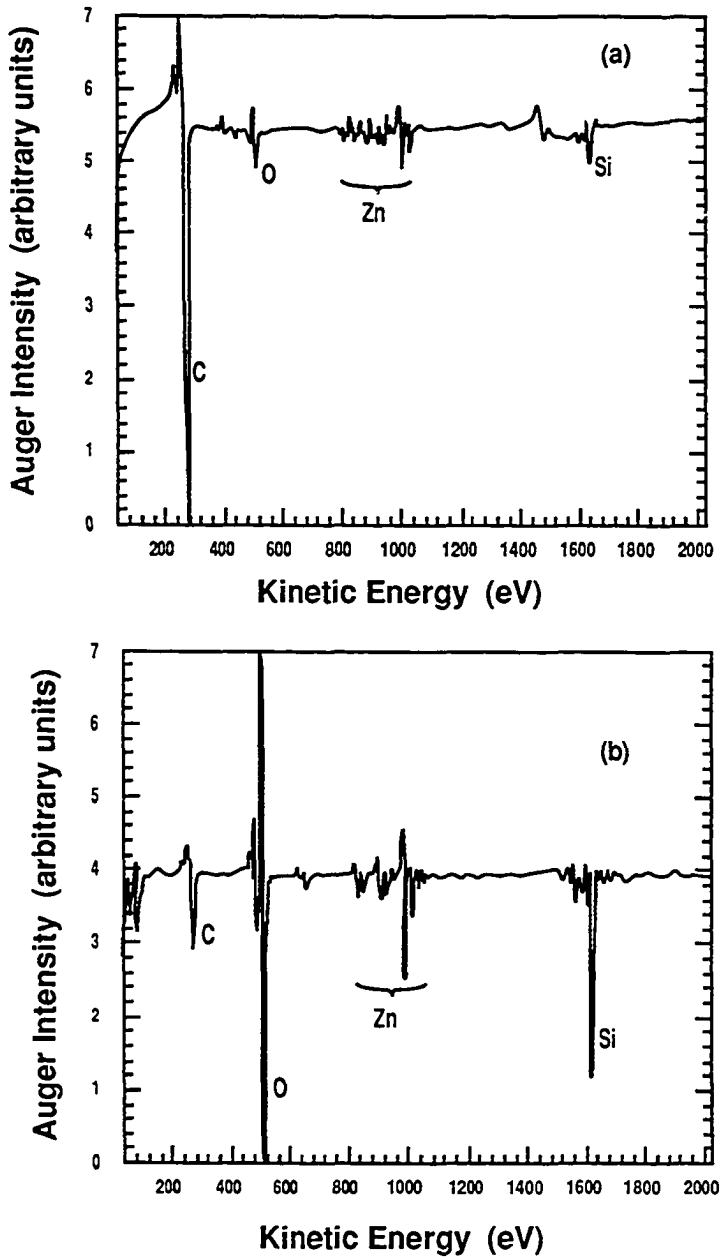


Figure 3.7: (a) Auger spectrum of as deposited Zn-Ar on Si. The smaller peak of Zn compared to C indicates that Zn content is lower compared to C. (b) Auger spectrum of oxyplasma treated Zn-Ar, plotted on a more sensitive scale. Higher intensity of Zn peak indicates that oxyplasma removes the C in the Zn-Ar LB film.

for 10, 20 and 40 minutes are shown in Figure 3.8. The dependence of the junction depth x_j on the diffusion time yields a diffusion coefficient of 1-2 x 10^{-13} cm^2 sec^{-1} at 600°C, in agreement with that reported (2 x 10^{-13} cm^2 sec^{-1}) by Aytac, et. al.[47]

With the SiO_2 cap, about 10-20% of the total cadmium dose could be incorporated into the InGaAs and the peak carrier concentration of 2 x 10^{19} cm^{-3} occurred at about 50-100 nm beneath the surface. On the other hand, in samples capped with Si_3N_4 the total sheet carrier concentration was two to three times larger and the peak acceptor concentration occurred at the surface. We believe that these differences are due to the stresses of the cap. PECVD Si_3N_4 and SiO_2 are known to be under tension[60] and compression, respectively.

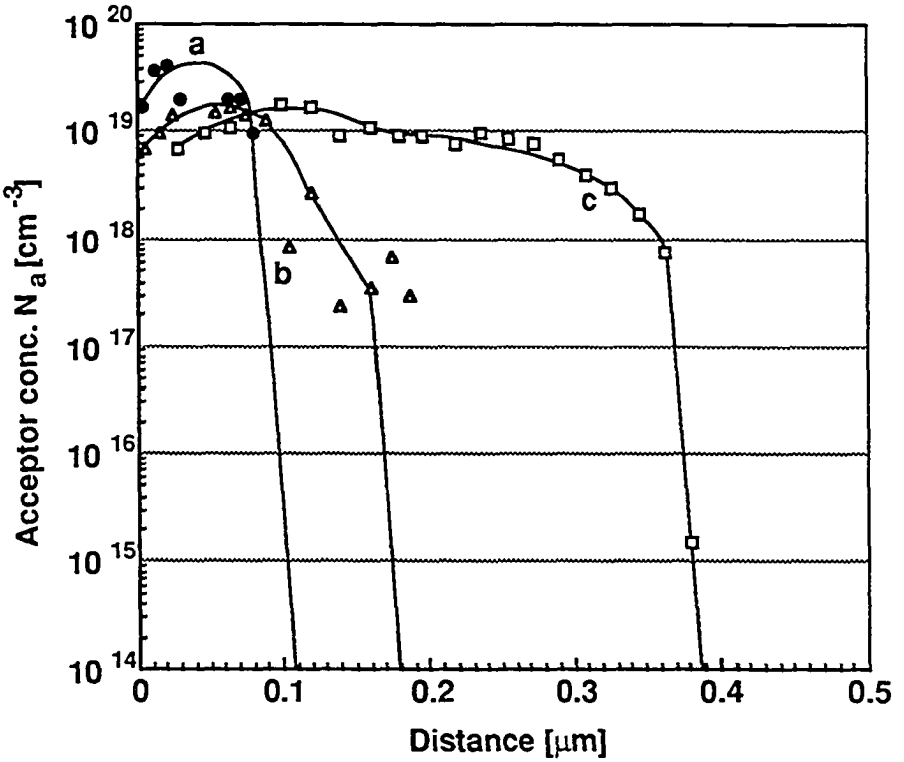


Figure 3.8:Differential Hall profiles of Cd diffused InGaAs/InP. Diffusion temperature; 600°C, Cd source; 1.4 x 10^{15} cm^{-2}, Time (a) 10 (b) 20 and (c) 40 minutes

For a low cadmium source of 2 x 10^{14} cm^{-2} and a long (20 minutes, 600°C) diffusion time, the peak acceptor concentration is reduced to 50% of that obtained with a 12 minute diffusion and a long tail develops in the carrier profile (Figure 3.9). This is due to

redistribution of acceptor Cd after the diffusion source is exhausted. A comparison of integrated dopant densities of the two indicates that Cd incorporation after 20 minute diffusion is more than that after 12 minute diffusion.

Figure 3.10 shows SIMS profiles of Cd diffused InGaAs/InP for various temperatures and times with a constant Cd source of 1.4 x 10^{15} cm^{-2}. The SIMS depth profiles of Cd were obtained in an Atomika 3000-30 ion microprobe using 6 KeV Cs^+ ion bombardment with 0.17 μm thick silicon dioxide cap on each sample. Sputtered composite ions of $CsCd^+$ were monitored. A Cd implant into an InGaAs/InP superlattice (40 nm InGaAs/ 10 nm InP x 20 periods) was employed as a standard such that the indicated concentration scale in the figure is accurate within a factor of two. The $CsCd^+$ signal was normalized to the Ga^+ signal measured simultaneously to account for variations in beam current. An equivalent background of 1.5 x 10^{18} cm^{-3} was then subtracted from each profile to account for instrumental background. The profiles therefore do not extend below 10^{18} cm^{-3} in the figure. Since the profiles were normalized to Ga, they are meaningless within the oxide and are not shown in this region. As each profile was treated in precisely equivalent fashion, the indicated trends are expected to be reliable.

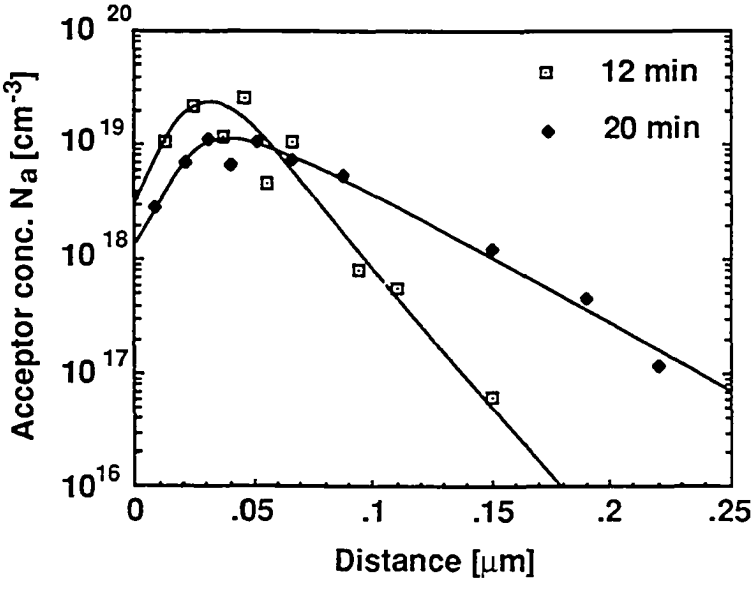


Figure 3.9: Differential Hall profiles of Cd diffused InGaAs showing the effect of dopant dose depletion. Diffusion temperature: 600°C, Cd source: 2 x 10^{14} cm^{-2}

As seen in the SIMS profiles, for short diffusion time, a maximum concentration of the acceptors occurs at about 10 nm beneath the surface rather than at the surface where it is

expected to be from the solution of the diffusion equation. A similar behavior was also observed in the samples characterized by differential Hall technique. This anomalous diffusion behavior is attributed to the stresses of the SiO_2 diffusion cap arising either from its intrinsic stress or from the large difference in the coefficients of the thermal expansion of the SiO_2 (5×10^{-7} per°C) and InGaAs/InP ($5\text{-}7.4 \times 10^{-6}$ per°C). This results in a stress in the semiconductor that is greatest at the surface. The anomalous diffusion behavior arises because the diffusion coefficient which depends on stress,[61-62] varies with depth. For longer diffusion times, maximum acceptor concentration occurs at the surface because of the redistribution of the acceptors after the diffusant dose has exhausted.

Feasibility of Zn diffusion in InGaAs from the LB film was also investigated. Preliminary results are shown in Figure 3.11. SIMS profiles of Zn diffused InGaAs/InP shown in

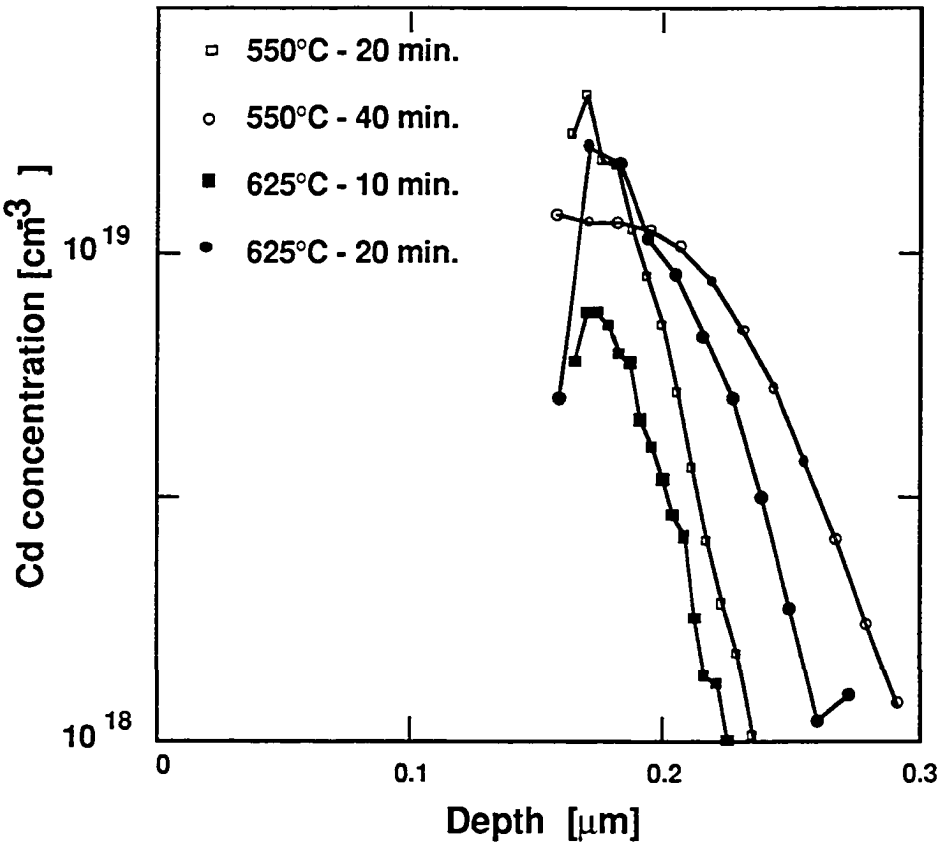


Figure 3.10: SIMS profiles of Cd diffused InGaAs/InP for different temperatures and time. Cd dose: 1.4×10^{15} cm^{-2}

Figure 3.11 were obtained by O_2^+ ion bombardment on the samples diffused at 600°C for 4, 10 and 16 minutes with the Zn sources of 1×10^{15} cm^{-2} for 4 and 16 minutes and 1.4 x

10^{15} cm^{-2} for 10 minute diffusion. A Zn implanted InGaAs/InP sample was used a standard such that the indicated scale of ion count is accurate within a factor of two. Base line in the figure corresponds to an equivalent instrumental background of 1 x 10^{17} cm^{-3}. A maximum zinc concentration of 5 x 10^{19} cm^{-3} is obtained for a 16 minute diffusion at 600°C.

3.5 Example Applications of LB Film to Optoelectronic Device Fabrication

Junction Field Effect Transistors (JFETs) and PIN photodetectors were fabricated using Cd diffusion from LB deposited Cd-Ar monolayers. Electrical characteristics of JFETs and PIN photodetectors are described in the next two sections.

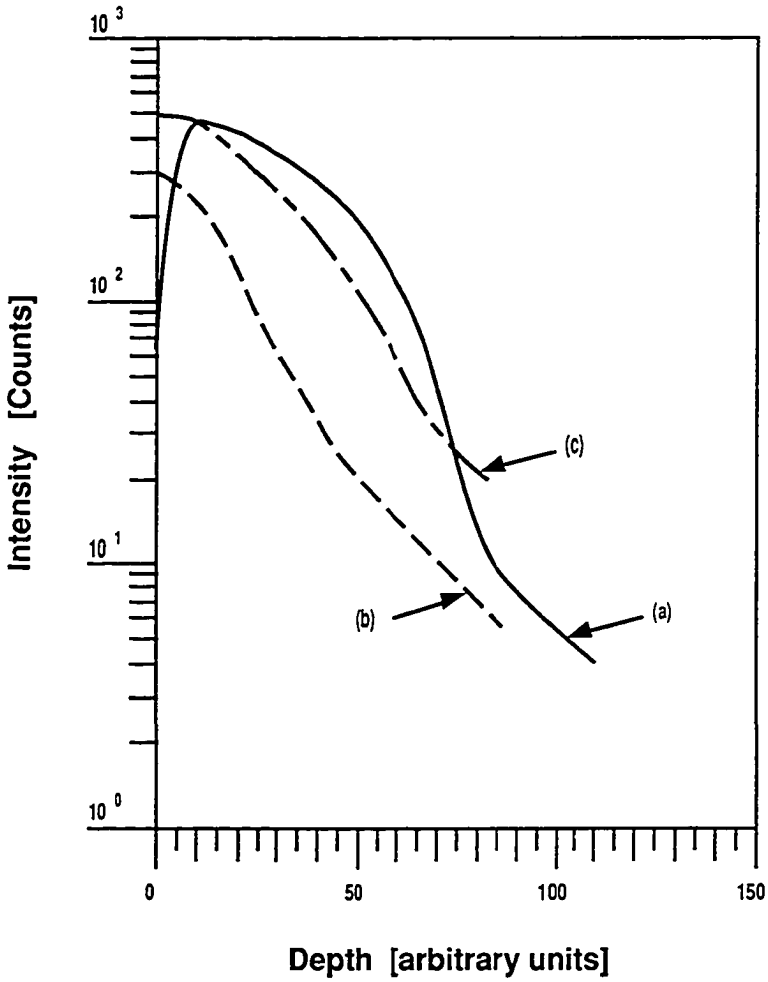


Figure 3.11: SIMS profiles of Zn diffused InGaAs/InP. Zn dose: 1.4 x 10^{15} cm^{-2}, Diffusion temperature: 600°C, Time (a) 10 (b) 4 and (c) 16 minutes

3.5.1 Junction Field-Effect Transistors

Low Schottky barrier heights and the absence of a good insulator in the InGaAs/InP system pose a challenge to the development of good field-effect transistors in this system. These shortcomings have stimulated the device researchers' interest in Junction Field-Effect Transistors (JFETs). An N channel JFET fabrication requires fabrication of a p type gate electrode over the channel for current modulation in the channel. While p-n junction gates can be epitaxially grown, it is difficult to include simultaneously an n^+ cap layer for low source resistance. JFETs with junctions diffused into epitaxially grown channel and n^+ cap layers can have lower source resistance and therefore higher extrinsic transconductance (g_m), an important figure of merit. For high performance diffused JFETs, the junction must be shallow and highly doped. Compared with a graded junction, an abrupt (shallow) junction can deplete more channel for a given change in gate bias, resulting in a higher g_m. A high gate doping similarly will deplete more channel for a given change in gate bias as well as decrease the gate resistance. A major parasitic contribution to the gate capacitance for short ($\leq$1 μm) gate lengths is the sidewall capacitance which becomes small only when the junction depth is smaller than the gate length. JFET fabrication using Cd diffused p^+ gates, as described in the next section meets these requirements.

3.5.1.1 JFET Fabrication and DC Characteristics

For JFET fabrication a 250 nm n^+ InGaAs cap, a 10 nm n^+ InP stop etch, and a 400 nm thick n = 6 x 10^{16} cm^{-3} InGaAs channel were grown on a semiinsulating InP substrate by OMCVD. The JFET was fabricated following the process sequence outlined below. The fabrication sequence is also shown in Figure 3.12.

(a) Mesa definition by photolithography and isolation down to the semiinsulating InP substrate by ion milling.

(b) Eighty nm silicon nitride mask deposition by PECVD.

(c), (d) 1. Gate window definition in SiN by photolithography and CF_4 plasma etching of SiN for Cd diffusion.

2. The n^+ InGaAs contact layer etching from the gate window by 1 H_3PO_4 : 1H_2O_2 : 38 H_2O and n^+stop-etch removal by 1 HCl : 10 H_3PO_4

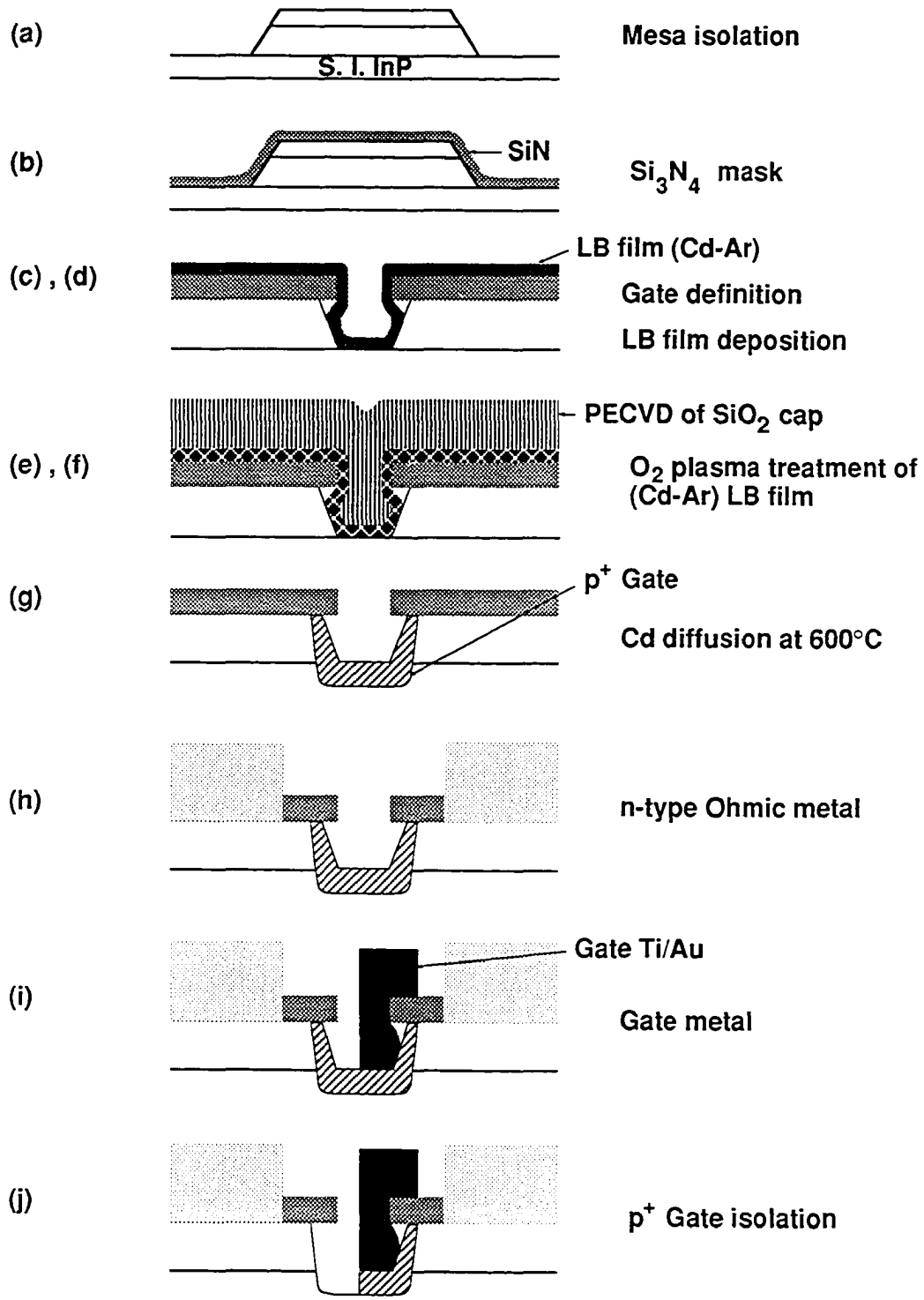


Figure 3.12: JFET fabrication sequence

3. Eight monolayers of Cd-Ar LB film deposition.

(e), (f) 1. O_2 plasma treatment of Cd-Ar LB film.

2. PECVD of ~150 nm thick SiO_2 cap for diffusion.

(g) P^+ gate formation by Cd diffusion at 600°C in a rapid thermal annealer.

(h) N-type ohmic contacts to the source and drain.

(i) Ti/Au gate metallization.

Figure 3.13 shows a source-drain I-V characteristics of a typical JFET. The JFET had a saturated drain current I_{dss} = 50 mA/mm, transconductance g_m = 80 mS/mm, contact resistance obtained from transmission line measurements R_c = 0.11 Ω-mm, and gate-channel breakdown voltage V_b = 1.6 V. The channel breakdown was increased to 3.5 V by isolation of diffused p^+ gate from the channel, as shown in the Figure 3.12(j). The p^+-n^+ junction, as shown in Figure 3.12 (g), leads to a lower gate breakdown voltage. The low junction breakdown voltage may also be from a sharp curvature in the gate-channel p^+n junction leading to a high field region along the gate periphery. Formation of a sharp curvature in the gate-channel junction is attributed to the stresses of SiN cap.

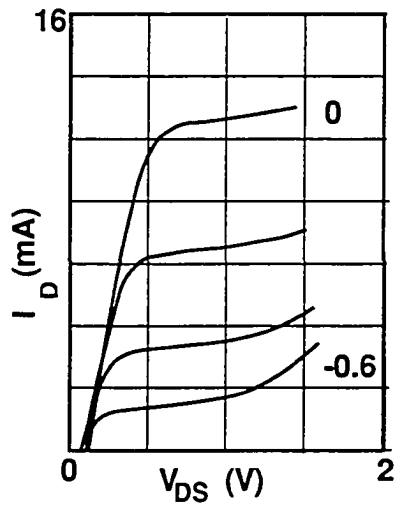


Figure 3.13: Drain I-V characteristics of a JFET made using Cd diffusion from the LB film. V_G/ step = -0.2 V.

3.5.2 PIN Photodetectors

A PIN photodetector is essentially a p-n junction diode with an intrinsic, light absorbing layer sandwiched between the p and the n type electrodes. A PIN photodetector is operated with small ~5 V reverse bias across it such that the intrinsic layer is completely depleted. When light of appropriate wavelength is shone on the detector, hole-electron pairs are generated in the depleted, intrinsic layer with the absorption of photons. The holes and the electrons are separated by the electric field in the intrinsic layer and collected by the p and the n type electrodes, respectively. With a field of greater than 2×10^4 V/cm, the charge carriers traverse the intrinsic layer with saturation velocity. The internal quantum efficiency, the ratio of the carrier pairs generated per incident photon, of the detector is given by

$$\eta_i = (1 - e^{-\alpha d})\ 100\ \% \qquad (3.1)$$

where α is the absorption coefficient of the intrinsic layer in cm^{-1}, and d is the thickness of the intrinsic layer in cm. The responsivity, R, of the PIN photodetector, defined as the current produced per unit optical power incident, is given by

$$R = \frac{\eta_i\, q}{h\, \nu} = 0.805\, \eta_i\, \lambda \qquad (3.2)$$

where ν is frequency of incident radiation and λ is the wavelength of the incident radiation in μm. Thus, the detector responsivity depends on its quantum efficiency and the wavelength of the incident radiation.

The bandwidth of the PIN photodetector depends on the carrier transit time across the intrinsic layer and the RC time constant of the detector. For the detector with thick intrinsic layer, quantum efficiency is high but carrier transit time is also high which limits its bandwidth. Shorter transit times are obtained with a thinner intrinsic layer which increases the detector capacitance and decreases its quantum efficiency. The bandwidth of a detector with thin absorbing layer is limited by its capacitance. Thus the PIN photodetector bandwidth is either transit time limited or capacitance limited. The bandwidth of a transit time limited detector is given by

$$B = \frac{v_S}{2\pi\, d} \qquad (3.3)$$

where v_S is the saturation velocity of holes. The bandwidth of the capacitance limited detector is given by

$$B = \frac{1}{2\pi\ R\ \ C} \qquad (3.4)$$

where C is the detector capacitance in Farads and R is the resistance of the measurement circuit. A good PIN photodetector design is a compromise between the two extremes described above.

While shallow p^+-n junctions are not an absolute requirement for PIN photodetectors, their use can certainly improve the detector performance. For a top illuminated PIN photodetector with a highly doped, shallow p^+-n junction, carrier generation in the low field surface region is low, so the loss of quantum efficiency is minimum. With fewer carriers in the low field surface, diffusion of electrons, a slow charge transport process, can be kept lower for high speed signal detection. Another advantage of diffused junction is that local diffusion of acceptors through a mask can result in photodetectors with dark currents approaching the theoretical minimum.[63] The shallow p^+-n junction fabrication technique developed in the previous section can readily be used for such photodetector fabrication.

3.5.2.1 PIN Photodetector Fabrication

A PIN photodetector was fabricated in an OMCVD grown epitaxial layer structure consisting of a 100 nm undoped InP and 2.5 μm thick intrinsic InGaAs on n^+ InP wafer. The photodetectors were fabricated by selective diffusion of Cd from the LB film through a window in silicon nitride mask. The complete fabrication process is outlined below.

1. One hundred nm silicon nitride mask deposition by PECVD.

2. Active area definition for diode by photolithography and selective etching of SiN by CF_4 plasma.

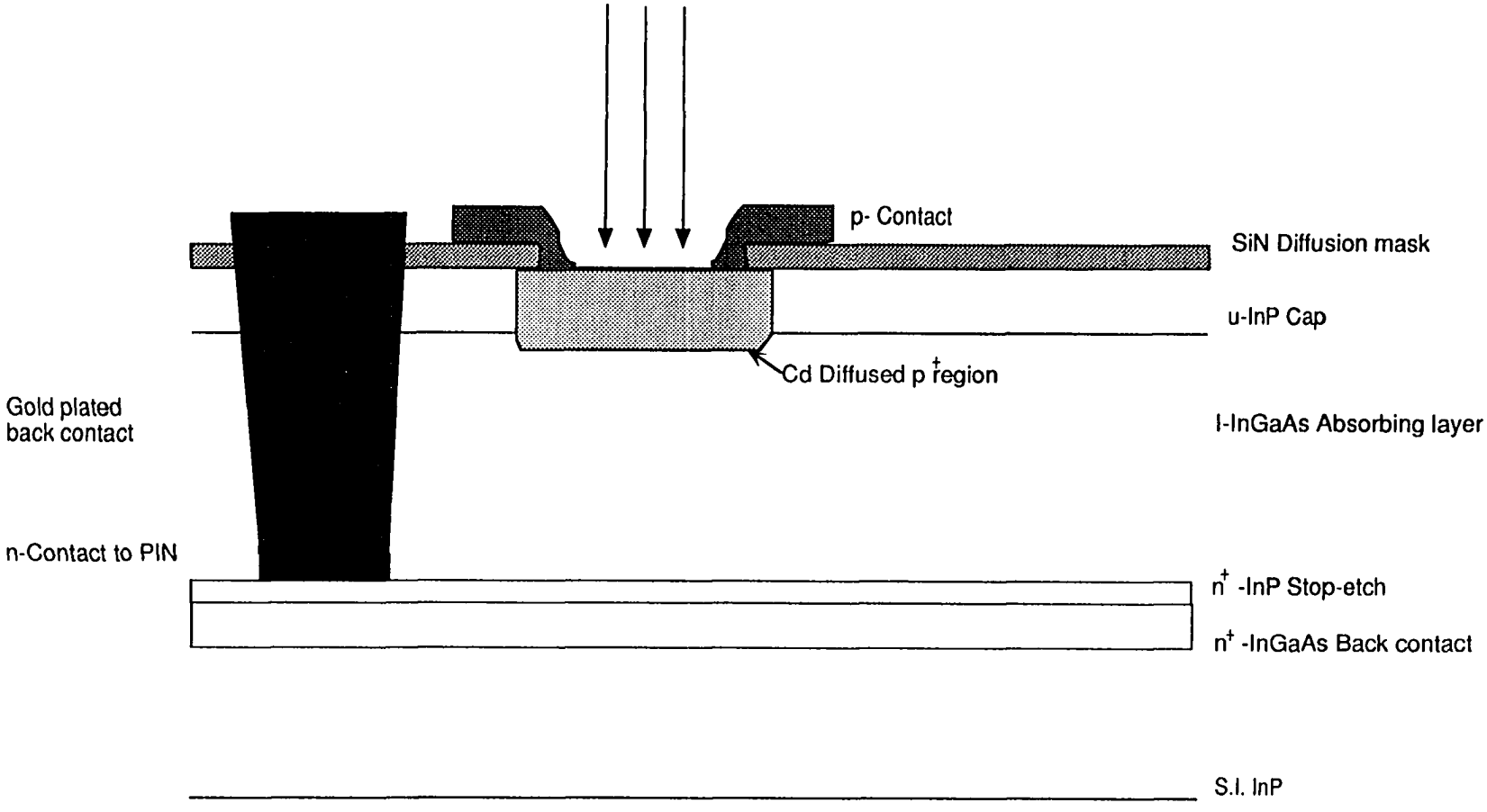


Figure 3.14: Cross section of a PIN photodetector fabricated using Cd diffusion from LB film

3. Eight to twelve monolayers of Cd-Ar deposition in LB trough.

4. Oxyplasma treatment of Cd-Ar to remove hydrocarbons from it.

5. One hundred fifty nm SiO_2 cap deposition by PECVD.

6. Cd diffusion at 600°C for 20 minute under flowing argon in a furnace.

7. Ohmic contact to the top p^+ electrode.
8. N-type ohmic contact to the back side.

9. Simultaneous annealing of p and n-type ohmic contacts in a rapid thermal annealer at 420°C for 20 s under flowing argon.

Figure 3.14 shows a cross section of a completed PIN photodetector. A typical reverse I-V characteristics of a 30 μm diameter diode in dark is shown in the Figure 3.15. As seen in the figure, the detector had a dark current of 100 pA at -5 V reverse bias. This is comparable to that obtained in PIN photodetectors made by conventional diffusion technique. The dark current is low because the only part of the junction that is exposed and therefore can be a source of generation current, occurs in the wide bandgap InP rather than the narrow bandgap InGaAs.

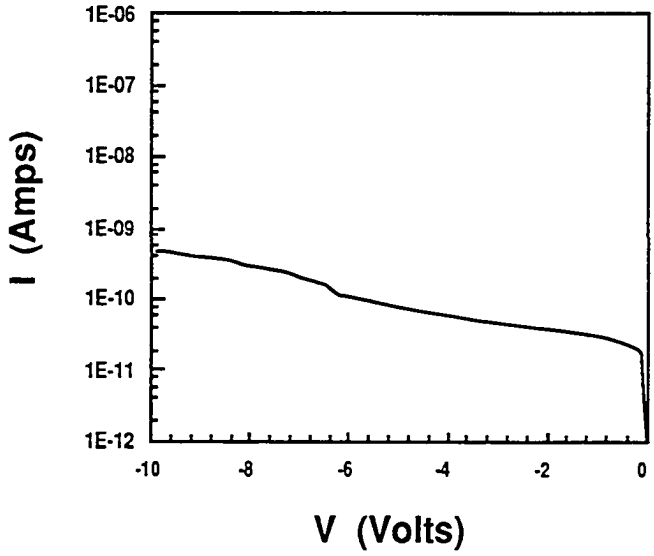


Figure 3.15: PIN photodetector characteristics in dark.
Detector diameter : 30 μm,Dark current: 100 pA at -5V

A new epitaxial layer structure on semiinsulating InP was designed to make photodetectors for OEICs which required low capacitance at the amplifier input. The OMCVD grown layer structure on semiinsulating InP had 10 nm cap layer of undoped InGaAs, 100 nm undoped InP, 2.5 μm absorbing layer of intrinsic InGaAs, 50 nm n^+ InP etch stop, and 250 nm n^+ InGaAs for ohmic contact to back side of PIN. The thin InGaAs layer on top prevents a chemical reaction between InP and ammonia from a mixture of silane, ammonia, and argon gases used for PECVD silicon nitride deposition. About 0.2 μm of intrinsic InGaAs is converted into p^+ and the remaining 2.3 μm of the intrinsic InGaAs absorbing layer yields ~89% internal quantum efficiency. DC and pulse response characteristics of these detectors are described in the next section.

3.5.2.2 PIN Photodetector Characterization

Photodiodes with 2.3 μm absorbing layer and 40 μm diameter were characterized using a 1.3 micron wavelength laser pulsed at 40 ps FWHM. The laser light was coupled into the detector by a single mode, pig-tailed silica optical fiber. An internal quantum efficiency η_i = 84% and a responsivity R = 0.88 A/W were obtained. The detector had a reverse breakdown voltage V_b = -2.5 V. The lower breakdown is attributed to the stresses of the diffusion cap, as conjectured in the previous section on JFETs.

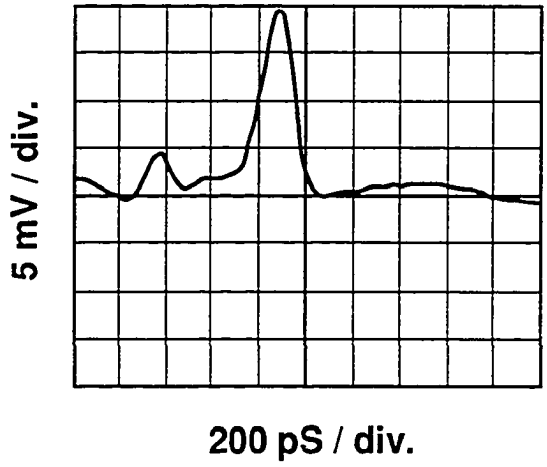


Figure 3.16: Pulse response of a PIN detector made using Cd diffusion from the LB film.The full width at half maximum (FWHM) is 160 ps, which corresponds to 2 GHz bandwidth

A measurement set up used for obtaining pulse response of the photodetector consisted of an HP 8656 signal generator and a Tektronics sampling scope TEK 7854 with trigger

module S-53 and a sampling head S-4. As shown in Figure 3.16, a response pulse with full width at half maximum (FWHM) of 160 ps was obtained, corresponding to a 2 GHz bandwidth. Capacitance measurement made on a detector without a large pad on p-type InGaAs showed that the bandwidth was limited by the pad capacitance. An intrinsic bandwidth calculated from the detector capacitance was ~20 GHz. The tail in the photodetector pulse response may be from the holes trapped at the InP/InGaAs interface due to large difference in their bandgaps. This abrupt change in the bandgap can be eliminated by use of a compositionally graded quaternary $In_xGa_{1-x}As_yP_{1-y}$ instead of InP.

3.6 Summary

Shallow p^+-n junction fabrication has been accomplished with a simple process employing a LB film as a diffusion source for accepters. With the use of LB films, large area diffusion is also simplified. The use of the LB film allows the quantity of diffusant to be precisely controlled through the film deposition conditions. A new technique of diffusion without a diffusion mask is also proposed. This new source can be adapted to diffusion of other dopants by the use of an appropriate buffer solution and amphiphilic molecule of hydrocarbon. PIN photodetectors with low dark currents have been fabricated. Preliminary investigation of JFET fabrication by Cd diffusion from LB film diffusion source also has been done. Further optimization of the diffusion cap is required to reduce the stresses and to obtain better junction breakdown characteristics.

CHAPTER 4

ELO and LB Film Application to Optoelectronic Integrated Circuits

4.1 Introduction

An application of ELO GaAs to integrated circuit (IC) amplifier fabrication is described in this chapter. The amplifier had a DC gain of 2 and an RC time constant limited bandwidth of 500 MHz. An optoelectronic integrated circuit (OEIC) photoreceiver for 1.3-1.55 μm optical fiber communication system that uses a novel fabrication technique is also proposed. The proposed OEIC uses the ELO GaAs MESFET and InGaAs/InP photodetector described in the previous two chapters.

This chapter is divided into four sections. Various approaches of realizing OEICs for 1.3-1.55 μm wavelength photoreceivers are reviewed in section 4.2. The proposed OEIC photoreceiver with a possible fabrication sequence is described in section 4.3. Fabrication and characterization of a high input impedance amplifier using ELO GaAs MESFETs is also described in the section 4.3. Section 4.4 contains a summary.

4.2 Review of OEICs for 1.3-1.55 μm Wavelength Optical Communication

Long distance optical communication at 1.3-1.55 μm wavelength is attractive because of low signal dispersion and loss in the silica optical fibers at these wavelengths. While the information transmission over the fibers is in lightwaves, the communication equipment at either end is electronic and can process only electrical signals. The need for electrical- to-optical and optical-to-electrical conversion has resulted in the advent of optoelectronic transmitters and receivers. The transmitters and receivers in current use are made by integrating separately fabricated and individually selected lasers, photodetectors, and amplifiers, commonly known as 'hybrids'. Bandwidth of the hybrids is limited by large parasitic inductance and capacitance associated with wire bonds used for interconnecting the optical and electronic components. Monolithic integration of optical and electronic components into an optoelectronic integrated circuit (OEIC) can overcome this problem. Mass production of OEICs through batch processing can also bring more uniformity to receiver/transmitter performance characteristics and lower their cost. Therefore, the OEICs for 1.3-1.55 μm wavelength optical communication are of much current interest.[64-65-66-

[67-68] The $In_{0.53}Ga_{0.47}As$ (hereafter referred to as InGaAs) has a large absorption coefficient in the same range. InGaAs also has high electron mobility and high saturation velocity, basic requirements for high performance transistors. These properties make InGaAs, lattice matched to InP, a desirable material for OEICs. However, low Schottky barrier height and absence of a suitable gate insulator in the InP material system has been a major obstacle in developing a transistor technology.

OEIC photoreceivers potentially have higher sensitivity than hybrid receivers, but due to inherent incompatibility of photodetector and transistor material requirements and large gate leakage in InGaAs FETs, performance tradeoffs have resulted in poor OEIC receiver sensitivity. InP based OEIC photoreceivers described in the above mentioned references also have not matched the performance of the hybrid photoreceivers made from InGaAs/InP photodetectors and GaAs amplifier circuits. A new technique of OEIC fabrication proposed in the next section can overcome the problem.

4.3 Proposed OEIC Photoreceiver

Several high performance heterostructure FET technologies exist for III-V compound semiconductors. For the reasons mentioned earlier, an OEIC based on a single material system such as InGaAs/InP is very attractive but difficult to implement. In the early stage of the project I proposed to fabricate an OEIC based on single material system, namely, InGaAs/InP. As described in Chapter 3, Junction Field-Effect Transistors (JFETs) and PIN photodetectors were fabricated using our newly developed technique of cadmium diffused shallow p-n junctions. Inherent incompatibility of the PIN photodetector and JFET material layer structure make OEIC processing very complex and several performance tradeoffs would have to be accepted in favor of simpler fabrication procedure. These efforts were abandoned in favor of Dr.Winston Chan's proposal of realizing the photodetector and the amplifier in InGaAs/InP and GaAs, respectively. Since GaAs material and device technology is mature, fabrication of an amplifier using GaAs MESFETs is relatively simpler. This new technique of OEIC photoreceiver fabrication takes advantage of the device technologies for both material systems. The photoreceivers made using this new technique are expected to have the following advantages over the conventional hybrid photoreceivers and OEIC photoreceivers made using heteroepitaxial and homoepitaxial semiconductors.

1. Higher sensitivity compared to that typically obtained from MSM type photodetectors, as described in the next section.

2. Low noise resulting from extremely low dark current of the photodetector.

3. A low dielectric constant buffer layer between the detector and MESFETs can be chosen independent of material growth requirements to obtain low interconnect capacitance.

4. Lowest reported sidegating (drain current modulation by neighboring devices) for less cross-talk which is a major problem in GaAs integrated circuits.

5. Possibility of large scale OEIC production at lower cost, compared to labor intensive and time consuming hybrid circuit fabrication.

4.3.1 Photodetector Selection Criteria for OEIC

Many different types of photodetectors exist: metal-semiconductor-metal (MSM), PIN, avalanche photodiode, photoconductors, etc. The choice of detector type is governed by noise, sensitivity, gain, speed and power supply requirements. Avalanche photodetectors can achieve higher sensitivity but the noise associated with the avalanche process can reduce the dynamic range of the detector. Low step coverage and operating voltage make an MSM type detector highly suitable for integration with FETs. When fully depleted, an MSM type detector exhibits very low (~ fF) capacitance and can be operated at high speeds but its sensitivity is limited by the electrode shadow and depletion depth.[69] A PIN type detector has several advantages over APD and MSM type detectors. In the 1.3-1.5 μm wavelength range, an InP/InGaAs/InP double heterostructure PIN photodetector described in Chapter 3 can achieve extremely low dark current. With a proper choice of absorbing layer thickness and antireflection coating, its quantum efficiency can be maximized (up to ~ 95% and higher) with some reduction in the response speed. The ability of obtaining low dark currents and high quantum efficiency is translated into highly sensitive, low noise detection of signal. The locally diffused PIN photodetectors are planar, which is a prerequisite for bonding ELO GaAs to the new host containing photodetectors.

Because of these advantages, the PIN photodetector has been chosen for the OEIC.

4.3.2 OEIC Fabrication Process

The OEIC is fabricated in two stages. In the first stage, an InGaAs/InP PIN photodetector is fabricated on a semiinsulating InP substrate using the technique of Chapter 3.

In the second stage of the OEIC fabrication, a transimpedance or high input impedance type amplifier is made in an OMCVD grown GaAs MESFET layer structure lifted-off from its growth substrate and grafted onto the InP substrate containing PIN type photodetectors fabricated in the previous stage. This avoids heteroepitaxial growth of GaAs on InP and eliminates the need for growing a high dielectric constant semiconductor for isolation between the detector and the FETs. The GaAs MESFETs with alloyed contacts and without recessed gates, as described in the chapter on ELO GaAs FETs, are used for high input impedance and transimpedance amplifiers in the grafted ELO GaAs layer. At the end, the detector and the amplifier are connected with a via in the buffer layer.

The choice of dielectric buffer layer is very important. It must have low dielectric constant, must be transparent for the ease of alignment of the GaAs devices with the PIN photodetectors and must be compatible with both GaAs and InP processing. The buffer must be smooth, planar and hydrophilic for bonding ELO GaAs to it. The requirement of planarity is very strict for bonding ELO GaAs film to the new host. A rough wafer surface results into poor adhesion of the ELO GaAs. Silicon dioxide or silicon nitride can meet all these requirements. At the semiconductor fabrication facility of Bellcore, insulating layers of SiO_2 and Si_3N_4 can be deposited using PECVD. These are suitable as masks for device processing but do not have adequate uniformity in thickness over large area and their growth rate is very slow (2-6 nm/min). Therefore, they are not suitable as an integral part of the OEIC. So, a search for suitable buffer layer was started. Dr. Steven Dzioba of Bell Northern Research, Ottawa, Canada, agreed to deposit thick SiO_2 using his electron cyclotron resonance (ECR) plasma deposition system on the InP wafers with PIN photodetectors provided by me. The ECR deposited SiO_2 was found very uniform over large area and ELO GaAs film could be easily bonded to it. The ECR SiO_2 was also transparent and could be etched selectively using RIE. Wet chemical etching of the ECR SiO_2 is not recommended due to very high etch rate resulting in large undercut. However, the etch rate can be reduced by densifying the SiO_2 at high (500-700°C) temperature. Because of the need for sending the PIN wafers to Canada for the SiO_2 deposition, I decided to try an alternative technique of forming thick buffer layer.

Next, spin-on glass (SOG) was chosen as a buffer because it is simple to use and many different types of spin-on glasses are commercially available. An SOG is a hydrocarbon polymer containing SiO_2, can be easily dissolved in organic solvents and spun-on like photoresist. Until recently, only very thin ~100 nm coating of SOG could be applied to a sample without cracking, but recent advances in technology has made it possible to use several micrometer thick coating of SOG without developing cracks. While looking for a suitable SOG formulation, I came across an experimental SOG from Owens-Illinois, a manufacturer of synthetic polymers. With the help of Dr. Brian Bagley and T. S. Ravi, members of technical staff of Bellcore, I developed a process using SOG that has been described in Appendix. Seven hundred fifty nm thick SOG could be spun-on in a single coat. With multiple spins, up to 2.25 μm thick glass coating can be obtained. The SOG coated wafer was cured in air at 130°C for 1 hour to remove solvents. Chemically bonded hydrocarbon polymers must be removed from the SOG to obtain SiO_2. Complete curing of the SOG required high temperature (400°C) treatment for 1-2 hours. Because of a large difference in the thermal expansion coefficients of SOG and InGaAs/InP, the glass developed cracks after the high temperature curing. Bonding of ELO GaAs to cracked SOG would have been difficult because of nonplanar surface. So, the SOG was not cured at high temperature, instead, it was treated with oxyplasma for one hour to remove hydrocarbons from the top layer and make it hydrophilic for bonding ELO GaAs to it. The process worked well for a device fabrication sequence requiring three to four mask levels but the yield of testable OEICs was significantly affected by poor erosion resistance of partially cured SOG to acetone used for dissolving photoresist.

The OEIC fabrication sequence can be outlined as follows.

Stage I: PIN photodetector fabrication

1. One hundred nm thick PECVD silicon nitride mask deposition on an InP wafer with OMCVD grown PIN photodetector layers.

2. Definition of photodetector active area by photolithography and CF_4 plasma etching of silicon nitride.

3. Deposition of ten monolayers of Cd-Ar LB film using LB deposition system described earlier.

4. Oxyplasma treatment of LB film to remove hydrocarbons from it.

5. Deposition of 150 nm thick PECVD silicon dioxide cap for semiconductor surface protection during high temperature diffusion.

6. Cadmium diffusion at 600°C for 20 minutes under flowing argon on a graphite plate heated by quartz lamps.

7. Removal of SiO_2 cap by a buffered oxide etchant.

8. P-type Ohmic contact to the diffused p^+ region.

Stage II: ELO GaAs MESFET amplifier fabrication

A. Dielectric buffer layer formation

1. Apply two coats (0.75 μm each) of spin-on glass (SOG) by two sequential spins with one hour baking in air at 130°C after each coat.

2. Removal of hydrocarbons from the SOG surface by oxygen plasma treatment for one hour. This step is essential for making the SOG surface hydrophilic for attaching ELO GaAs film to it.

B. Amplifier fabrication in ELO GaAs

1. Lift-off a GaAs MESFET layer structure from its growth substrate and attach it to the wafer processed in previous step.

2. Formation of N-type ohmic contact to FET source and drain.

3. FET mesa formation by photolithography and ion milling down to the SOG.

4. Back side n contact to the PIN photodetector by photolithography, reactive ion etching of SOG, wet chemical etching of PIN layers, electron beam evaporation of n-type metal and lift-off.

5. Simultaneous annealing of the p PIN and n FET contacts at 370°C for 20 s under flowing argon in a rapid thermal annealer.

6. One micron gate definition, Schottky metal deposition and lift-off.

7. Via hole definition by photolithography.

8. Filling the via hole by gold plating to bring the PIN back side contact pad on SOG surface to keep all the interconnects and pads in the same plane.

9. Interconnect definition by photolithography, electron beam evaporation of 5 nm Cr/ 200 nm Au and lift-off.

The process described above is realized with a set of ten photomasks. A cross sectional view of the OEIC is shown in Figure 4.1.

The above fabrication process was used for the OEIC fabrication for several times. Working OEIC has not been realized because of low yield of testable circuits. A photomicrograph of a completed OEIC with transimpedance amplifier is shown in Figure 4.2. The yield has suffered because of the poor erosion resistance of the SOG to the solvents used for circuit processing. Another problem is the adhesion of the ELO GaAs film to the new host. With the altered fabrication sequence described in the Chapter 2, yield was improved significantly. However, when the ratio of ohmic metal on GaAs to that on buffer was increased, the adhesion of the FET mesa was also reduced. It did not reduce yield significantly for short processing sequence up to three to four mask levels but the OEIC yield did suffer because of twice as many process steps.

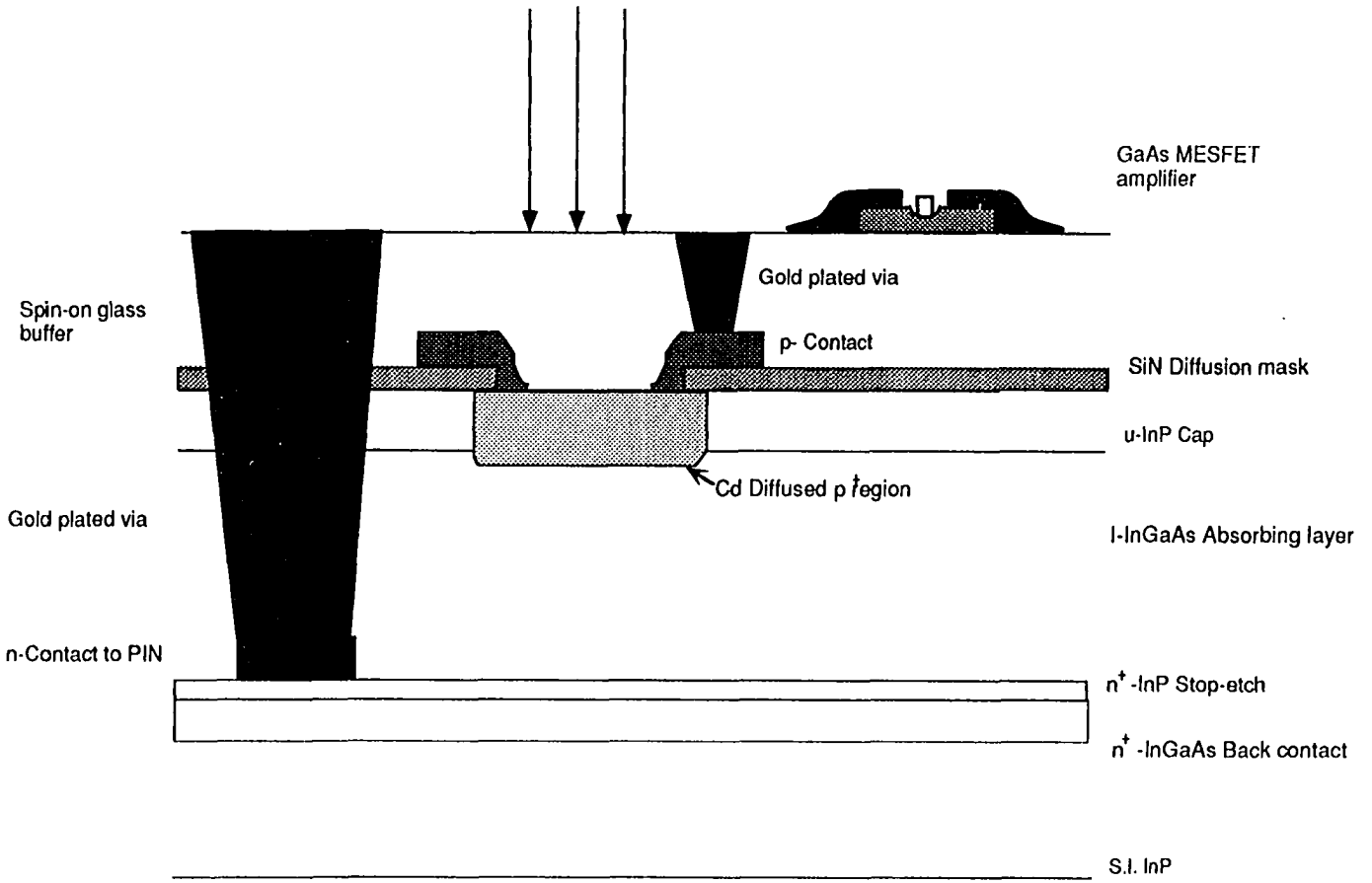


Figure 4.1:Cross sectional view of an OEIC in ELO GaAs/InP

Figure 4.2: A photomicrograph showing a completed
ELO GaAs / InGaAs / InP OEIC with transimpedance amplifier.
The amplifier has total 14 components. Die size: ~1200 μm x 1000 μm

4.3.3 High Input Impedance and Transimpedance Amplifiers in ELO GaAs

High input impedance and transimpedance amplifiers in ELO GaAs on silicon were fabricated first to test the integrability of the ELO FETs. This was also necessary to assess the intrinsic performance of the amplifier circuits. The amplifiers were fabricated using the same mask set as the one designed for the OEIC. The fabrication sequence is outlined below.

1. ELO of GaAs MESFET layer structure from its growth substrate and Van der Waals bonding to a silicon substrate with 1.3 μm thick thermally grown SiO_2.

2. N-type ohmic contacts to the source and drain.

3. Mesa isolation down to SiO_2 buffer by ion milling.

4. The ohmic contact annealing at 370°C for 20 s under flowing argon.

5. One micron long Ti/Au Schottky gate formation.

6. Interconnect formation by photolithography, 5 nm Cr/ 200 nm Au deposition and lift-off.

Photomicrographs of completed transimpedance and high input impedance amplifier circuits are shown in Figures 4.3 and 4.4, respectively. A schematic of the high input impedance amplifier is shown in Figure 4.4(a).

Figure 4.5 shows DC transfer characteristics of a high input impedance amplifier measured using an HP 4145 transistor parameter analyzer. The amplifier had a DC gain of 2. The amplifier was also tested up to 10 MHz. The test frequency was limited by the probe impedance. From the gate capacitance and input resistance measurement on the driver MESFET, a 500 MHz bandwidth was estimated for the amplifier. A discrete MESFET with 1.2 μm gate length on the same wafer had a unity current gain frequency f_t = 10 GHz. The transimpedance amplifier was not tested because of the unavailability of high frequency probe card.

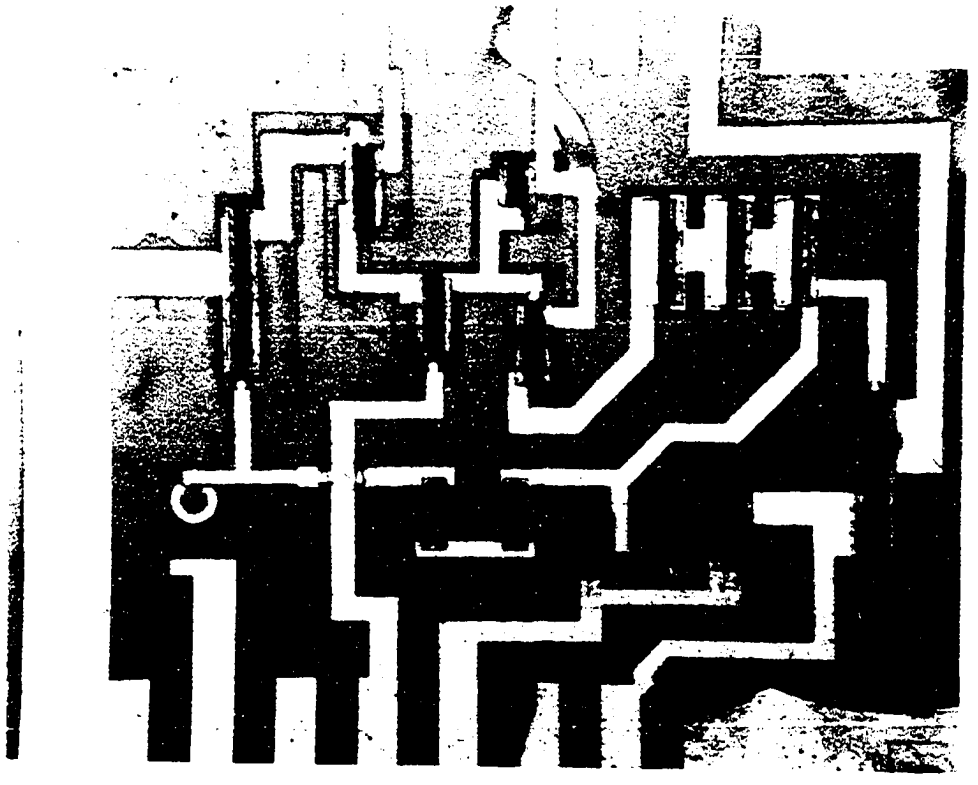


Figure 4.3: A photomicrograph showing a completed ELO GaAs / Si transimpedance amplifier. The amplifier has total 13 components. Die size: ~1200 μm x 1000 μm

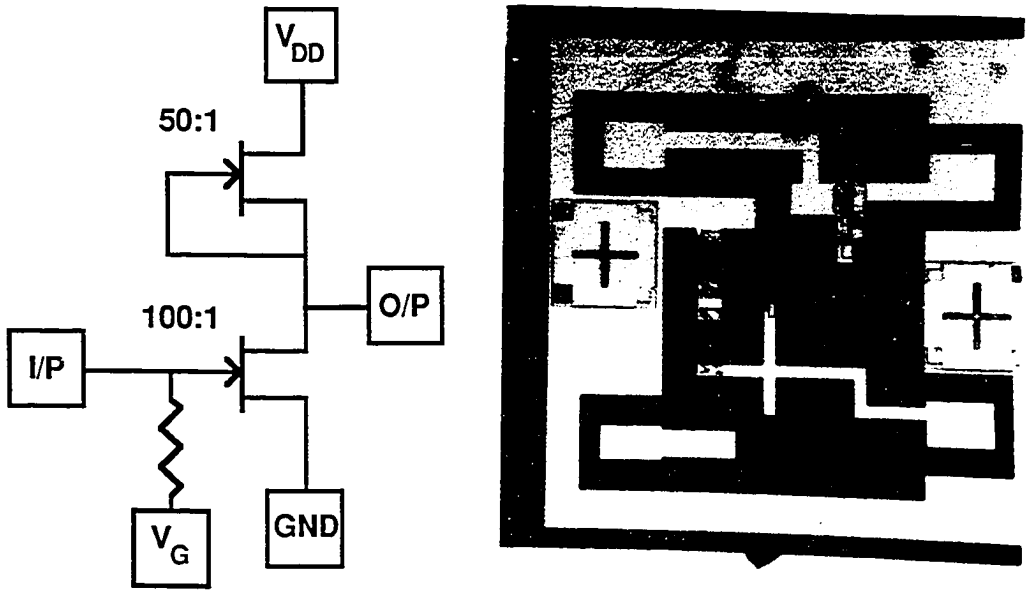


Figure 4.4: (a) Schematic of a high input impedance amplifier made using ELO GaAs MESFETs. (b) Photomicrograph of the same amplifier

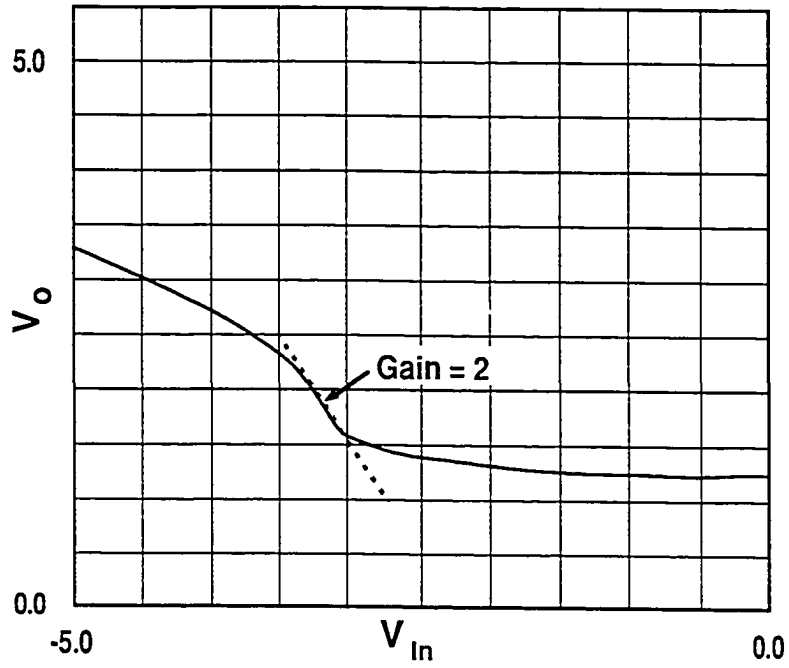


Figure 4.5: I/O characteristics of an ELO GaAs high input impedance amplifier on Si

4.4 Summary

High input impedance and transimpedance OEIC photoreceiver fabrication has been attempted using a novel technique of hybrid integration. Working OEIC has not been realized due to very low yield of testable circuits. However, a high input impedance amplifier was tested from DC to 10 MHz. The amplifier exhibited a DC gain of 2 and an input RC time constant limited bandwidth of 500 MHz. This is the first ever demonstration of a small scale integrated circuit fabrication using ELO GaAs. To summarize: the hypothesis of using ELO GaAs for integrated circuit has been successfully tested. A hybrid integration of GaAs on InP has also been accomplished by the use of ELO GaAs FETs and PIN photodetectors fabricated using Cd diffusion from LB films. This is a first ever conceptual demonstration of hybrid integration of InP and GaAs for photoreceiver fabrication. This is also the first demonstration of integrating thirteen components using ELO GaAs. The problems that must be solved before ELO GaAs technology can be routinely used as an alternative to the heteroepitaxy of GaAs on InP are: developing a better buffer layer and improving the adhesion of the ELO GaAs to the buffer. The ECR SiO_2 is a potential candidate for buffer layer.

CHAPTER 5

Conclusions

Conclusions from the experimental investigation of epitaxial lift-off and Langmuir-Blodgett thin films for optoelectronic device applications are presented in this chapter. Section one contains results and conclusions of investigation of ELO GaAs FETs. Section two contains summary of experiments with LB film diffusion source for optoelectronic devices along with conclusions. Like any other investigation of novel techniques, this one is also not complete by itself and some more work is required to optimize the techniques discussed in the earlier chapters. Suggestions for future research on ELO GaAs and diffusion from LB film are given at the end of sections one and two, respectively.

5.1 Epitaxial Lift-off For Substrate Independent GaAs FETs

This is the first published systematic and comprehensive study of epitaxial lift-off GaAs and AlGaAs/GaAs for high performance FETs. Substrate independence of ELO GaAs MESFETs has been demonstrated by fabrication and electrical characterization of the MESFETs on silicon and sapphire substrates. The findings of this study can be summarized as following.

An ELO MESFET on silicon with 0.1 μm gate length had f_t = 34 GHz and f_{max} = 23 GHz, both limited by parasitic gate capacitance from the conducting silicon substrate. An ELO AlGaAs/GaAs HEMT with ~1.1-1.2 μm gate length exhibited f_t = 14 GHz, and f_{max} = 12.5 GHz, slightly lower than typical HEMT with this gate length.

As shown in the Table 2.2, the ELO FETs have exhibited excellent DC as well as RF characteristics irrespective of the host substrate. Thus, the ELO preserves DC and RF performance characteristics of the GaAs FETs.

With the ELO, island isolation of devices is made possible and extremely low leakage currents between the devices are obtained. Sidegating has also been largely eliminated.

From the statistical study of I_{dss} and g_{mi} distributions across an ELO HEMT and on-wafer HEMT samples it is concluded that the ELO FETs are not significantly different from the on-wafer FETs.

ELO GaAs MESFETs have been successfully used for a high input impedance amplifier exhibiting a DC gain of 2 and a RC time constant limited bandwidth of 500 MHz. This is the first demonstration of ELO GaAs for small scale integrated circuit application.

An OEIC using an InGaAs/InP PIN photodetector and an amplifier in ELO GaAs MESFETs has also been attempted. A completed OEIC was not tested because of very low yield of testable circuits. The yield has suffered due to poor adhesion of ELO GaAs film to the SOG buffer layer used on PIN photodetectors for electrical isolation of the two.

All of the observations listed above establishes that ELO presents a potential alternative to the heteroepitaxy of GaAs on silicon, InP, dielectrics (such as sapphire and glass) and any other substrate of interest.

In spite of the excellent DC and RF performance characteristics of the ELO FETs, several fundamental issues related to the ELO GaAs processing must be resolved for fully exploiting the new technique. First and foremost is the adhesion of the ELO GaAs film to the new host.

As shown in the chapter two, the Van der Waals bonding is not always adequate for keeping the GaAs film in place. Some kind of external reinforcement, such as tacking the mesas down by ohmic metal before mesa isolation, is required. This is crucial for the survival of the ELO GaAs film to the end of the processing sequence which involves several metallizations and etchings. As seen in chapter two, the high frequency performance of the ELO FETs has suffered from capacitive coupling to the conducting silicon substrate as well as higher parasitic source and drain resistances. The former can be eliminated by increasing thickness of the buffer but a significant reduction of the latter requires the use of n^+ cap for ohmic contacts and a gate recess etch with uniform etching over large area. Dry etching of GaAs with low radiation induced damage must be developed for this purpose. The non-uniformity of gate recess etch is believed to arise from inhomogenious stresses of the ELO GaAs film. The stresses in the film may also have reduced the Hall mobility by 15-20% in 2-DEG at the AlGaAs/GaAs heterointerface by spatial variations in the bandgap that can give rise to additional scattering

For the OEIC using ELO GaAs on InP ~2 μm thick spin-on glass was used as a buffer as described in Chapter 4. The yield of testable OEICs was significantly affected by poor

erosion resistance of the SOG to the solvents. The SOG also developed cracks after ohmic contact annealing. Although the cracks are cosmetic in nature, they can also stress the ELO GaAs. So, a buffer layer with better physical characteristics must be used in the future.

5.2 LB Films for Optoelectronic Devices

A new application of LB deposited Cd-Ar and Zn-Ar monolayers for Cd and Zn diffusion has been demonstrated for the first time. Highly doped (N_A = 2-4 x 10^{19} cm^{-3}), shallow ~0.1 -0.4 μm p^+-n junctions in InGaAs/InP have been obtained. Following advantages of the new diffusion source over conventional sources have also been demonstrated:

Dopant dose is accurately controlled through the total number of LB film monolayers because each layer has a fixed density of Cd or Zn ions (2 x 10^{14} cm^{-2}).

Better control over junction depth is obtained through rapid heating and cooling of the sample in the rapid thermal annealer as opposed to the conventional closed ampoule or open tube diffusion in furnace that requires temperature ramp up/down times comparable to the total diffusion time.

This new technique is a safer method of handling potentially toxic Cd because only extremely small amount (~46 mg/liter of water) of $CdCl_2$ is required. Moreover, the buffer once made, can be stored for a few months.

The new process is used for diffusing Cd/Zn in a quarter of a two inch diameter InGaAs/InP wafer. The same trough can be used for a two inch diameter wafer. Even larger diameter wafers can be used in a trough with larger surface area and depth.

The usefulness of this new technique is demonstrated with the fabrication of JFETs and PIN photodetectors. In both cases, the junction breakdown voltages are lower than those obtained with conventional diffusion. It was conjectured in Chapter 3 that this is due to stresses of the SiN mask. A new mask set is required to use the mask-less diffusion for improving junction breakdown characteristics.

Patterned diffusion without presence of mask during diffusion is possible with LB film through lift-off. Elimination of mask for patterned diffusion can result into better junction breakdown characteristics.

The impurities in diffusion sources are known to adversely affect material properties such as minority carrier life time. As indicated by the Auger spectra of the oxyplasma processed LB film, carbon is not completely removed from the LB film and some residues are left on semiconductor surface. Apparently, the hydrocarbon residues from the LB film do not seem to alter p-n junction characteristics. Long term effects of residual hydrocarbons on electrical characteristics of the p-n junction are not known and require further study.

APPENDIX

Standard Processes For III-V Compound Semiconductors

Processes used frequently during the course of this research work at the Navesink facility of Bellcore are described in this chapter. Contrary to what the title of this chapter may suggest, these are not the semiconductor industry standards but the standard for this particular research project only. During this research work, these processes have been tried as much as possible and exceptions are mentioned explicitly. These processes can be catagorized into two main groups: deposition and etching. Deposition includes dielectric mask deposition and contact metallization. Etching includes dry and wet chemical etching of semiconductors as well as dielectrics.

A1 Deposition Of Dielectrics and Contact Metallizations

Dielectric deposition includes silicon dioxide and silicon nitride deposition using a system of Plasma-Therm, Inc., model no. PD-2411. This technique is commonly referred to as PECVD. The substrates must be cleaned to remove surface contaminants and blow dried with dry nitrogen prior to insertion in the deposition chamber.

A1.1.1 PECVD of Silicon Dioxide

Typical deposition conditions were:

Gases: SiH_4 , N_2O, Ar
Gas flow rates: SiH_4; 160 sccm, N_2O ; 90 sccm, Ar; 680 sccm
Reaction chamber pressure: 200 m torr
Substrate temperature: 300°C
RF power: 30 W
Deposition rate: ~5-6 nm/min

A1.1.2 PECVD of Silicon Nitride

Typical deposition conditions for PECVD of silicon nitride were:
Gases: SiH_4 , NH_3 , Ar
Gas flow rates: SiH_4 ; 170 sccm, NH_3 ; 620 sccm, Ar; 970 sccm
Reaction chamber pressure: 350 m torr
RF power: 30 W
Substrate temperature: 300°C
Deposition rate: ~1.5-2.5 nm/min

A1.2 Contact Metallization

Three different types of most frequently used metal contacts and their fabrication techniques are described below. Semiconductor substrate is etched in 1 NH_4OH : 10 H_2O prior to insertion into electron beam evaporator for removing native oxide from its surface. This is necessary for consistently reproducing ohmic contacts with low contact resistance R_C .

A1.2.1 Ohmic Contacts for n-type GaAs, InGaAs and InP

A n-type contact includes: electron beam evaporation of 5 nm Ni/ 35 nm Ge/ 50 nm Au/ 30 nm Ni/ 130 nm Au and annealing at 420°C under flowing argon in a rapid thermal annealer for 20 seconds.

A1.2.2 Ohmic Contacts for p-type GaAs, InGaAs and InP

An ohmic contact to the p-type semiconductor is made by electron beam evaporation of 5 nm Cr/ 80 nm AuBe/ 120 nm Au and annealing at 420°C under flowing argon in a rapid thermal annealer for 20 seconds.

A1.2.3 Schottky Contact

This contact metal is used to form a Schottky barrier diode at the gate-channel interface of an FET. All the MESFETs and HEMTs described in this thesis had Ti/Au Schottky gates formed by electron beam evaporation of 15 nm Ti and 135 nm Au.

A2 Dry and Wet Etching of Dielectrics and Semiconductors

Three different techniques, namely, ion beam assisted etching (commonly referred to as ion milling), reactive ion etching (RIE) and plasma etching were used. Ion milling was used for non selective etching of GaAs, AlGaAs, InGaAs, and InP. Spin-on glass was etched using RIE. Plasma etching was used for selective etching of silicon nitride with photoresist mask. Typical parameters for all three are listed below.

A2.1.1 Ion Milling

Equipment: Veeco ion miller model 6" Microetch Ion beam milling system
Gas ambient: Ar
Gas pressure: 2×10^{-4} torr
Acceleration voltage: 500 V
Ion beam current: 0.25 mA/ cm^2
Milling rate: ~50 nm/min for most semiconductors, ~20-25 nm/min for SiO_2

A2.1.2 Reactive Ion Etching

Reactive gas: C_2F_6
Chamber pressure: 30 m torr
Gas flow rate: 5 sccm
RF power: 100 W
Etch rate: ~70 nm/min for SOG baked at 130°C, ~28-40 nm/min for SOG treated in oxyplasma for 60 min.

A2.1.3 Plasma Etching of Silicon Nitride

A Technics planar etcher model PEII-A was used for selective etching of silicon nitride with photoresist mask.

Reactive gas: 4% CF_4 in O_2
Chamber pressure: 280 m torr
Power: 50 W
Etch rate: 100 nm/min

A2.1.4 Oxygen Plasma Treatment of LB Film

This is also referred to as 'oxyplasma' treatment. A Technics planar etcher model PEII-A was used with O_2 gas pressure of 280 m torr and 50 W power for removing organic part of the LB films. Oxyplasma treatment of two to three minutes is sufficient for removing most of the hydrocarbons from 8-14 monolayers of LB film.

A2.2 Wet Chemical Etching

Many different etchants are popular for wet chemical etching of GaAs, InGaAs and InP but the ones described below were used for this work.

A2.2.1 GaAs, AlGaAs Etchant

Etchant composition by volume: 1 H_2SO_4 : 8 H_2O_2 : 500 H_2O
Temperature: Room temperature
Etch rate: ~100-120 nm/min
Comments: No selectivity between GaAs and AlGaAs. Does not work well in presence of native oxide on semiconductor surface.

A2.2.2 InGaAs and GaAs Etchant

Etchant composition by volume: 1 H_3PO_4 : 1 H_2O_2 : 38 H_2O
Temperature: Room temperature
Etch rate: ~100-120 nm/min
Comments: Etches InGaAs selectively from InP. It also etches GaAs and AlGaAs at almost same rate.

A2.2.3 InP Etchant

Etchant composition by volume: 1 HCl : 10 H_3PO_4
Temperature: Room temperature
Etch rate: 100 nm/min
Comments: Etches InP selectively from InGaAs.

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