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Design, fabrication and characterization of silicon microlenses for IR-CCD image sensors

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ABSTRACT

DESIGN, FABRICATION AND CHARACTERIZATION OF SILICON MICROLENSES FOR IR-CCD IMAGE SENSORS

by
Dhiren K. Pattnaik

There is a growing trend in the study of Focal Plane Arrays(FPAs) of very small microlenses, used for a wide variety of imaging and sensing applications, to increase optical efficiency. Present day sensor technology might take a different direction altogether with the development of compact, high quality, high resolution imaging microlenses, which could make the fill factor >90%. A method to increase light sensitivity of Interline Transfer(IT) type image sensors is to position microlens FPAs on top of the image sensors. FPAs are structures of small lenses which focus the incoming light on the photo sensitive part of the image sensor. The objective of this thesis was to develop reliable and efficient microlens FPAs for a 320 X 244 element PtSi-IT infrared image sensor. The proposed FPAs overcome the difficulty most commonly faced with IT image sensors i.e. low light sensitivity, and in fact makes it superior in light sensitivity to Frame Transfer/Frame Interline Transfer types of image sensors. We have introduced additional degrees of freedom into surface profile of microlens. ZEMAX tool was deployed to model, analyze and assist in the design of the lenses. Standard IC processes were applied to fabricate the lenses with a strict control over process parameters. As a result, we have fabricated prototype microlenses which are expected to assist in obtaining the high sensitivity level of the sensor.

DESIGN, FABRICATION AND CHARACTERIZATION OF SILICON MICROLENSES FOR IR-CCD IMAGE SENSORS

by
Dhiren K. Pattnaik

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Dedicated to
My Beloved Family

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CHAPTER 1

INTRODUCTION

In the past decade, micro-optics technology has evolved through three generations: the first is characterized by slow diffractive micro-optics; the second by fast microlens arrays; and the third by integrated layers of micro optics and photonic devices. The first generation optical elements have large periods(hundreds of microns); the second and third generation have submicron zone widths. The first generation hybrid diffractive/refractive technology, primarily used to correct aberrations in large aperture refractive optics, has bee adopted by many industrial, federal and defense organizations. The second generation consists of efficient microlens arrays comprised of large numbers ($> 10^5$) of identical elements used in such diverse applications as focal plane arrays, laser beam addition and IR sensors. The ultimate potential of these micro-optics arrays awaits the fruition of third generation binary optics technology-a new architecture that integrates multiple planes of optics and electronics[1-3].

Optical systems of the twenty-first century will employ hybrid and integrated diffractive optical elements to effect lightweight, compact designs. This requires the optics industry to adopt new manufacturing paradigm- i.e., to design electro-optics systems in totality and to implement the new fabrication techniques necessary to make novel optical components. Micro-optics technology adapts the complexities of integrated circuit manufacturing technology, i.e., CAD/CAM optics tools and design packages coupled with sophisticated and mature VLSI microstructure fabrication techniques to make both diffractive and refractive microlenses. By sharing a common base with

microelectronics, photonics and micromachining communities, manufacturing costs are reduced and integration of these technologies is simplified. From its inception, micro-optics technology has been driven by demand for fast broad-band flat optics needed for low cost smart sensors. High functionality micro optical elements streamline the optical train and simplify system assembly[2,3].

The aim of this thesis was to design, fabricate and characterize microlens array for use in IR image sensors and to study the suitability for monolithic integration of lens array with sensor circuitry. The investigation of the various aspects of lenses have been discussed in the next six chapters. In chapter 2, the background for lens applicability has been summarized. This discussion heavily relies on the data available in the literature. In chapter 3, basic operation of CCD arrays has been discussed, which strengthens the case for microlenses. In Chapter 4, the need for lenses is discussed. In chapter 5, various present day techniques for fabrication of microlenses have been summarized. Chapter 6 elaborates in detail about various methods adopted to design, fabricate and characterize the microlenses. At the end of chapter 6, the results are summarized. In chapter 7, various issues relating to future work are identified. Conclusions and recommendations based on these studies are presented in chapter 8.

CHAPTER 2

BACKGROUND

IR detectors, which operate by converting the thermal radiation into electrical signal, are key to performance of many optical/infrared systems. The light sensitivity(capacity to convert incoming light into an electrical signal) is an important aspect of a sensor. To achieve improved light sensitivity and to increase the detectivity of the detector, microlenses need to be used to focus the incident radiation on to the active area of the detector[4,5].

There are various types of solid-state image sensors. The most commonly used are interline transfer(IT) sensors, frame transfer(FT) sensors and frame interline transfer(FIT) sensors. Fine pattern processing makes it possible to shrink the pixel sizes. With reduction in pixel size, the aperture size of the light shield and channel stop region become so small that its low sensitivity and larger smear values become major problems for CCD image sensors[6]. The light sensitivity of IT and FIT image sensors is lower than that of FT image sensors. One method to increase the light sensitivity is to use microlenses on top of the image sensor. Microlenses are small lenses which are positioned in arrays on top of the image sensors and focus the incoming light on the photosensitive parts of the image pixels. Most manufacturers of IT and FIT image sensors compensate for the lower light sensitivity by using microlenses. Until now, however, IT image sensors have not been equipped with them. As a result of ongoing miniaturization in the industry, the light sensitivity of these sensors has decreased. A detailed analysis of the literature suggests that IT image sensors combined with microlenses have more light

sensitivity than traditional FT/FIT image sensors. Preliminary calculations suggest an improvement of about 68% light efficiency with the use of microlenses. However, detailed calculation shows that there is a potential of >90% optical efficiency. Microlenses can be used to create an erect 1:1 image of the scanned document on the image sensor without requiring intimate contact between the two, thus avoiding electro-static and mechanical damage to the array[51].

Therefore, research on the use of microlenses on IT image sensors becomes important. In this thesis, a detailed investigation on the technical feasibility of microlens FPAs on IT image sensors has been performed.

CHAPTER 3

OPERATION OF CCD ARRAYS

3.1 Introduction

Charged-coupled devices were invented by Boyle and Smith in 1970. Since then considerable work has been done to improve the fabrication and operation of CCDs. However the CCD arrays do not create an image by themselves. A CCD array requires an optical system to image the scene on to the array's photo sensitive area. Apart from this, the array requires a bias and clock signal. Its output is a series of analog pulses that represent the scene intensity at a series of discrete locations.

CCDs may be described functionally according to their architecture (frame transfer, interline transfer, etc.) or by application. Certain architectures lend themselves to specific applications. For example, astronomical cameras typically use full frame arrays whereas consumer video systems use interline transfer devices.

The heart of the solid state camera is the CCD array. It provides the light intensity as measurable voltage signals[7]. Here, microlenses play a crucial role to portray the real image on to the CCD array without loss of information. With appropriate timing signals, the terminal voltage signals represent spatial light intensities. When the array output is amplified and formatted into a standard video format, a CCD camera is created. The array specifications are only part of the overall system performance. The system image quality depends on the performance of all the components. Array specifications, capabilities and limitations are the basis for the camera specification.

A camera is of no value by itself. Its value is only known when an image is evaluated. The camera output may be directly displayed on a monitor, stored on video tape or disk for later viewing or processed by a computer. The computer may be part of the machine vision system or be used to enhance the imagery or used to create hard copies of the imagery. Effective design and analysis of the opto-electronic devices such as CCDs require an orderly integration of diverse technologies and languages associated with radiation physics, optics, solid state sensors, electronic circuitry, human interpretation of displayed imagery(human factor), computer models and image processing algorithms. Each field is a complex and a separate discipline.

3.2 Charge Coupled Devices(CCDs)

CCD refers to a semiconductor architecture in which charge is read out of storage areas. The CCD architecture has three basic functions: (a) charge collection, (b) charge transfer, and (c) the conversion of charge into measurable voltage. The basic building block of the CCD is the Metal-Oxide-semiconductor (MOS) capacitor. The capacitor is called a gate. By manipulating the gate voltages, charge can either be stored or transferred. Charge generation in most CCDs occur in a MOS capacitor(also called a photo gate). For some devices(notably interline transfer devices)photo diodes create the charge. After charge generation, the transfer occurs in the MOS capacitor for all CCDs. Since most sensors operating in the visible range use a CCD type architecture to read the signal, they are popularly called CCD cameras. For these devices, charge generation is often considered as the initial function of the CCD. More explicitly, these cameras should called be solid state cameras with a CCD readout.

CCDs and detectors can be integrated either monolithically or as hybrids. Monolithic arrays combine the detector and CCD structure on a single chip. The most common detectors are sensitive in the visible region of the spectrum. They use silicon photo gates or photo diodes and are monolithic devices. CCDs have been successfully used for infrared detectors such as Schottky Barrier Devices(SBD) that are sensitive in the 1.2 μm to 5 μm radiation. Hybrid arrays avoid some pitfalls associated with the growth of different materials on a single chip and provide a convenient bridge between well-developed but otherwise incompatible technologies.

3.3 Image Quality

Image quality is a subjective impression ranking of imagery from poor to excellent. The relationships are many and not well understood. Seeing varies between individuals and over time, in an individual. There exists large variations in the observer's judgment so as to the correct rank ordering from best to worst and therefore image quality cannot be placed on an absolute scale.

Many formulae exist for predicting image quality[9-12]. Each is appropriate under a particular condition. These expressions are typically obtained from empirical data in which multiple observers view many images with a known amount of degradation. The observers rank-order the imagery from worst-to-best and then an equation is derived that relates the ranking scale to the amount of degradation.

Early metrics were created for film based cameras. Image quality was related to the camera lens and film modulation transfer functions(MTFs). MTF is the primary

parameter used for optical system design, analysis and specifications. It is represented by positive values. In simple words, MTF is a measure of how well the system will faithfully reproduce the scene. MTF is defined as the ratio of output modulation to input modulation normalized to unity at zero spatial frequency.

$$\text{MTF} = \text{Output Modulation/Input Modulation}$$

where

$$\text{Modulation= M= } (V_{max}-V_{min})/ (V_{max}+V_{min})$$

Here V_{max} and V_{min} are the maximum and the minimum signal levels respectively[13]. With the advent of better imaging circuits, image quality centered on the perception of raster lines and the minimum SNR (signal-to-noise ratio) required for good imagery. Many tests have provided insight into the image metrics that are related to image quality. Most metrics are related to the system MTF, resolution or the SNR. In general, images with higher MTFs and less noise are judged as having better image quality. There is no single ideal MTF shape that provides best image quality.

In a CCD camera system, the lens, array architecture, array noise, and display characteristics affect system performance. Only an end-to-end assessment of the entire system will determine the overall image quality.

Electro-optical imaging system analysis is a mathematical construction that provides an optimum design through appropriate trade-off analysis[15]. A comprehensive model includes the target, optical system, detector, display and interpretation. Any of these parameters can be studied separately but not in an the electro-optical imaging

system Only a complete end-to-end analysis(scene-to-observer interpretation) permits system optimization.

The system MTF is the major component of the system analysis. It describes the propagation of sinusoidal patterns through the system. Since any target can be decomposed into Fourier series, the MTF approach indicates quality of image on display. The sensor resolution is limited by lens focal length, pixel size, and detector center-to-center spacing(also called detector pitch or pixel pitch). Any image processing algorithm must take into account the sensor resolution.

3.4 CCD Arrays

CCD(Charged couple device) refers to a semiconductor architecture in which charge is transferred through storage areas. Since most sensors operating in the visible region use a CCD architecture to move a charge packet, they are popularly called as CCD arrays. The CCD architecture has three basic functions: (a) Charge collection (b) Charge transfer and (c) The conversion of charge into a measurable voltage. Since arrays operating in the visible are monolithic devices, charge generation is often considered as the initial function of the CCD. The charge is created at a pixel site in proportion to the incident light level present. The aggregate effect of all pixels is to produce a spatially sampled representation of the continuous scene.

The basic building block of the CCD is the metal-oxide-semiconductor(MOS) capacitor. The capacitor is called a gate. Charge packets are sequentially transferred form capacitor to capacitor until they are measured on the sense node. Charge generation in most devices occur in a MOS capacitor(also called a photo gate). For some

devices(notably interline transfer devices) photo diodes create the charge. After charge generation, the transfer occurs in the MOS capacitor for all devices.

With silicon photodiodes arrays, each absorbed photon creates an electron-hole pair. Either the electrons or holes can be stored and transferred. In the present architecture, electrons are collected and transferred. An identical process exists for CCD arrays, in which holes are collected and stored. The charge transfer physics is the same for all CCD arrays. However the number of phases and number and location of the serial shift readout registers vary. Although CCD arrays are common place, the IR-CCD fabrication is quite complex. The fabrication process might vary from minimum 29 steps procedure to 150 different operations. The complexity depends on the array architecture.

3.5 CCD Operation

The basic building block of the CCD is the metal-oxide-semiconductor(MOS) capacitor. Applying a positive voltage to the gate causes the mobile positive holes in the p-type silicon to migrate towards the ground electrode, since like charges repel. This region, which is void of positive charge, is the depletion region. If a photon whose energy is greater than the energy gap is absorbed in the depletion region, it produces an electron-hole pair. The electron stays within the depletion region whereas the hole moves to the ground electrode[15-18]. The amount of negative charge (electrons) that can be collected is proportional to the applied voltage, oxide thickness and gate electrode area. The total number of electrons that can be stored is called the well capacity (Fig. 3.1).

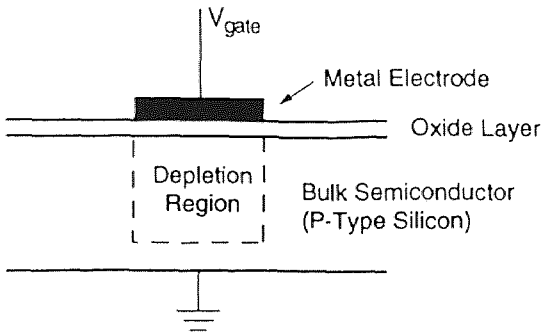


Figure 3.1 Metal-Oxide-Semiconductor(MOS) gate for p-type silicon

As the wavelength of the incident photon increases, they are absorbed at increasing depths. Very long wavelength photons may pass through the CCD and never be absorbed. A photoelectron generated deep within the substrate will experience a three dimensional random walk until it recombines or reaches the edge of a depletion region where the electric field exists. If the diffusion length is zero then the electron hole pair generated in the substrate combines immediately[20]. This limits the long wavelength response. If the diffusion length is extremely large, then all the electrons will eventually migrate to a charge well. Doping alters the diffusion length.

CCD register consists of a series of gates. Manipulation of the gate voltage in a systematic and sequential manner transfers the electrons from one gate to the next in a conveyor-belt-like fashion. For charge transfer, the deletion region must overlap (Fig. 3.2). The depletion regions are actually charge gradients and the gradients must overlap for charge transfer to occur.

Each gate has its own control voltage that is varied as a function of time. The voltage is a square wave and is a called clock or clocking signal. When the gate voltage is

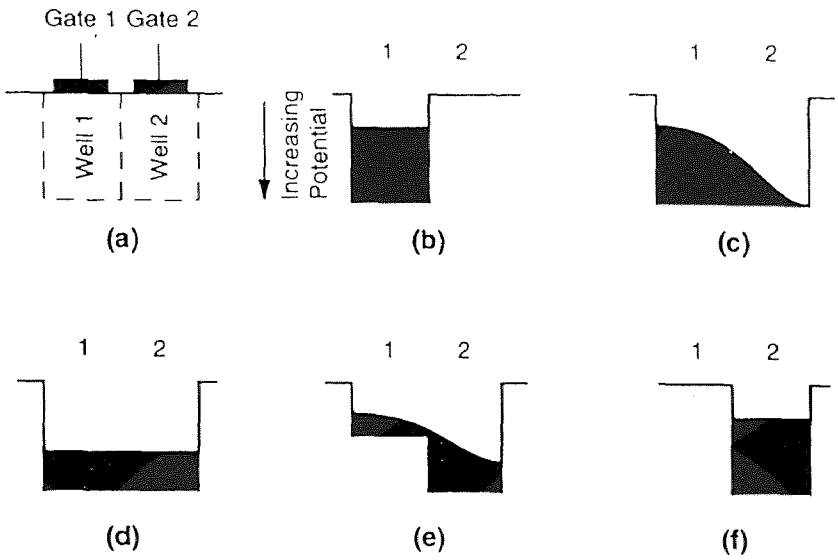


Figure 3.2 Charge transfer between two wells. (a) Adjacent wells. (b) Charge in well 1. (c) After voltage is applied to gate 2, electrons flow into well 2. (d) Equilibration of charge. (e) Reduction of gate 1 voltage causes the electrode well 1 electrons to fully transfer into well 2. (f) All electrons have been transferred into well 2.

low, it acts as a barrier whereas when the voltage is high, charge can be stored. Initially a voltage is applied to gate 1 and photo electrons are collected in well 1(Fig. 3.2b). When voltage is applied to gate 2, electrons move to well 2 in a waterfall manner(Fig. 3.2c). This process is rapid and the charge quickly equilibrates in two wells(Fig. 3.2d). As the voltage is reduced in gate 1,. well potential decreases and electrons again flow in waterfall manner into well 2. Finally when gate 1 voltage reaches zero, all the electrons are in well 2(Fig. 3.2f). This process is repeated many times until the charge is transferred through the shift register.

The CCD array is a series of column registers(Fig. 3.3). The charge is kept within rows or columns by channel stops or channel blocks and the depletion region overlaps in one direction only. At the end of each column is a horizontal register of pixels. This

register collects a line at a time and then transports the charge packets in a serial fashion to an output amplifier. The entire horizontal serial register must be clocked out to

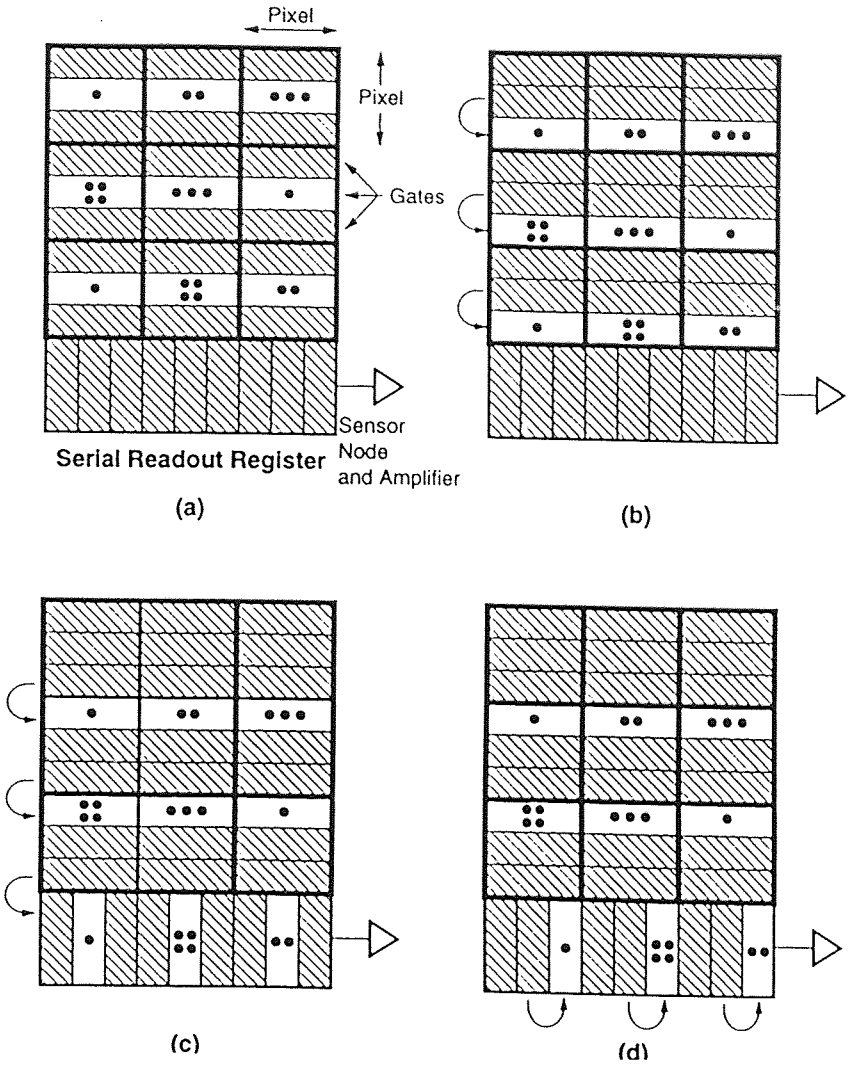


Figure 3.3 Representative CCD operation of 3x3 array with three gates per pixel. Nearly all the photoelectrons generated within the pixel are stored in the well beneath that pixel. (a) The CCD is exposed to light and an electron image is created. (b) The columns are shifted down in parallel, one gate at a time. (c) Once in the serial row register, the pixels are shifted right to the output node. (d) The entire register must be clocked out before the next packet can be transferred into the serial readout register.

the sense node before the next line enters the serial register. Therefore separate horizontal and vertical clocks are required for all arrays.

Interaction between many thousands of transfers reduces the output signal. The ability to transfer charge is specified by the charge transfer efficiency(CTE). Although any number of transfer sites(gates) per detector area can be used, it generally varies from two to four. The well potential depends on the oxide thickness underneath the gate. In Fig. 3.4, the alternating gates have different oxide thickness and therefore will create different well potentials. With different potentials, it is possible to create a two-phase device. Charge will preferentially move to the right hand side of the pixel where the oxide layer is thinner. Assuming that initially the wells controlled by V_2 are empty(this will occur after a few clock pulses) at time t_1, both clocks are low. When V_2 is raised, the potential increases as shown at time t_2. Since the effective potential increases across the gates, the charge cascades down to highest potential. V_2 is then dropped to zero and the charge is contained in the V_2 gate at time t_3. This process is repeated until the charge is clicked off the array. The voltage timing is shown in Fig 3.5. While Fig. 3.4 illustrates the variation in the oxide layer, the potential wells can also be manipulated through ion implantation. This can also be operated in anti-parallel mode: V_2 is a mirror image of V_1. That is when V_1 is high V_2 is low.

The virtual phase device requires only one clock (Fig 3.6). Additional charge wells are created by internally biased gates. Charge is stored either beneath the active gate or the virtual gate. When V_1 is low, charge will cascade down to the highest potential(which is beneath the virtual well). When V_1 is applied at t_2, the active potential increases the charge moved to the active gate well.

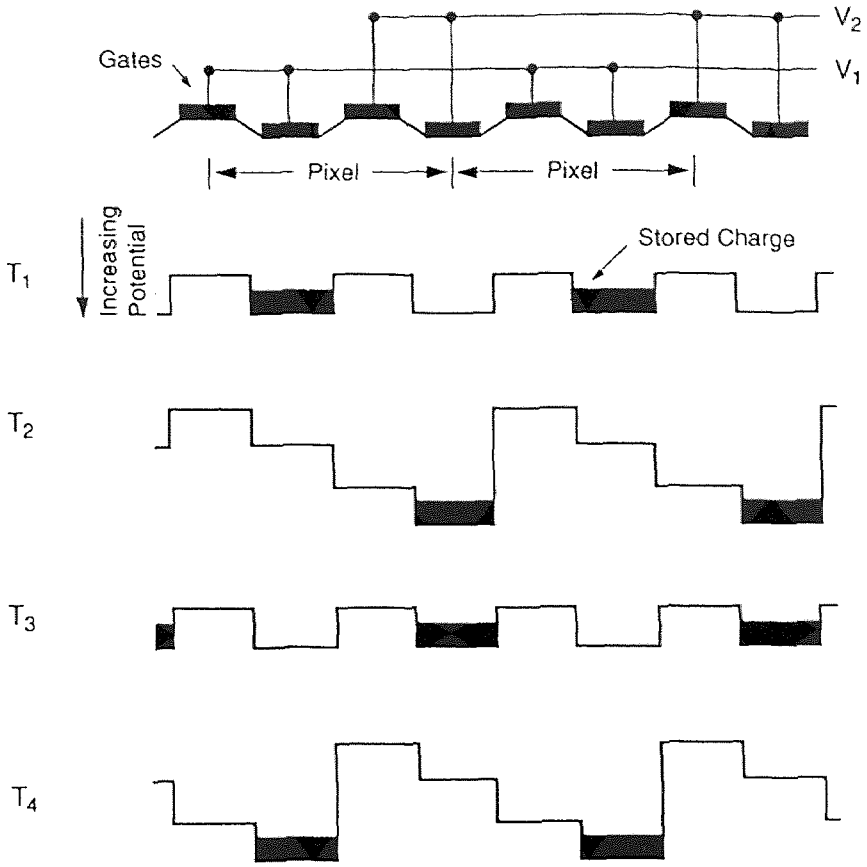


Figure 3.4 Charge transfer in a two-phase device. Well potential depends on the oxide thickness.

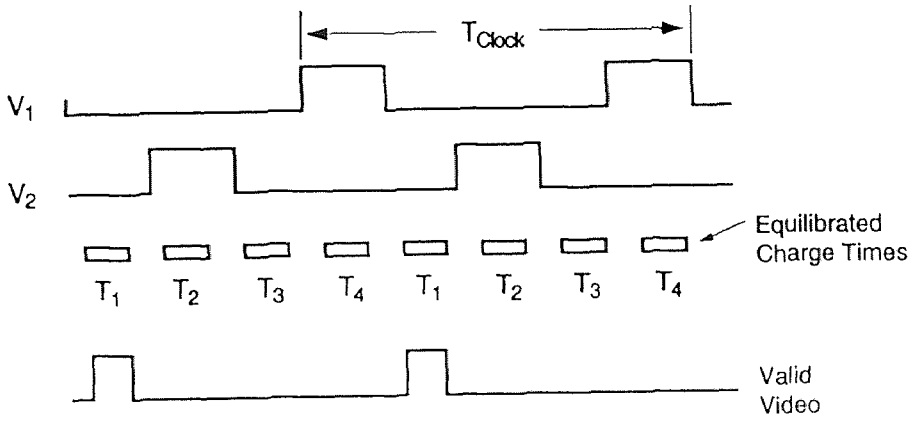


Figure 3.5 Voltage levels for two-phase systems

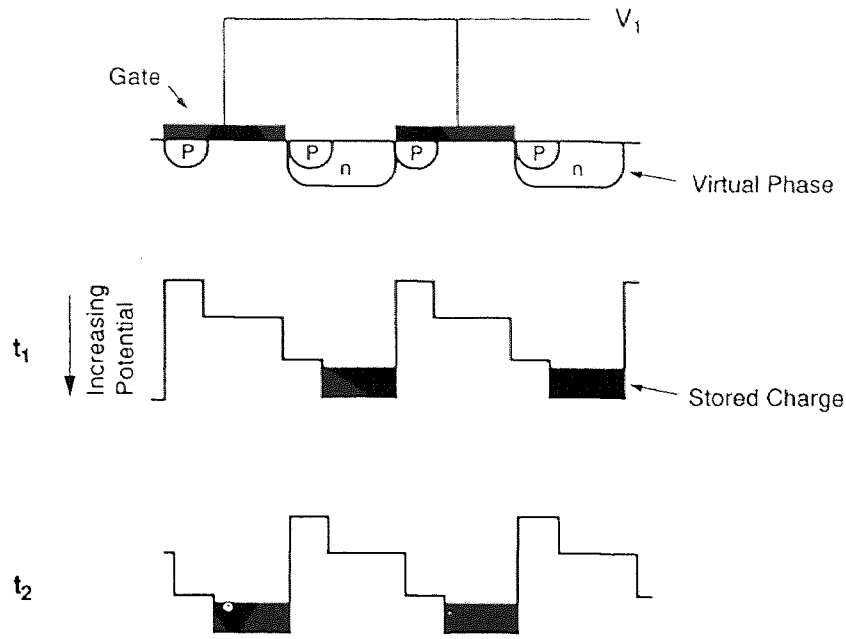


Figure 3.6 Charge in a device with a virtual phase. The virtual well is created by p- and n- material implants. These ions create a fixed bias and therefore a well with a fixed potential. By changing V_1, the active gate potential can be lower than the virtual well (t_1) or higher (t_2). This represents one column. Rows go into the paper.

The final operating step is to convert the charge packet to measurable voltage. It is accomplished by a floating diode or floating diffusion. The diode acting as a capacitor creates a voltage proportional to the number of electrons n_e. The output voltage is sensed by a source follower and is

$$V_{SIGNAL} = N_e \; Gq/C$$

The gain G of a source follower amplifier is approximately one, q is the electronic charge and is equal to 1.6 X 10^{-19} C. The signal is then amplified, processed and digitally encoded. With many arrays, it is possible to shift more than one row of charge into the serial register. Similarly it is possible to shift more than one serial register element into a

summing gate just before the output node. This is called charge grouping, binning, super pixeling, or charge aggregation. Binning increases signal output and dynamic range at the expense of spatial resolution. Because it increases signal-to-noise ratio, binning is useful for low light level conditions in those cases where resolution is less important. Serial registers and the output node require larger capacity charge wells for binning operation. If the output capacitor is not reset after every pixel, then it can accumulate charge.

3.6 Array Architecture

Based on its application, array architecture is selected.

(i) Full frame and frame transfer devices tend to be used for scientific applications.

(ii) Interline transfer devices are used in consumer camcorders and professional television systems.

(iii) Linear arrays, Progressive scan and Time-delay and integration (TDI) are used for industrial applications.

For present purposes only Interline Transfer(IT) type of sensors will be discussed.

3.7 Interline Transfer

The Interline Transfer(IT) array consists of photo diodes separated by vertical transfer registers that are covered by an opaque metal shield(Fig. 3.7). After integration, the charge generated by the photodiodes is transferred to the vertical CCD registers in about 1μs and smear is minimized. The main advantage of interline transfer is that the transfer from the active sensor to the shield storage is quick. There is no need to shutter the

incoming light. This is commonly called electronic shuttering. The disadvantage is that it leaves less real estate for the active sensors. The shield acts like a Venetian blind that obscures half the information that is available in the scene. The area fill factor may be as low as 44%. Since the detector area is only 44% of the pixel area, the output voltage is only 20% of the detector that would completely fill the pixel area. Microlenses increase the optical fill factor.

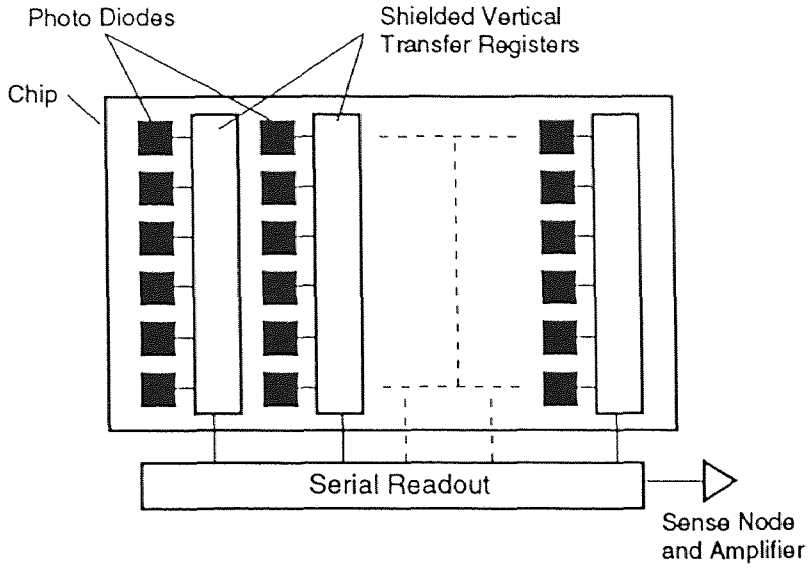


Figure 3.7 Interline transfer architecture. The charge is rapidly transferred to the interline transfer registers. The registers may have three or four gates.

A fraction of the light can leak into the vertical registers. This effect is almost pronounced when viewing an ambient scene that has a bright light in it. For professional television applications, the frame-interline transfer(FIT) array was developed to achieve even lower smear values(Fig 3.8). This can be very well referred from the figures and is

mentioned in subsequent descriptions. The same is also analyzed and performed in a review[21].

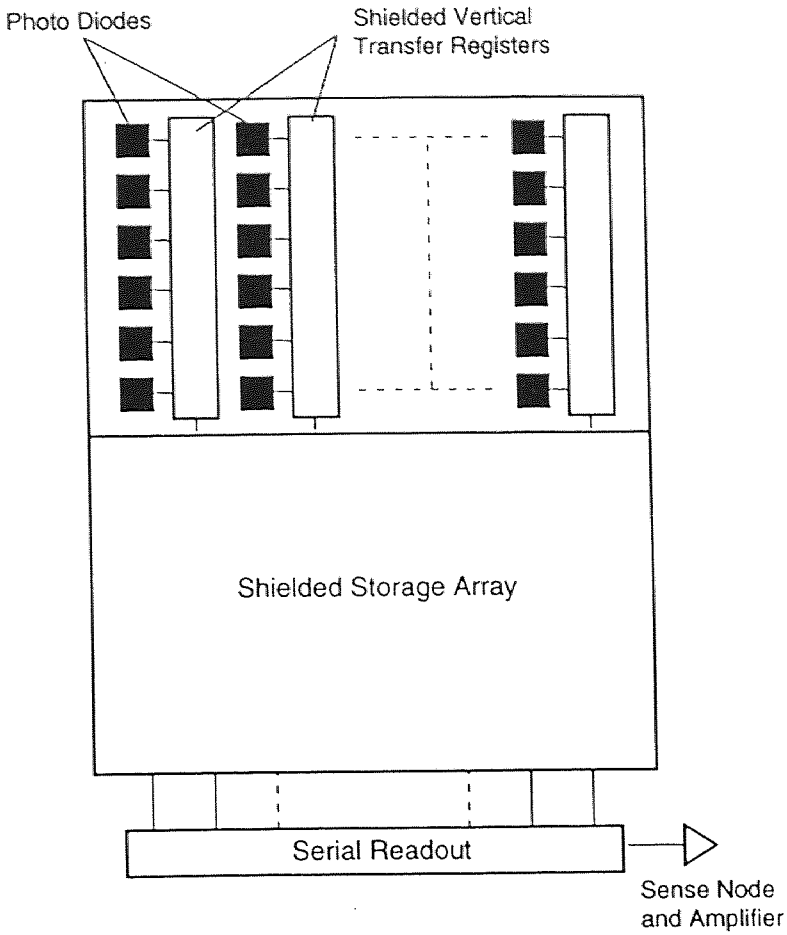


Figure 3.8 Frame-Interline transfer architecture. Both the vertical transfer gate and storage area are covered with an opaque mask to prevent light exposure.

3.8 Dark Current

The CCD output is proportional to the exposure, $L_q(\lambda, T)t_{INT}$. The output can be increased by increasing the integration time and long integration times are generally used

for low-light-level operation. However this approach is ultimately limited by dark current leakage that is integrated along with the photocurrent. The dark current is only appreciable when t_{INT} is long.

A critical design parameter is the dark noise reduction. There are three main sources of dark current: (a) Thermal generation and diffusion in the neutral bulk material, (2) Thermal generation in the depletion region (3) Thermal generation due to surface steps. Dark current due to thermally generated electrons can be reduced by cooling the device. Surface state dark current is minimized with multi phase planning.

3.9 Microlenses

Optical fill factor may be less than 100% due to manufacturing constraints in all transfer devices[24]. In interline devices, the shield storage area reduces the fill factor to even less than 20%. Microlens assemblies(also called microlenticular arrays or lenslet arrays) increase the effective fill factor(Fig. 3.9). But it may not reach 100% due to slight misalignment of the microlens assembly, imperfections in the microlens itself, nonsymmetric shielded areas, and transmission losses. As shown in the camera formula[61], the number of photoelectrons generated in the solid state detector is directly proportional to detector area.

The photosensitive area is below the gate structure and the ability to collect the light depends upon the gate thickness. The cone of light reaching the microlens depends upon the f-number of the primary camera lens. Fig. 3.9 illustrates nearly parallel rays falling on the microlens. This case is encountered with high f-number camera lens

systems. Low f-number primary camera lenses increase the cone angle and the effective fill factor decreases with decreasing f-number. Microlenses are optimized for most practical numbers. As the array size increases, off-axis detectors do not obtain the same benefit as on-axis detectors.

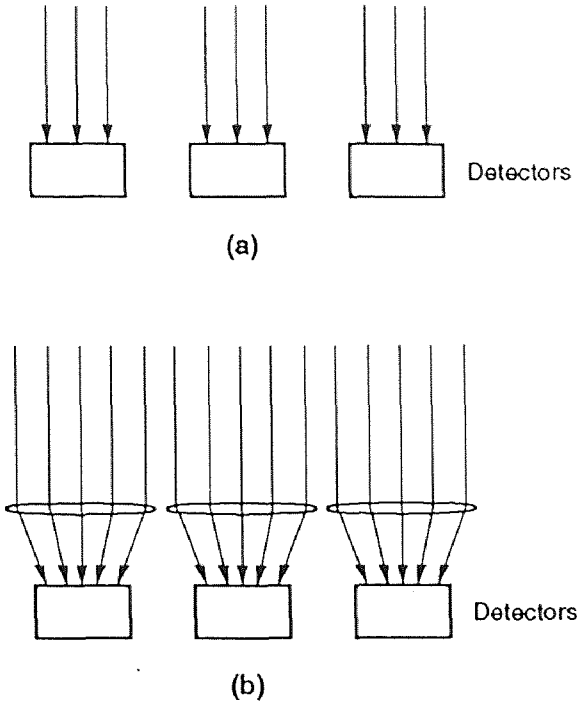


Figure 3.9 Optical effect of a microlens assembly. (a) With no microlens, a significant amount of photon flux is not detected. (b) The microlens assembly can image nearly all the flux on to the detector when a high camera f-number is used. The effectiveness of the microlens decreases as the f-number decreases.

CHAPTER 4

OPERATION OF LENSES

4.1 Introduction

Microlens array has been introduced into CCD image sensor to compensate for the low sensitivity level of the sensor. In order to realize higher density image sensor, we have introduced additional degrees of freedom into surface profile of the microlens[7]. It is important to design microlenses considering the presence of main lens or image lens.

The present 320X244 element PtSi IR-CCD FPA is an interline transfer(IT) imager designed for operation with a readout of two vertically interlaced films per frame. The pixel layout is shown in Fig. 4.1. Each pixel has a size of 40μmX40μm. The Schottky Barrier Diodes(SBDs) are contained on all four sides of polysilicon gates. It leads to detector dimension of 33μmX23μm with a nominal fill factor of 44%. The IR-CCD camera is equipped with an objective lens of F/2.

The nonunity fill factor of IR-CCD FPA results in reduced efficiency. Microlens arrays with the same pitch as the pixels can further concentrate the light, which permits the use of small detector areas. This concentration has a number of advantages such as :

(a) Higher efficiency can be obtained since the fill factor for microlens arrays can generally be made greater than the detector fill factor.

(b) It is possible to have an improved detector-array modulation transfer function resulting from reduced cross talk between detectors. Microlens arrays in front of detector array may be of refractive and diffractive type.

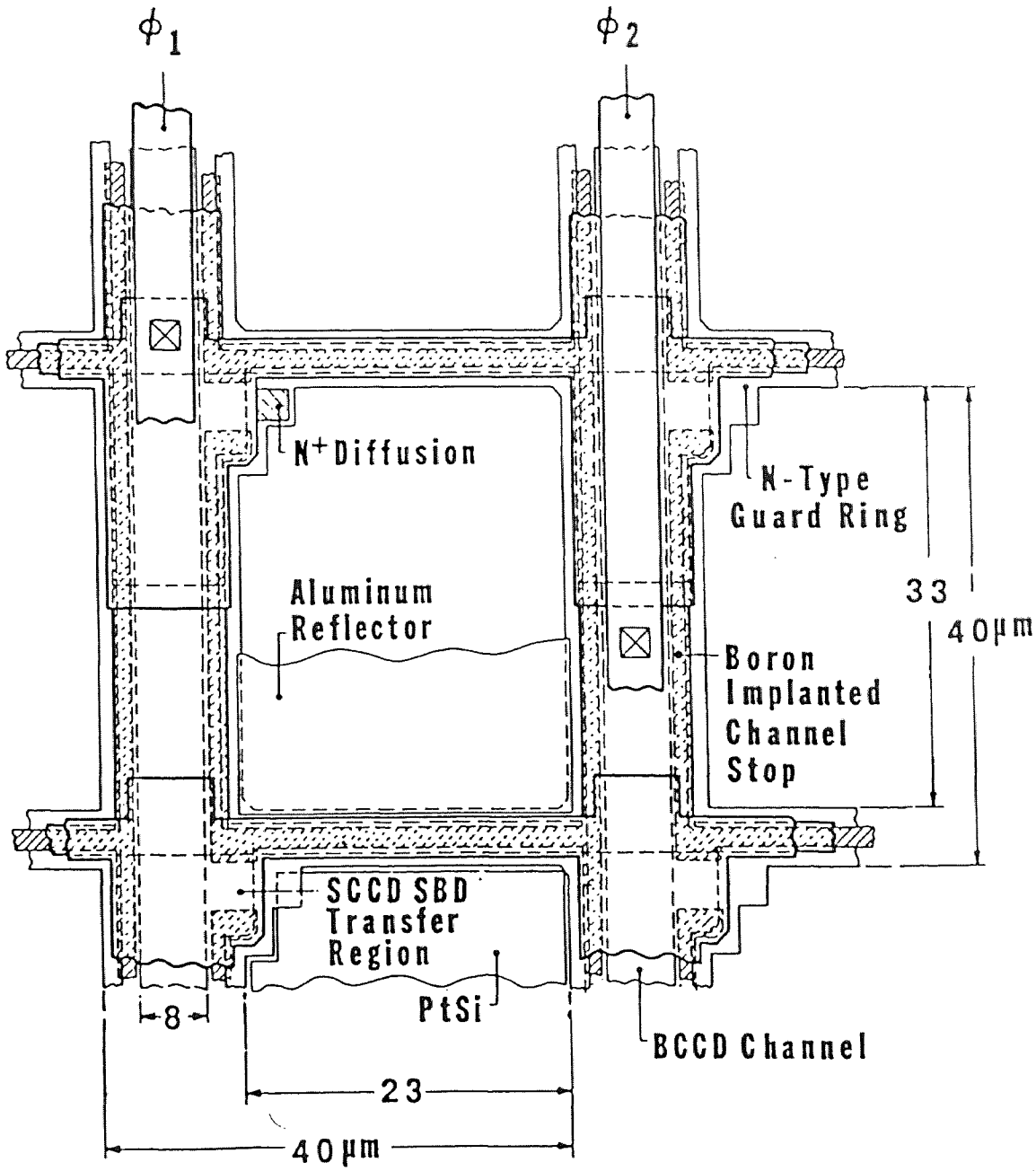


Figure 4.1 Pixel layout of 320x244 FPA

Fig. 4.2 shows an optical schematic of the system considered. The microlens array is located at the nominal focal plane of the optical receiver. Light is incident on the

objective lens which is focused down by the receiver optics to the focal plane where the microlens array is inserted. It then goes through the microlens to the focal plane of the microlens, where the detector array is located. PtSi IR-CCD FPAs are backside illuminated image sensors.

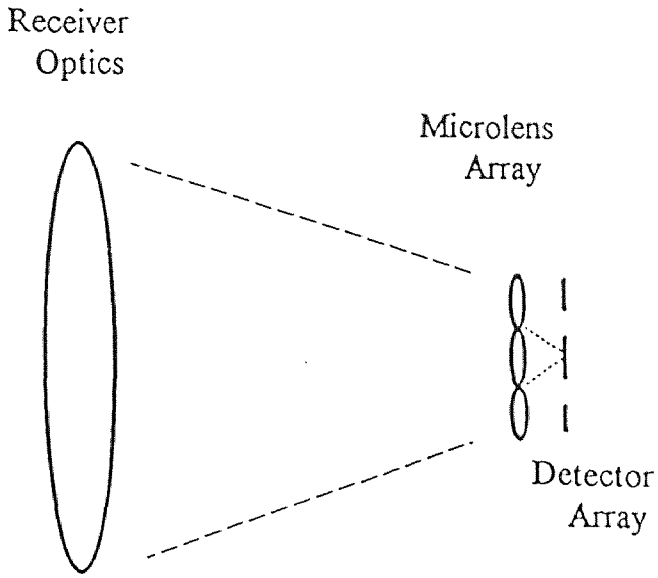


Figure 4.2 Optical schematic of the microlens array placed at the focal plane of the receiver optics and detector array at the focal plane of the microlens array.

Fig. 4.3 shows the cross sectional view of the pixel construction of the sensor. It shows that the PtSi SBDs are surrounded by n-type guard rings, p-type channel stop and transfer gates. Microlenses can be directly fabricated on the backside of the Si wafer, opposite to the PtSi detector and can be made themselves composed as part of the silicon substrate.

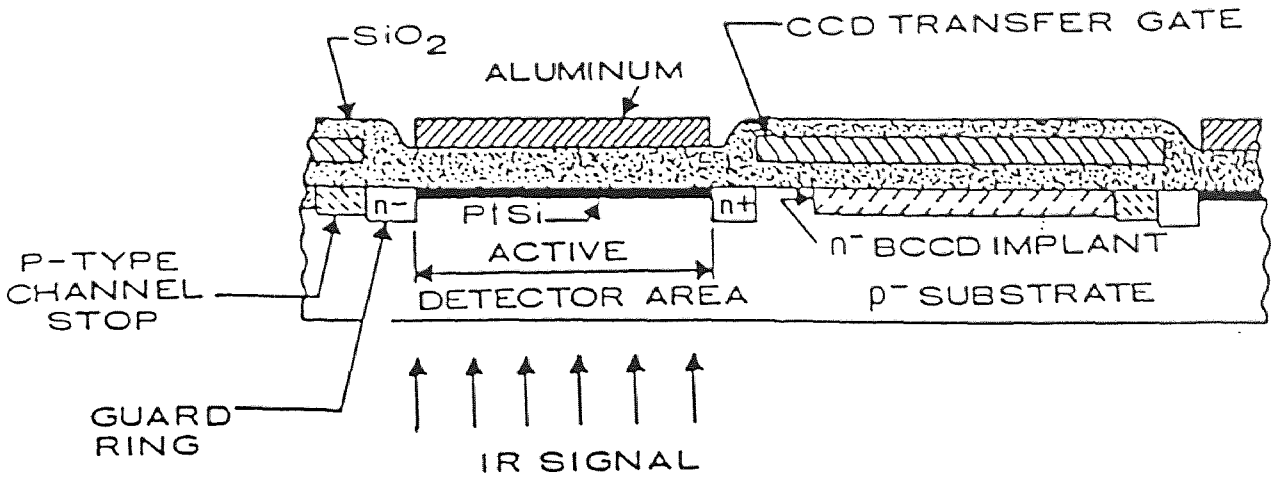


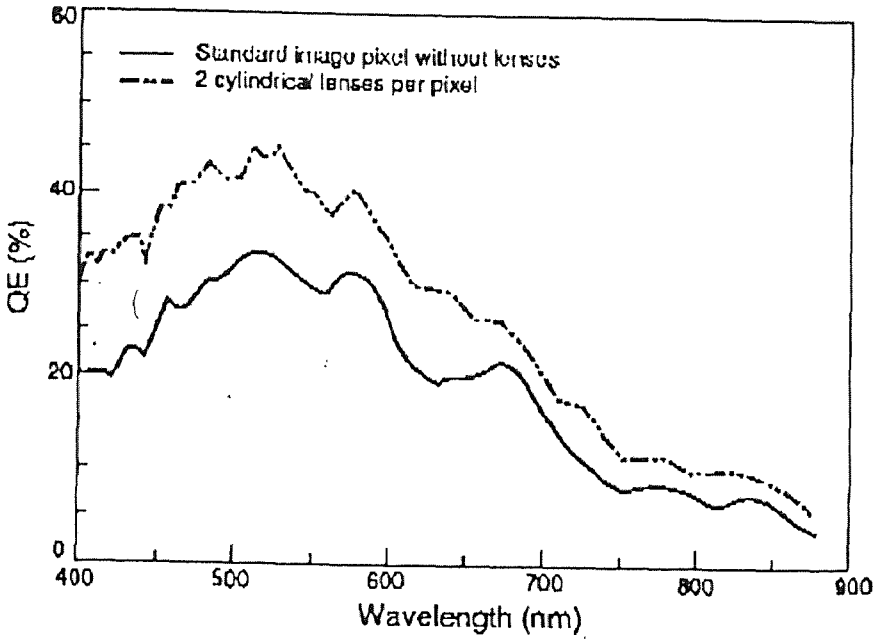
Figure 4.3 Cross-sectional view of the 320x244 pixel

4.2 Spectral Response

Quantum efficiency(QE) is defined as the ratio between the electrons actually collected and the maximum number of electrons which could have been generated by photons impinging on the image sensor (Fig. 4.4.[36]). For an ideal material, when the photon energy is greater than the semiconductor band gap energy, each photon produces one electron-hole pair(quantum efficiency is one). However, the absorption coefficient is wavelength dependent and it decreases for longer wavelength. This means that long wavelength photons are absorbed deeper into the substrate than short wavelengths. Very long wavelength photons may pass through the CCD and may not be absorbed.

Any photon absorbed within the depletion region will yield a quantum efficiency near unity. However, the depletion region size is finite and long wavelength photons will be absorbed within the bulk material. An electron generated within the substrate will

experience a three dimensional random walk until it recombines or reaches the edge of a depletion region where the depletion field exists. If the diffusion length is zero, all electrons created within the bulk material will recombine immediately and the quantum efficiency approaches zero for these wavelengths. As the diffusion length approaches infinity, the electrons eventually reach a charge well and are stored. Here the quantum efficiency approaches one. Doping controls the diffusion length and the quantum efficiency



------- Standard image pixel without lenses
_____ Standard image pixel with lenses

Figure 4.4 Quantum efficiency(QE) of the standard image pixel with and without microlenses

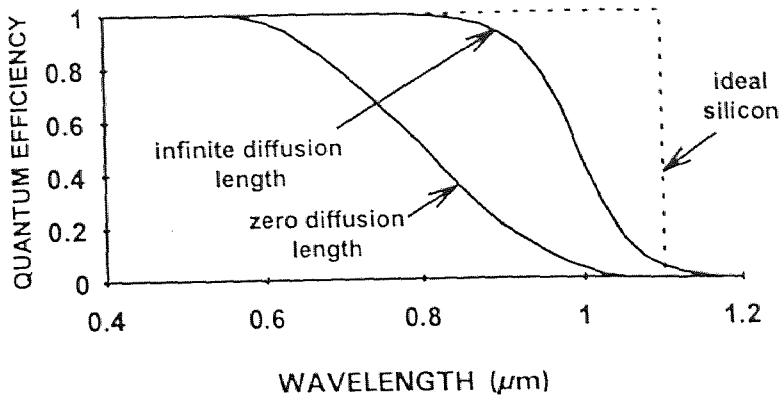


Figure 4.5 The theoretical internal quantum efficiency for silicon photosensors 250 μm thick[61]. The long wavelength quantum efficiency depends upon the thickness of the substrate and the diffusion length. Most arrays have a relatively large diffusion length so that the quantum efficiency tends to be near the infinite diffusion length curve.

is somewhere between these two extremes as shown in Fig. 4.5. The quantum efficiency is dependent upon the gate voltage (low voltage produces small depletion regions) and the material thickness (long wavelength photons will pass through thin substrate).

Illuminating the array from backside (BCCD) avoids the polysilicon problem and increases the quantum efficiency below 0.6 μm as shown in Fig4.6[27]. Photons entering the backside are absorbed in the silicon and diffuse to the depletion region. However, short wavelength photons are absorbed near the surface and these electron-hole pairs recombine before reaching a storage site in a thick wafer. Therefore the wafer is thinned to 10 μm or less to maintain good spectral responsivity (Fig.4.7). In back-side thinned devices, the incident flux does not have to penetrate the polysilicon gate sandwich structure and interference effects are much easier to control.

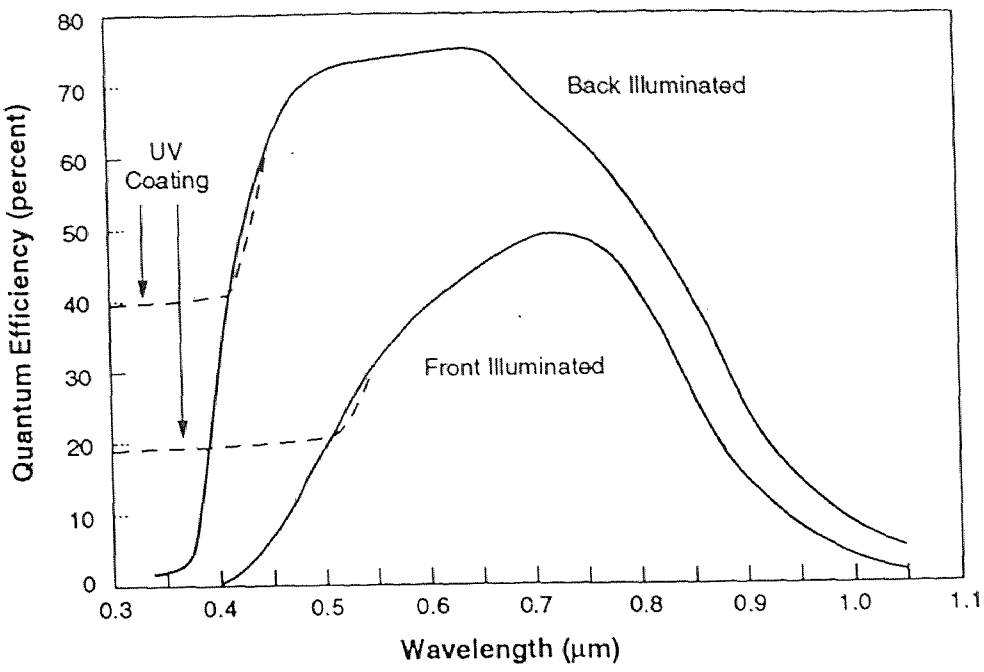


Figure 4.6 Representative spectral response of front-illuminated and back-side illuminated CCD arrays. The spectral response depends upon the process used to manufacture each device.

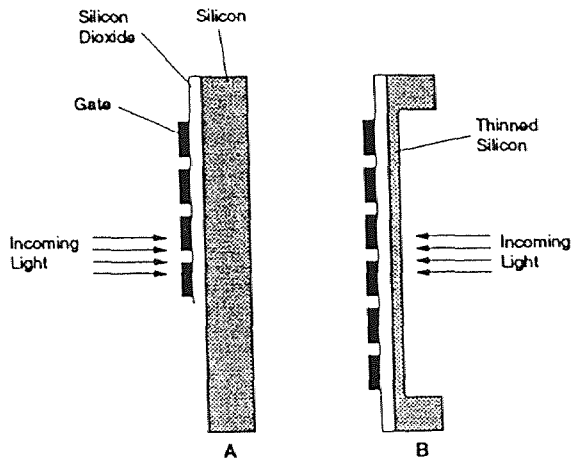


Figure 4.7 (a) Front illuminated and (b) backside illuminated arrays. The thinned backside illuminated array is used for specific scientific applications where high quantum efficiency is required.

With a proper anti-reflection coating, a quantum efficiency of 85 % is possible. Owing to its extremely complex and fragile design, backside illuminated devices are usually limited to scientific applications requiring high quantum efficiency. CCD arrays for consumer and industrial applications are within a sealed environment for protection. Light must pass through a window (lens) to reach the array. In addition to reflection losses at all wavelengths,the glass transmittance decreases for wavelengths below 0.4 μm. So, for scientific applications, requiring high sensitivity, the lenses can be coated with a broad-band anti-reflection coating.

4.3 Reflected Light in Lenses

When light passes form one medium to another medium of different refractive index, as for example from air to silicon, some of it is reflected at the surface and lost. The reflected and the transmitted light obey the basic Fresnel relation for normal incidence:

$$R= (n-1)^2/(n+1)^2$$

where R is the fraction of light reflected from normal incidence on a surface at which the index of refraction changes by n. Thus with silicon having refractive index of 3.5, about 30% of the incident light is reflected, so that a single lens with two surfaces transmits only about 40% of the incident light, ignoring the light absorbed by the silicon as this is small as compared with that lost by reflection[39].

The loss by reflection depends upon the wavelength of light and the angle of incidence. In Fig. 4.8, the middle curve shows the reflected light as a percentage of the

incident light in relation to the angle of incidence, measured from the normal to the surface. This curve is the sum of the upper curve, representing light waves vibrating parallel to the reflecting surface and the lower curve, representing light vibrating perpendicular to the surface. The upper curve increases steadily with the incidence, but the lower drops to zero in reflectance and then increases. This means that for light vibrating perpendicular to the surface, there is an angle of incidence at which no reflection occurs. With silicon having a refractive index of about 3.5, the surface reflectance is less than 10% for angles upto 60% off the normal, but increases rapidly beyond this.

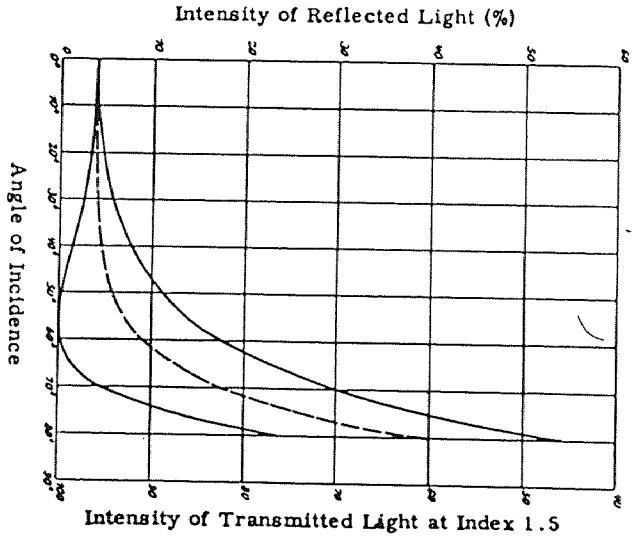


Figure 4.8 Loss of light by reflection at a surface, in terms of angle of incidence.

4.4 Requirements of Anti-Reflection Coating

To suppress or substantially reduce, reflection from the surface of a lens, a coating must fulfill these there conditions.

1. The coating must have a refractive index between that of air and silicon.

2. The amount of reflectance at both surfaces of the coating must be equal.

3. The optical thickness of the coating must be such that the light reflected from the under side next to the silicon will interfere destructively with the light on the air coating surface.

The first and second of these make the refractive index of the coating the geometrical mean of the refractive indices of the silicon and surrounding medium. Since the index of air is unity, the refractive index of the coating must be the square root of that of silicon. The third requirement establishes the thickness of the coating . To interfere destructively, i.e., to result in no movement at all, two equal wave motions must arrive together at a point in opposite phase. This occurs when half wave length has elapsed, and thus the anti-reflection coating must be one quarter wavelength in thickness optically, since the reflected light travels twice the thickness of the coating[30].

A single coating is completely effective at only one wavelength but reduces the surface reflectance at other wavelengths by an amount proportional to the wavelength. To overcome this, multiple coating was developed and the employment of two or more thin films of coating is effective. Lens coating also greatly enhances the light transmitted. For ease of manufacture the plano-convex element is in practice, usually a hemisphere. The primary interest here is the imaging of an object located at infinity; thus the imaging

plane is located at the effective back focal length of the lens, i.e., the lens is being used at infinite conjugate ratio.

CHAPTER 5

PRESENT STATUS

Silicon is transparent to IR radiation beyond its absorption edge of about 1.1 μm, and gives a maximum transmission efficiency of 60 % for wavelength around 1.5 μm. In fact the operating range of the sensor device is 1.2-4.5 μm. So the above mentioned lenses could be fabricated and used very well within this wavelength range.

At least there different approaches have been pursued in the manufacturing of microlenses. There is a selective ion exchange technique, ion-beam etching method, and photoresist melting technique. The methods suggested here exploit etched micromirrors as templates for microlenses. Possible advantages over the other methods are cost and repeatability, as well as the possibility of producing either single or double convex lens. Microlenses having diameters from a few micrometers to several millimeters can be produced by wet etching in $KOH:H_2O$[31]. As mentioned in the literature[32], the concordance of the normalized etched profiles for all diameter lenses demonstrates that the etching is dominating surface reaction rather than diffusion reaction. The outer rims of these lenses can be smoothed by chemical-mechanical polishing for possible use as substrates for microlens arrays. The interest in these planar wave guide focusing elements in the early 1980s has waned, apparently because of the lack of (a) a viable way to produce them economically and (b) control over process parameters. Two dimensional arrays of Fresnel zone microlens can be fabricated and coated with antireflection layers by ion-beam-Sputter deposition technique[9]. This method is subjected to strong limitations. One of the restrictions is the limited lower value of the numerical aperture

(NA) and hence the limited focal length of the lens. Only NA values of 0.1 or higher have been achieved. Another disadvantage is the large deviation from a sphere, for low aspect ratios. The aspect ratio is defined as the cylinder height divided by the diameter of the initial resist cylinders. The sphericity of the photoresist microlenses can be improved by varying the melting temperature and reflow duration or by using the base layer, but these techniques suffer from limitations, due to the polymerization of the photoresist material during thermal reflow. Furthermore, the thermal melted lenses lose the option of further photolithographic processing[33].

For working wavelength of around IR frequency band(1300 nm), the resist lenses are not suitable because of high absorption coefficient[34]. Spherical microlenses are shown to have nearly diffraction limited performance[35]. Ion beam machining is one method to transfer the photoresist arrays into an appropriate material[36]. It is a common practice to ion mill the three dimensional microlens features, made of photoresist, on to the underlying substrate. Most microlens manufacturing techniques which pattern the photoresist do not account for the distortions due to the ion milling. Even for the simplest microlens, the assumption that ion milling is anisotropic in its behavior can introduce significant aberrations[37, 38].

Preliminary results regarding direct fabrication of microgratings and microlenses by laser driven deposition of polysilicon from SiH_4 and bulk silicon etching in Cl_2 atmosphere is reported in the literature[39]. The photoresist microlenses[40] are usable in the near-to-mid-infrared wavelength (0.6-2.7 μm and 3.3 -4.5 μm). Even though photoresist lends itself to simple processing and can be easily reworked, it is desirable to fabricate microlens arrays in IR substrates for wider wavelength range and for

durability[41]. Various etching tools for resist pattern transfer are: conventional parallel-plate reactive ion etcher(RIE), a magnetically enhanced reactive ion etcher(MERIE), an electron cyclotron resonance reactor, and an rf helical resonator(Helicon) reactor[42]. The performance of each tool is examined with respect to etch rate, etch profile, selectivity between the image layer and the pattern transfer layer. For etch rate of 1μm/min., Helicon is found most suitable[44]. A polar coordinator laser writer can be used to create spherical profile in the photoresist. The Photoresist Refractive Optics by Melting (PROM) and Preshaped Photoresist Refractive Optics by Melting (P^2ROM) process use a thermal cycle to produce high optical quality microlenses. The laser writer has several advantages over electron-beam lithography, because it requires neither a vaccum system nor a conductive film on the substrate and has a larger writing field[45]. Arrays of submillimeter microlenses are made from droplets of UV curable optical adhesive dispensed from a pressurized syringes under computer control[46]. Pattern replication technique may be optimized to generate high-quality efficient micro-optics in visible and IR materials[47].

In most practical cases, only one mask is necessary to fabricate the microlens array, with diffraction efficiency exceeding 90 %. Binary optics[48] has diffraction efficiency of 99% for 16-phase level lift-off technology[33]. Here thin film deposition overcomes the shortcomings of RIE. A diffraction limited Fresnel Zone Plate(FZP) lens is proposed to focus the incident radiation on to the sensitive area of the IR detector, which is easily implemented utilizing inexpensive thin film coating and modern integrated optics technique. The proposed thin film FZP substitutes the microlenses used for the same application and FZP lenses present none of the drawbacks of the double

refractive surface microlenses[35]. Replication techniques like embossing or injection molding allow mass production of high quality microlenses[48].

For fabrication process it is necessary to control accurately the level heights, the alignments of the mask, and line widths of the structure. To obtain such control of the level heights, lenses can be fabricated by thin film deposition of SiO_2 on Quartz-glass and Silicon substrate. The layers are produced by Ion Beam Sputter Deposition(ISBD) technique and their optical thickness is controlled by a reflection wide band monitoring system(RWMS)with high accuracy. To reduce reflection losses, possible cross-talk, and feedback effects of cascaded elements in an optical interconnection network, the Fresnel Zone Lens array are coated with two layer antireflection(AR) coating of TiO_2, or SiO_2[49, 50]. The fabrication process for the formation of bifocal microlenses on InP and Si substrates by Ar ion beam etching is also emerging as new technique[49].

Another method of producing micro-lenses on soda-lime plates is by combining the techniques of laser annealing and ion-exchange method and hence therefore referred to as "Laser Ion Exchange Method". The use of this technique makes it possible to simultaneously increase the refractive index on both sides of the glass plate at the laser beam irradiation zone[43].

Major problem in any microlens fabrication process based on melting of the lens material is the control of the spreading . Often lens material can be very well controlled by forming the lens on top of a small pedestal whose melting point exceeds that of the lens material[54]. A tailored distribution of light creates three dimensional pattern in exposed phptoresist, which is then reproduced by ion beam etching in the substrate resulting in the desired microlenses[55].

Recently a new method has been developed for fabrication of microlenses on flat quartz plates by using laser chemical vapor deposition (LPCVD) technique[53]. Fabrication of microlenses by combining silicon technology, mechanical micromachining and plastic molding is another emerging technique[50].

CHAPTER 6

PROPOSED APPROACH

In this chapter, the whole concept of silicon lenses is approached in four steps (I) Design Methodology (ii) Fabrication Technique (iii) Characterization Methods (iv) Results and Discussion. Each chapter is dealt separately.

6.1 Design Methodology

6.1.1 Introduction

The primary objective of the project was to be able to design a lens structure, which could sit on top of the sensor chip and maximize the incoming light and focus that on to the light sensitive area of the chip. In other words, a better lens design could enhance the image quality and increase light sensitivity of the sensor. The basic lens design has two powered surfaces[55]. The first is a convex spherical surface that transforms an incident plane wave on axis to a converging spherical wave. The second is a plane surface with a refraction that is due only to a change in refractive index. The lens thus can be considered and analyzed as simply as a plano-convex element with different refractive media on either side. As the physical dimension of the lens elements are small(~ 60 μm), the lens can be termed as microlens.

The application discussed here is integration of microlens array on the backside of a back side illuminated image sensor wafer to increase the sensor quantum efficiency. Microlenses on the back side of the focal planes concentrate the photons on to a smaller area, thus reducing the required volume of the detector elements, with a corresponding

increment in sensitivity. In back-side thinned devices, the incident flux does not have to penetrate the polysilicon gate sandwich structure and interference effects are much easier to control. With a proper anti-reflection coating, a quantum efficiency of 85 % is possible. Owing to its extremely complex and fragile design, backside illuminated devices are usually limited to scientific applications requiring high quantum efficiency. The procedure developed here for IR wavelength focal plane uses a silicon wafer as the substrate for processing of patterned lenses[32].

6.1.2 Design of FPAs

Microlens array has been introduced into CCD image sensor to compensate for the low sensitivity level of the sensor. In order to realize higher density image sensor, we have introduced additional degrees of freedom into surface profile of microlens[7]. The realization of compact, high-performance solid state image sensors depends on the advances in the combination of VLSI process and optical design technology, which means the introduction of an on-chip microlens array on to the sensors so that we can compensate for the low sensitivity in high density image sensor. It is important to design microlenses considering the presence of main lens or image lens. As mentioned in the literature[7], the large lens surface influences on the sensor sensitivity level and the surface profile can provide higher gain of microlens. Microlens with lower lens height provides higher gain in sensitivity. This is because the lateral magnification of the microlenses with low lens height can be small.

The present 320X244 element PtSi IR-CCD FPA is an interline transfer(IT) imager designed for operation with a readout of two vertically interlaced films per frame.

The pixel layout is shown in Fig. 3.10. Each pixel has a size of 40μmX40μm. The Schottky Barrier Diodes(SBDs) are contained on all four sides of polysilicon gates. It has detector dimension of 33μmX23μm with a nominal fill factor of 44%. The IR-CCD camera is equipped with an objective lens of F/2.

The nonunity fill factor of IR-CCD FPA results in reduced efficiency. Microlens arrays with the same pitch as the pixels can further concentrate the light, which permits the use of small detector areas. This concentration has a number of advantages as

(a) Higher efficiency can be obtained since the fill factor for microlens arrays can generally be made greater than the detector fill factor.

(b) It is possible to have an improved detector array modulation transfer function resulting from reduced cross talk between detectors. Microlens arrays in front of detector array may be of refractive and diffractive type.

An algorithm for specifying a particular design solution has not yet been developed, but can tailor the lens geometry to an individual solution by using a ray-tracing program like ZEMAX. Ray tracing is necessary to investigate the detailed aberrations in the microlens design. The design sequence starts with a specification for image size, field of view, and aperture. The image height and field of view give an approximate focal length and hence the starting value for the radius of hemisphere, r_1. A typical ray trace is shown in Fig. 6.1. In order to estimate the possible improvement of thelight sensitivity of an IT image sensor by using microlenses, the following assumptions are made.

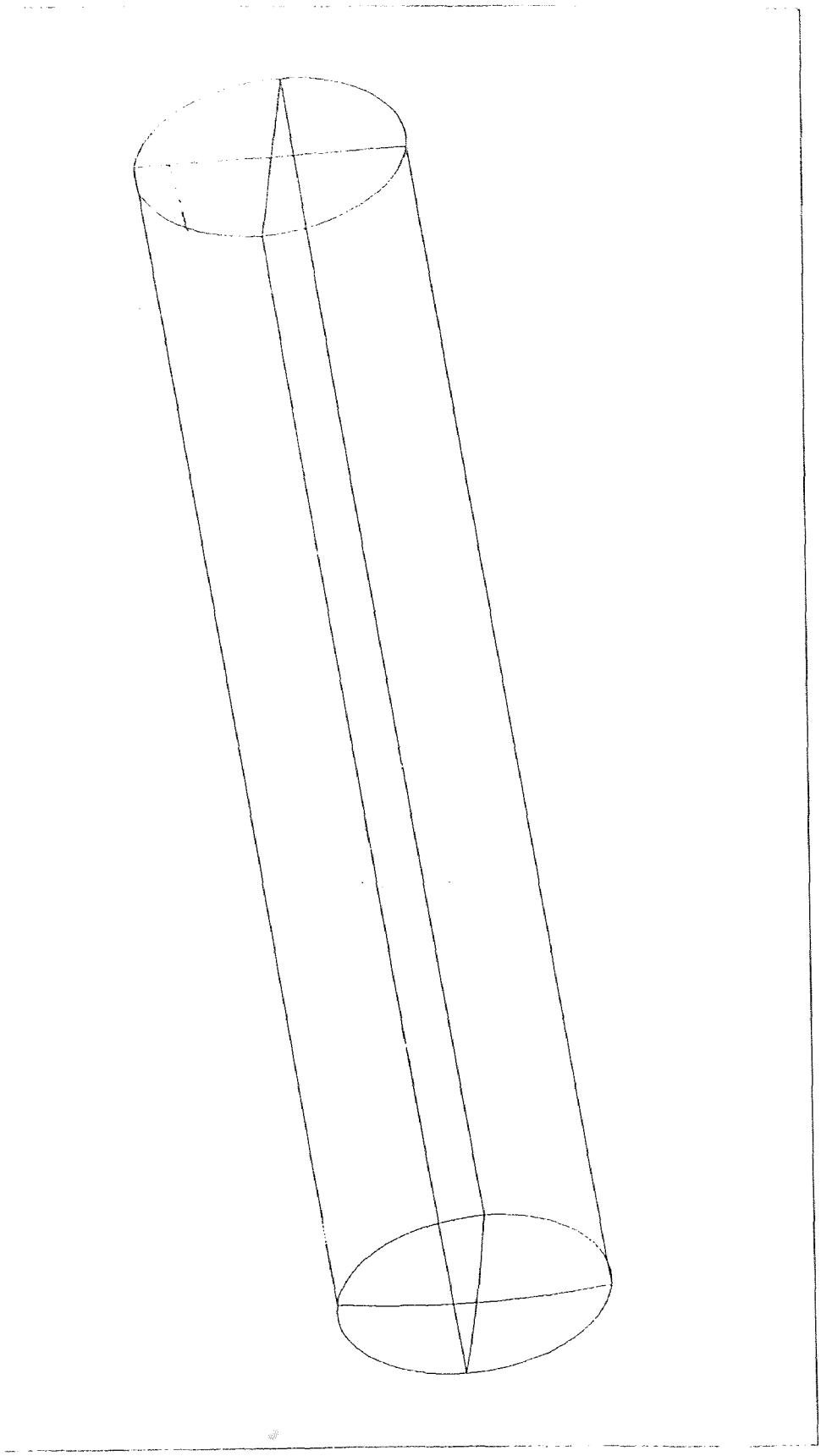


Figure 6.1 A 3-D layout of ray-tracing in ZEMAX

(a) No sensitivity in the channel stop areas and readout areas.

(b) Only photo response in the detector areas.

(c) Completely sensitive to IR in the range of 1μm to 6μm.

(d) No reflection, scattering or aberration losses.

6.1.3 Aperture Ratio or Relative Aperture

If the losses due to the absorption and reflection of light are ignored, the illumination of the image on the axis depends on the ratio of volume of light admitted by the lens, i.e., its aperture and the circle illuminated. If a point object exists at infinity, then the image will. be formed at f_1, which is the focal length of the lens, and the circle of illumination may be represented by F_1. If the lens is replaced by another with the same diaphragm in front, but having twice the focal length, the volume of light admitted is same, but both the image and the diameter of the circle of illumination will be twice as large(F_2). Thus the volume of light admitted is proportional to d^2, while the circle of illumination is proportional to F^2. Therefore the illumination on the axis is f/d. This is termed as aperture ratio or relative aperture.

Fig. 6.2 presents a cross sectional view of a cylindrical microlens on an image sensor. The important parameters are the radius of curvature(R), the height(h) and the distance(d) between the vertices of the lens surface and the sensor surface. These parameters can be calculated as a function of the F-number of the camera(F), the total width of microlens(p), the dimensional reduction factor τ, and the effective light

transmitting width of the window (w). The dimensional reduction factor (τ) is given by: $\tau = w / p$

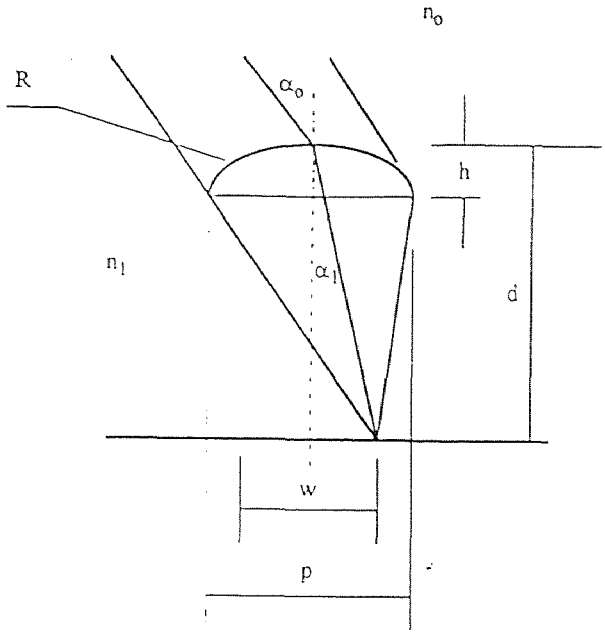


Figure 6.2 Cross-sectional view of microlens on an image sensor

One can predict the paraxial optical characteristic of a simple hemispherical lens by using conventional optical relations. Consider a hemisphere of thickness t_c, equal to the radius of the second surface, r_1 and the radius of the second surface, r_2 be infinity. The light incident on each pixel has an aperture angle(α_0) which is given by the F-number($F_\#$) of the camera. The $F_\#$ is related to the aperture angle α_0 of the incident radiation by

$$F_\# = 1/2\sin \alpha_0$$

The calculations are made with the assumption that on the image side, silicon has index of refraction n and image side aperture angle α_1 is small. The optical power of microlens is given by

$$K = (n - n_0)/R = (n-1)/R$$

where n_0 is the refractive index of the air space(~1) and n is the refractive index of the lens material. The focal length of the image side is given by

$$f = n/K = nR/(n-1)$$

The image of an objective lens is therefore a disc of diameter

$$d = f/F_{\#} = nR/(n-1)\ F_{\#}$$

Considering a circular microlens of diameter d, concentrating all the incident radiation onto a circular detector of diameter D, the area gain is given by[15]:

$$\text{area gain} = d^2/D^2 = \{\ nR\ /\ D(n-1)F_{\#}\ \}^2$$

So the area gain can be maximized by increasing the radius of curvature of the microlens or increasing the refractive index. The fact that the microlens gain increases with decreasing $F_{\#}$ allows some extra flexibility in the design of IR imagers[56].

The radiation of each individual lens subtends a semi angle of α_0 in the object space and this leads to a transverse image dimension w_i in the focal plane.

$$w_i = 2\alpha_1 f = 2\ \alpha_0\ nR/(n-1)$$

where w_i is the image width on the focal plane, and α_0 is the semi-angle of incoming light in the image space. The image width w_i should be smaller than the geometrical width w of the individual pixel. This constraint leads to the following equations :

$$R \leq (n-1)\ \tau p F_{\#}$$

$$d \leq f_1 = n\ \tau p F_{\#}$$

$$h = R - (R^2 - p^2/4)^{1/2}$$

There are practical limitations to the minimal value of R. An absolute lower limit is R= (1/2) p, but larger values are actually required to decrease lens aberration and to lower the reflection at the microlens interface. For perpendicular impinging light, the reflection losses are about 6%, but increases to about 20% at steeper sides of the microlens. An anti-reflection coating can reduce this problem.

6.2 Fabrication Technique

6.2.1 Introduction

This chapter discusses in details about the fabrication procedure. A brief process flow is also described below. A schematic of the process flow is also provided, which shows the cross-sectional view after each step. The lens layer is made of silicon. Spherical microlenses are fabricated by thermal reflow of melting resist technology. Resist cylinders are patterned by photolithography, and subsequently dissolved in a controlled solvent atmosphere. This technique enables the fabrication of spherical resist microlenses of selectable rim angles in a range from 1 to 30 deg. by selecting the appropriate melting temperature and exposure time. The photoresist lenses are transferred into the silicon substrate through reactive ion etching[57]. The aberrations of spherical lenses decrease with increasing refractive index of the material.

The thickness of the silicon layer must be controlled to get right optical distance and planarization of the bottom surface. This is necessary to establish uniformity between lenses and sensors. All the fabrication steps except etching were done at the NJIT Microelectronics Research Center. Plasma etching was done in CVD laboratory at NJIT.

6.2.2 NJIT Clean Room

All the process steps were done at NJIT clean room and CVD laboratory. NJIT cleanroom is a 1200-sq.-ft and class 10 fabrication line. It is equipped with all the necessary equipment for processing wafers up to 6 inch in diameter. Some of the equipment in the cleanroom are:

1) Wafer inspection microscope, Dektak profilometer

2) Nanometrics optical line width

3) Wet chemical station Ultratek mask/wafer scrub

4) Semitool spin/rinse dryers

5) Karl Suss exposure system

6) Nanometrics FTM(Film Thickness Measurment)

7) Inspection microscope

8) MTI photoresist coat and develop system

9) Drytek reactive etching system

10) Leitz MPV FTM

11) Varian sputtering system

12) BTU diffusion furnace

13) BTU LPCVD furnace

14) MDA toxic gas monitors

15) Tube wash stations

16) MG Industries gas cabinets

6.2.3 Outline of Process Steps for Fabrications

The various standard VLSI process steps followed are outlined here. First the flow chart for the fabrication of the lens is detailed and following this is a schematic of the process details.

6.2.4 Flow Chart for Fabrication

The following chart shows a flow diagram of the entire process to fabricate silicon lens.

Silicon Wafer

⇓

Wafer Numbering

⇓

Primary Cleaning

⇓

Spin Drying

⇓

Applying Primer

⇓

Applying Special Photoresist

⇓

Soft Baking

⇓

Exposing to UV light for Patterning the Resist(Mask)

⇓

Developing

⇓

Hard Baking

⇓

Developing

⇓

Hard Baking

⇓

Thermal Reflowing of the Resist Patterns

⇓

Inspection of the Pattern

⇓

Reactive Ion Etching(RIE)

⇓

Lens Patterns on Silicon Substrate

6.2.5 Process Flow

A detailed description of each step of the process flow is described here followed by the cross sectional view after each step of fabrication.

6.2.5.1 Starting Material: Starting material for the microlens process were p-type (boron doped), <100> oriented 5 inch silicon wafers, with resistivity of 1.65-3.85 ohm-cm.

6.2.5.2 Wafer Numbering: All the wafers were numbered for individual attention and identification. This was done by scribing on the back using a diamond tipped pen.

6.2.5.3 Primary Cleaning: Impurities may affect the normal operation of the lens and give a blurred vision. Hence for high degree of efficiency and reliability it is necessary to get rid of all sources of contamination. Surface cleaning is important prior to high temperature processes because impurities react and diffuse at much higher rate at elevated temperature. The most commonly used wet chemical cleaning technology is based on hot alkaline or acidic peroxide(H_2O_2) solutions. These are used to remove chemically bonded films from the wafer surface prior to critical process steps.

RCA cleans are based on two step process: SC-1 is an aqueous alkaline solution which removes organic films, while SC-2 is an acidic mixture used to remove alkali ions, cations and metallic contaminants. SC-1 is typically a 5:1:1 solution of DI water, "unstibilized" H_2O_2(30%), and ammonium hydroxide (27%). This solution is very effective in removing organic contaminants. SC-2 typically consists of 6 parts of H_2O, one part H_2O_2 , and one part of hydrochloric acid(HCL, 37%) and is effective in removing heavy metals. The processing temperature is 80 ^{o}C.

6.2.5.4 Spin Drying: The wafers are put in a spin dryer and rotated vertically at a very high rpm for 10 minutes to get rid of all water particles.

6.2.5.5 Applying Primer: Perfect adhesion of the resist, which minimizes under cutting is generally the goal. The wafer was primed with a pre-resist coating of a material designed for better photoresist adhesion. It is 1% solution of hexamethyldisilazane

(HMDS) in xylene, spun on the wafer and allowed to dry for a few seconds before resist applications can be used. The wafers are then ready to be coated with photoresist.

6.2.5.6 Applying Photoresist: The main requirements for resist application are that the resist be pin-hole free and of uniform and reproducible thickness. The special photoresist(Shipley STR 1045) was applied as a film of 6μm thickness to the substrate. This takes into account the 20% shrinkage of the photoresist after soft baking. Spin coating is the most widely used technique to apply a uniform adherent film of desired thickness. This process was carried out by (a)dispensing the resist solution on the wafer surface (b)accelerating the wafer until the final rotational speed and (c)spinning at a constant speed until the desired thickness is reached. This makes the resist essentially uniform and dry. Here the spin speed is 4000 rpm, for 40 s at room temperature with acceleration rate of 1-10 krpms/s .

6.2.5.7 Soft Baking: After the wafers are coated with resist, they were subjected to a temperature step called soft-bake or pre-bake. This step accomplishes several important purposes including (a) driving off solvents from spun-on resist, reducing its level in the film from ~20-30% to ~4-7%; (b) improving the adhesion of the resist, so that it is better able to adhere during the development step; and (c) annealing the stresses caused by the shear force encountered in the spinning process. The condition under which photoresist is softbaked determine a number of parameters in the subsequent steps of the process. As a result of the solvent loss during the soft bake, the thickness of the resist is also reduced,

typically by ~20%. Here the softbaking temperature is 100 ^{o}C for 60 s on a hot plate. After resist coat has been stabilized, the wafer is ready for photolithography.

6.2.5.8 Photolithography: After the wafer has been coated with resist and suitably softbaked, resist film was exposed to UV light through a photomask. The mask contains clear and opaque features, that define the patterns to be created on photoresist(PR) layer. The patterns on the mask are made of chrome and are permanent. The degree of exposure was adjusted by controlling the energy impinging on the resist. The exposure parameters differ from resist to resist thickness, in this case, in a Ultratech 1000(0.34NA), Numerical aperture:0.34 NA, Sizing energy: 221 Mj/cm^2, Sizing ratio:1.0E_0, Exposure latitude: 12%, Aspect ratio:5:1 and exposure time: 30s.

6.2.5.9 Developing: After exposure, the resist film was made to undergo development in order to leave behind the image, which will serve as the basis for the lens pattern. Development is another of the critical steps in the photoresist process. The first goal of the development process is that the unexposed positive resist film should be minimally attacked by the developer. The areas in PR exposed to light are made either soluble or insoluble in a specific solvent known as developer. Here resist was retained only on the desired areas and removed from elsewhere. Here the developer is MF(Metal Free) 319 family, and total puddle time was 120 s at room temperature.

6.2.5.10 Hard Baking: After developing the wafers are again put on hot plate for 120s at temperature of 110 ^{0}C. Its main purposes are to remove residual solvents and improve adhesion.

6.2.5.11 Inspection of the Patterns: Following this development, an inspection was performed. The purpose was to insure that the steps of various process up to this point have been performed correctly and to within the specified tolerance. Any inadequately processed wafers detected by this inspection could have their resist pattern stripped and repatterned.

6.2.5.12 Thermal Reflow: To achieve thermal reflow the substrate temperature must exceed the glass transition temperature T_g, which ranges between 120 to 160 ^{0}C for typical positive photoresists. Then the amorphous polymer changes abruptly from a rubbery state to a glass state, which enables material flow while the viscosity decreases with temperature. But at the same time, the resist changes chemically because the remaining solvent evaporates and resist cross-links its polymer chains. This continuing process stops the material flow usually before an equilibrium of the interfacial tension has settled, and the lens surface does not reach a spherical form. If the aspect ratio of the resist cylinder is low, even a small dip may develop in the center of the lens. Therefore a theoretical model of the lens, which includes all these aspects is complex, and detailed knowledge of several process parameters is necessary for prediction. A practical advantage of the thermal reflow process is the fixed diameter of the lens during

formation; the high viscosity of the resist results in boundary conditions at the interface of the silicon and air that prevents an increase in the resist base in most cases. But with low viscosity resists, an additional pedestal below the resist cylinder may be necessary to avoid spreading of the resist[59]. Basically one would expect an increase or reduction of base diameter until a characteristic surface contact angle ø has been achieved. The rim angle is given by the interfacial tensions δ_{ij} of the three boundaries: $\cos ø = (\delta_{13} - \delta_{12})/\delta_{23}$. Here the indices denote: 1-substrate; 2-resist; 3-atmosphere. This equation represents a minimum state of surface energy of the three interfaces. Chemical bonds between the photoresist and the substrate prevent a reduction of base diameter. Instead the diameter of the lens remains fixed, and the surface energy minimum adjusts the rim angle away from ø, such that again a spherical lens shape results.

The focal length of lens depends on the thickness of the exposable layer as well as on the diameters of the resist cylinders. In practice, however the actual focal length depends on the critical angle between the substrate and the resist at the circumference of the lens[24]. This angle is a material constant which depends only on the three constants of the surface tension between substrate, liquid and air. The process of transferring a cylinder cross section to a circular one under the action of surface tension works reasonably well provided that the resist is sufficiently thick[8]. Under the force of gravity and surface tension the resist takes a round shape. For the special photoresist, melting temperature was at 135 ^{o}C for 120 s.

6.2.5.13 Dry Etching: Dry etching was necessary to transfer the accurate pattern on to the silicon substrate. A melting process of resist cylinders produces nearly ideal spherical lenses, because of the surface tension. Apart from the fact that it is difficult to obtain a selectivity of 1:1 between resist and silicon, which would guarantee equal heights of the resist and of etched lenses, the main reason for the behavior the specific etch mechanism of the RIE is anisotropic pattern transfer. The etching process is of a chemical nature supported by ion bombardment. The positive ions are accelerated towards the cathode where the substrate is placed. Through the impinging ions, the chemical bonding between the silicon atoms are excited and prepared for a chemical reaction with the etching components. The extent of the excitation depends on the kinetic energy of the impinging ions transferred to the silicon atoms. The energy transfer increases with number of impinging ions per unit area of lens surface. The reactive ion etching (RIE) machine is usually a vacuum chamber with a pair of parallel electrodes. A high frequency field breaks and produces in the etching gas, a plasma of electrons, ions and neutral radicals. The electrons drift to the lower electrode providing a negative bias voltage. The upper electrode is grounded so there is a direct voltage to accelerate the ions to the etching electrode. This means that the etching process is carried out under at 90^0 angle to the substrate. The etching gas is selected so as to generate species which react chemically with the material to be etched, and whose reaction product with the etched material is volatile. The reaction gas here is mixture of O_2, CF_4 gases. The etch rate depends on the percentage of O_2 in the reactive gases. By varying the flow of O_2, the etch rate can be altered. So spherical aberrations can be corrected by varying the ascent of the lens border.

Different etching conditions were applied to observe the effect on the microlenses such as:

(a)O_2 flow: 7 sccm/min, CF_4 flow: 30 sccm/min, Power: 197 W

(b)O_2 flow: 14 sccm/min, CF_4 flow: 60 sccm/min, Power: 400 W

(c)O_2 flow: 28 sccm/min, CF_4 flow: 60 sccm/min, Power: 400 W

For all these cases, pressure was at 250 mTorr and time was 60 minutes. Only in the last case, the photoresist was etched completely and the exact pattern of the lens was transferred to the substrate.

A schematic of the process flow diagram is shown in Fig. 6.3.

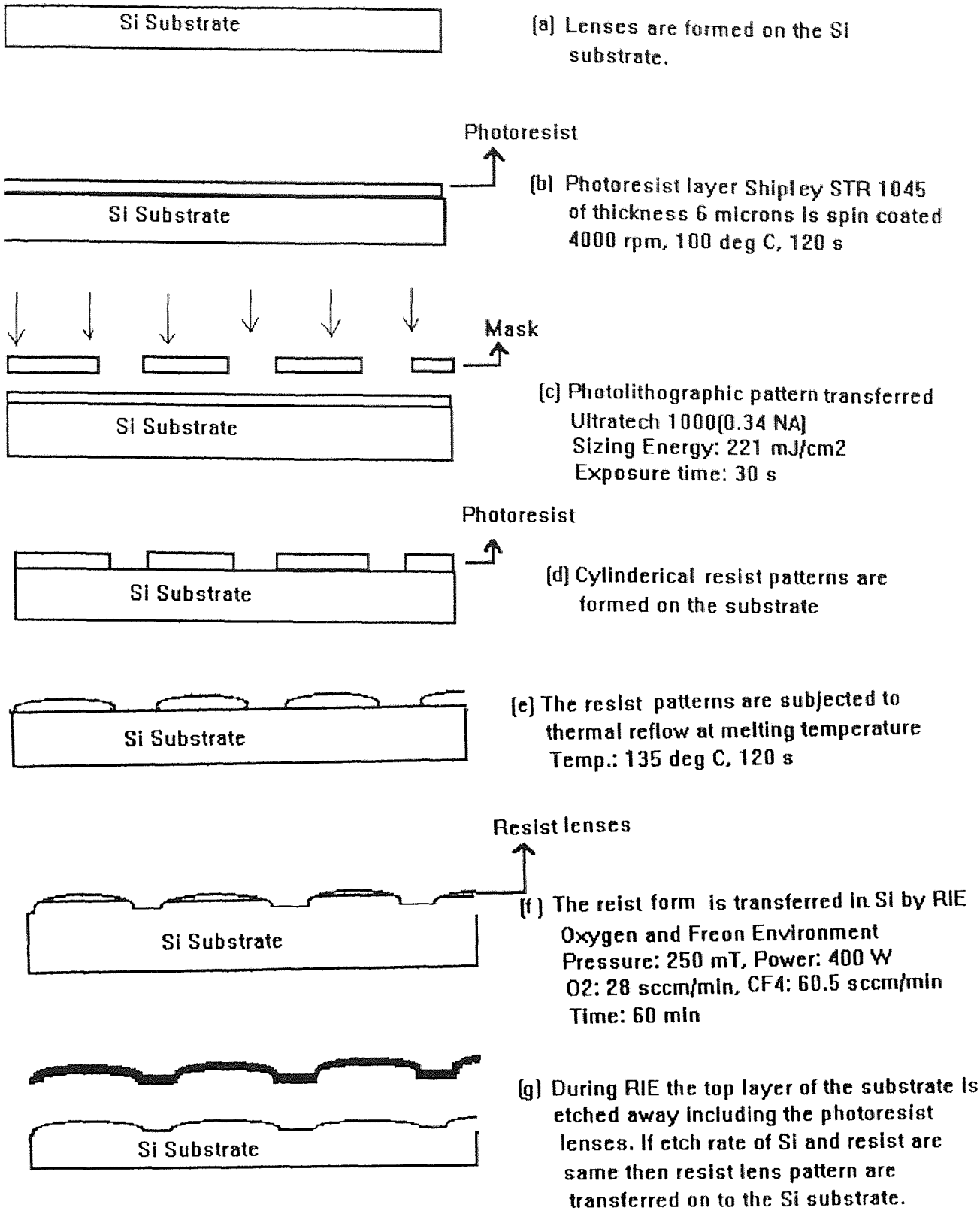


Figure 6.3 Schematic of Process Flow

6.3 Characterization

6.3.1 Introduction

Optical microlens array with diameter in the order of less than hundred micrometers present unique challenges for optical performance measurements. Characterizing these devices require measuring both the imaging characteristics and diffraction efficiencies. As suggested in the literature[58], the imaging and radiometric properties of erect lens arrays made up of convex microlenses may be derived from a ray analysis[24]. In the present case surface profoilometry and scanning electron microscopy has been performed to observe the lens pattern.

6.3.2 Surface Profilometry

Surface Profilometry is a useful tool for determining microlens focal length and optical aberrations. An accurate surface profile is sufficient to determine lens focal length for plano-convex lens, within the accuracy to which one knows the material index of the refraction and any curvature of the plano surface. We have measured the surface profile of microlenses using Tencor P-1 contact surface profiler with a 5 μm radius tip[60]. The results of the surface profilometry have been shown in Fig. 6.4.

6.3.3 Microscopy

Scanning electron microscopy(SEM) has become an important tool for VLSI analysis because it has the capability of providing much higher magnification, resolution and depth of field than optical microscopy[1-3, 58]. The resolution of SEM can be up to 10

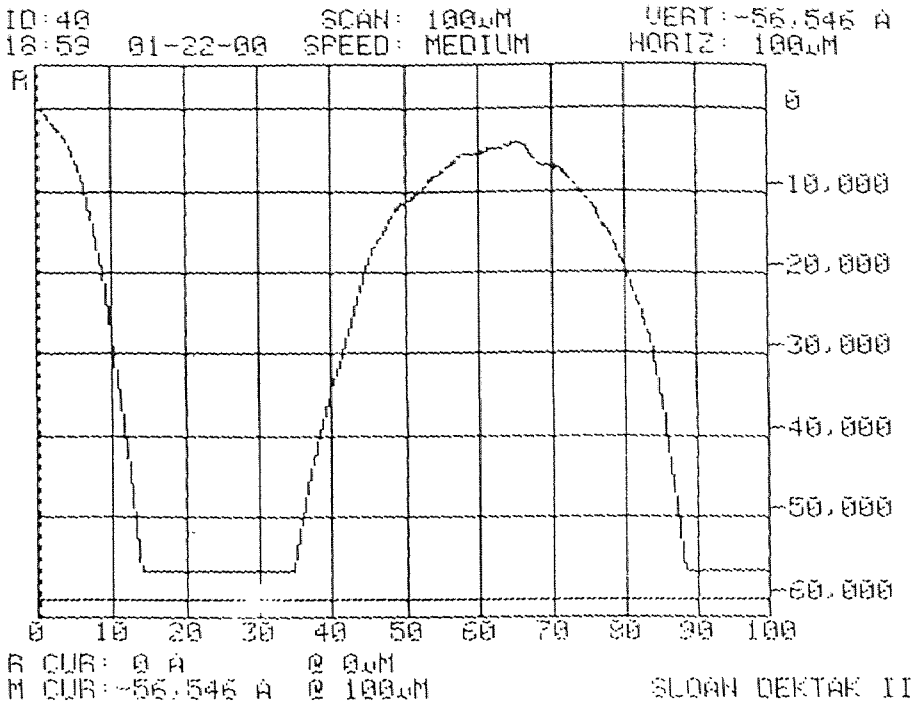


Figure 6.4 Surface Profilometry of the lens pattern

A^0 with magnification up to 100,000 times and the depth of fields of 2-4 µm. The high depth of field makes SEM especially useful for high magnification. SEM analysis can be used to yield information on line width, film thickness, step coverage, edge profiles after edge and other morphology data. The micrographs of electron microscopy are furnished in Fig. 6.5.

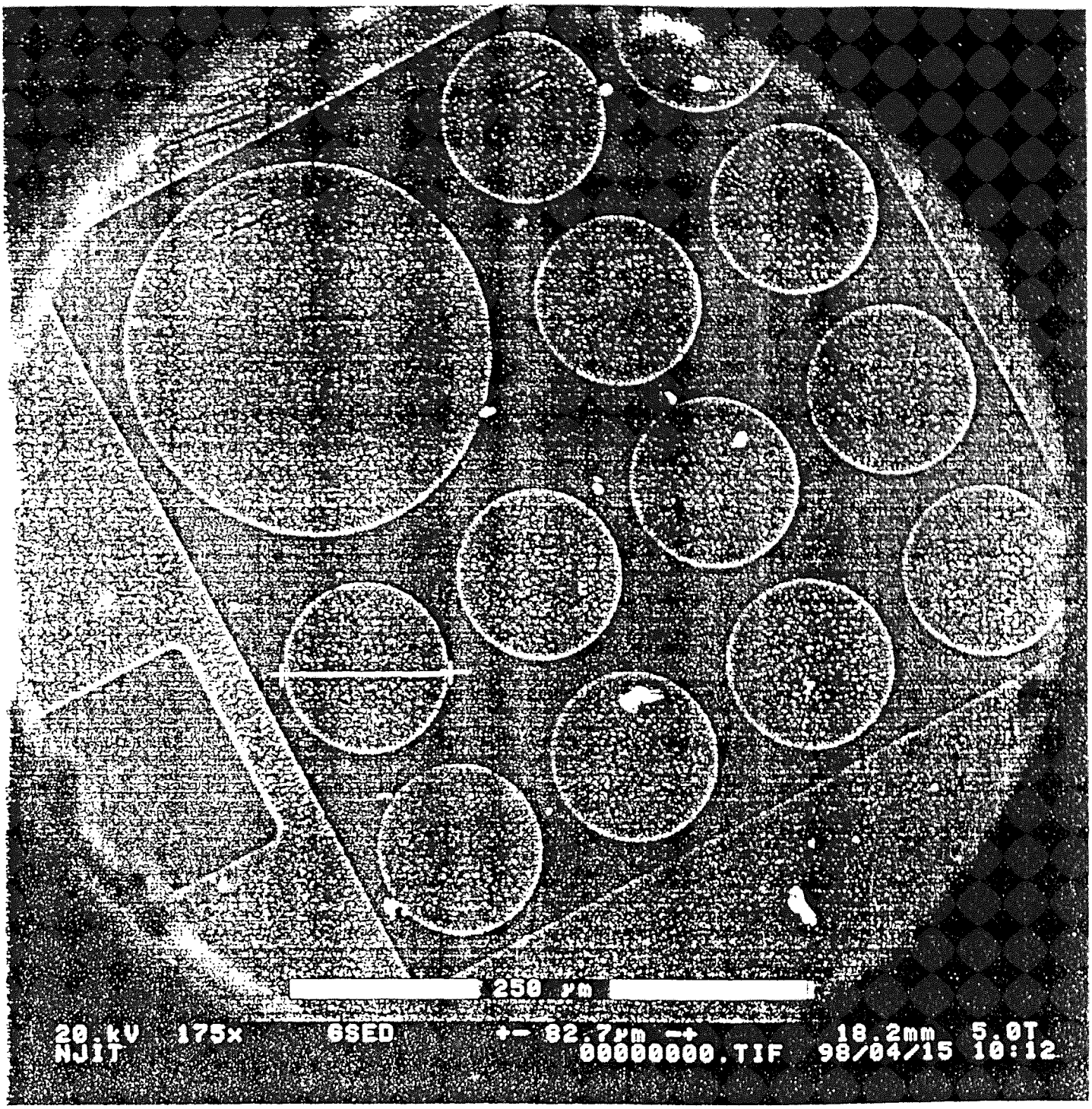


Figure 6.5(a) SEM Micrograph

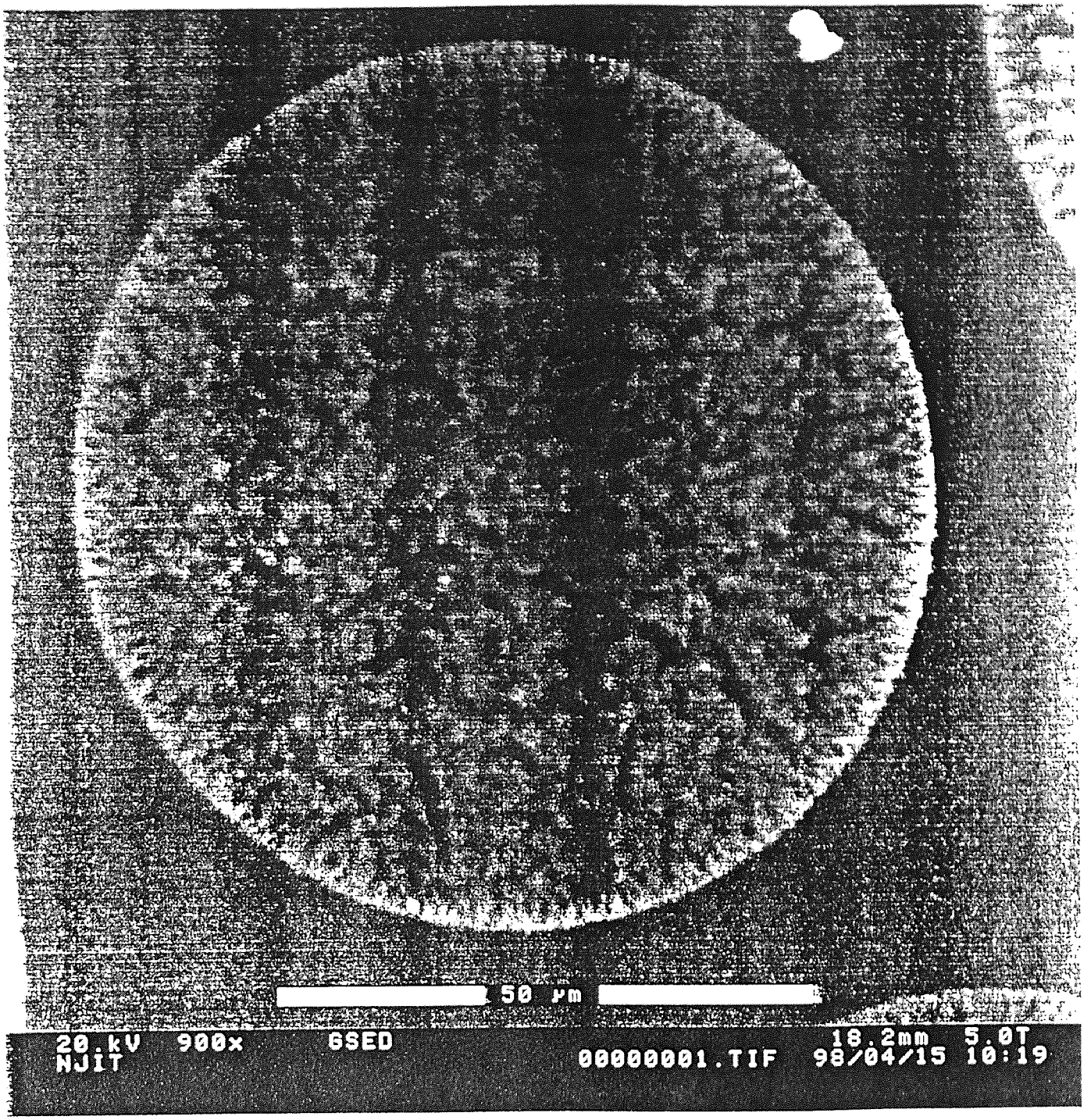


Figure 6.5(b) SEM Micrograph

6.4 Results and Discussions

6.4.1 Photoresist

With the variation of the spin speed and time, the thickness of the photoresist film goes on changing. Every lens dimension needs a specific thickness of the photoresist film as mentioned above. So as per the requirement of the lens, a specific thickness can be calculated and the corresponding spin speed and spin time can be selected. A graph of the resist thickness as a variable of the spin speed for the special photoresist (Shipley)STR 1045 is shown in Fig.6.6.

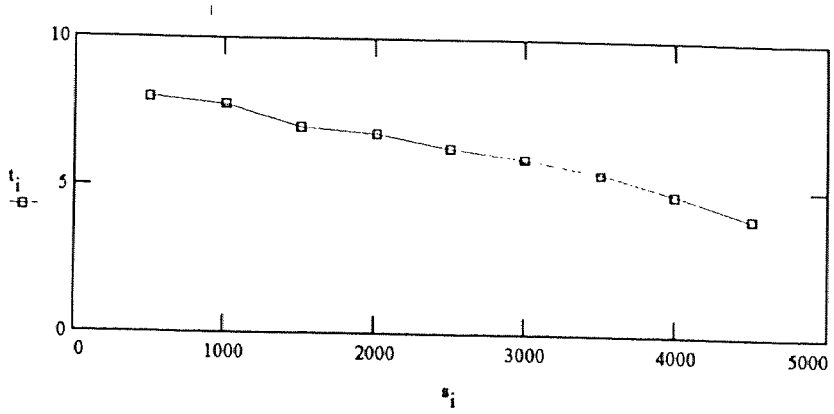


Figure 6.6 Variation of thickness(μm) of special photoresist(Shipley STR 1045) with respect to spin speed(rpm) at 100 ^{0}C/120s.

6.4.2 Etching

Because of the direction of the incidence of the ions which is vertical to the cathode, the number of ions per unit area("ion density") is greater in the middle of the lens than in the in the rim region. This fact contributes to a stronger excitation of atoms in the middle and

so enhanced etching. Therefore the etch rate decreases from the middle to the rim region of the lens. This is the reason one can't obtain spherical etched lenses by transferring spherical resist lenses via RIE[33].

To fabricate microlenses with low numerical aperture, the photoresist should be etched faster than the substrate[37]. Satisfactory lenses are formed only if the ratio of the diameter of the cylinders d to the thickness of the photoresist layer T is correct. For values around d = 10T, the lens shape is good. A correct separation distance between adjacent lenses is necessary to prevent fusion during melting[37].

6.4.3 Results of Optical Calculations

As mentioned above[36], minimum index of refraction can be calculated at the absolute lower limit R= (1/2)p, which leads to

$$p/2 = (n-1)\tau p F_{\#}$$

$$n = 1/(2\tau F_{\#} + 1)$$

For the IT image sensor considered, the maximum aperture angle α_0 is given by the camera with $F_{\#} = 2.0$ is 14.5 ^{0}. Again the refractive index of silicon is 3.5, which fulfills the above mentioned minimum requirements of 1.43. To reduce the spherical aberration, the lens profile should be less steep than the sphere in the rim region[38]. An estimation of the lens parameters(R, d and h) calculated using these equations leads to (with constraints $\tau<1$, that is $w<p$)

$$R < p(n-1)/2\ \alpha_0 n_0$$

At wavelength of 4μm and low temperature(100 ^{0}K), the refractive index of silicon n= 3.39 gives the range of R < 190 μm. Again d< 272 μm can be obtained from above. This indicates that an appropriate thinned silicon substrate is required for use in this microlens system. As an example, the reduction factor of the microlens is taken to be τ = 0.75, i.e. w = 30 μm. The corresponding calculated results are given in table 1.

Table 1-Calculation of Lens Parameter

$F_{\#}$=2.0, n=3.39	p(μm)	w(μm)	τ	R(μm)	d(μm)	h(μm)
Standard imaging pixel	**40**	**30**	**0.75**	**142**	**204**	**1.4**

6.4.4 Simulation Results

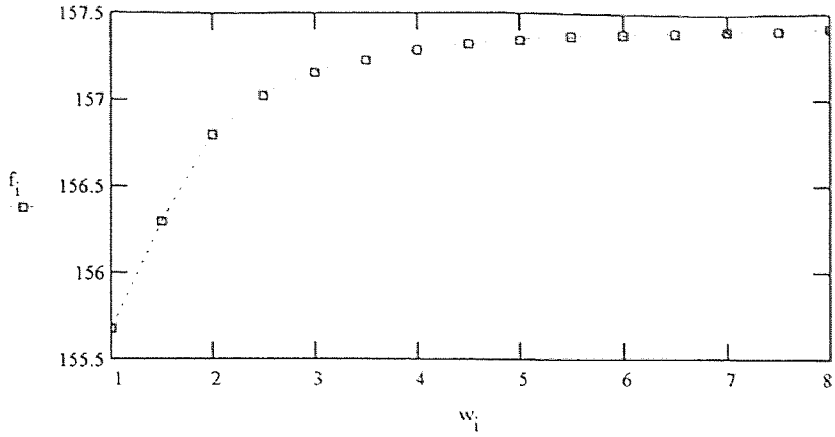
The proper alignment of the microlenses with respect to the detector area is of primary importance. For this, one should have a good idea about the behavior of the lenses particularly the focal length at different temperatures and wavelengths. For this reason, simulations were done at three different temperatures and wavelengths in the range of 1-8 μm, taking into account the refractive index change of the lens material. Two basic equations were used for simulations:

$$\text{focal length}(f) = nR/(n-1)$$

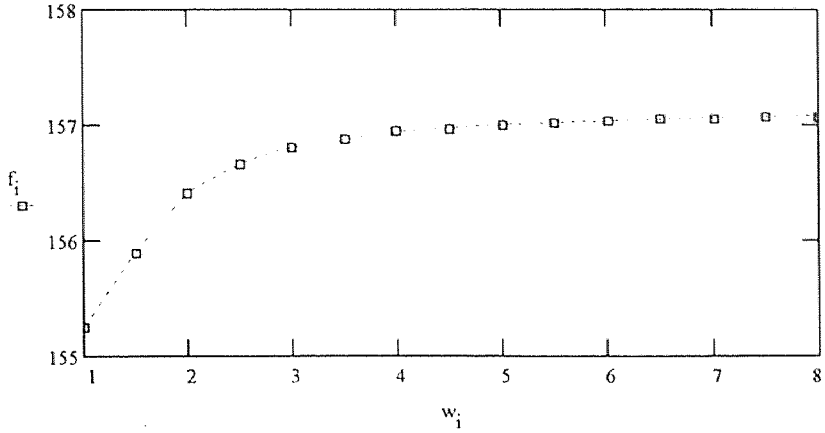
$$\text{Focal number}(F) = f/d = R.n/((n-1)2r)$$

Fig. 6.7 shows the change of focal length at different wavelengths at (a) 100 ^{0}K, (b) 250 ^{0}K and (c) 350 ^{0}K. As the temperature is increased, the focal length is reduced. Again in Fig. 6.8, (graph of f Vs n), the focal length decreases with increasing temperature. In Fig. 6.9(graph of F Vs w), the focal length decreases with increasing temperature. So while aligning the microlens surface with detector area, the change of focal length should be taken into account. Here w is the wavelength, n is the refractive index of silicon, f is the focal length and F is the focal power.

(a)



(b)



(c)

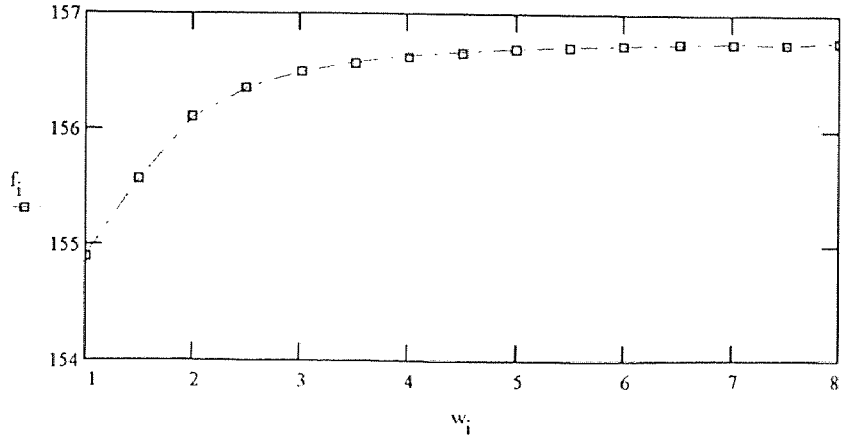
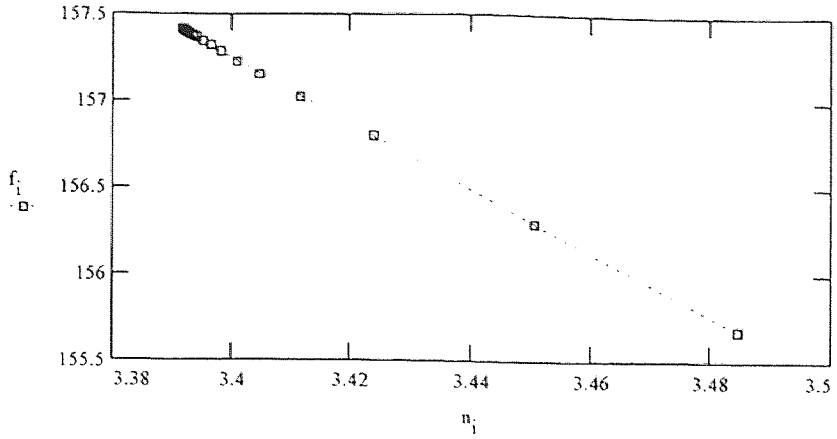
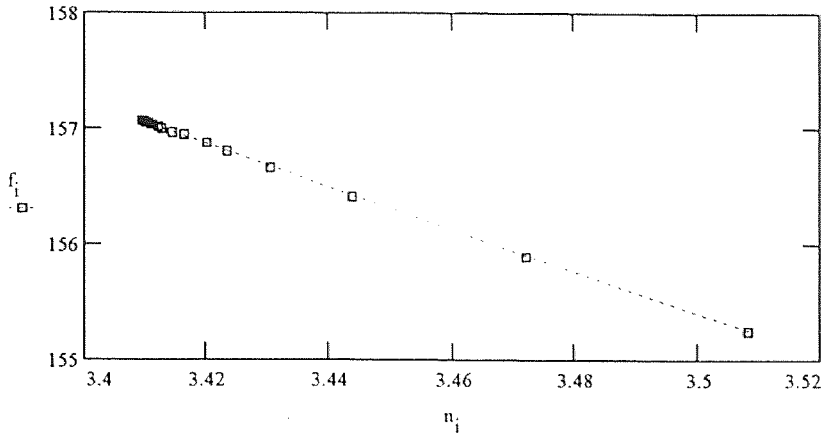


Figure 6.7 Graph of focal length(f) Vs wavelength(w) at (a) 100 ^{0}**K** (b) 250 ^{0}**K** (c) 350 ^{0}**K**

(a)



(b)



(c)

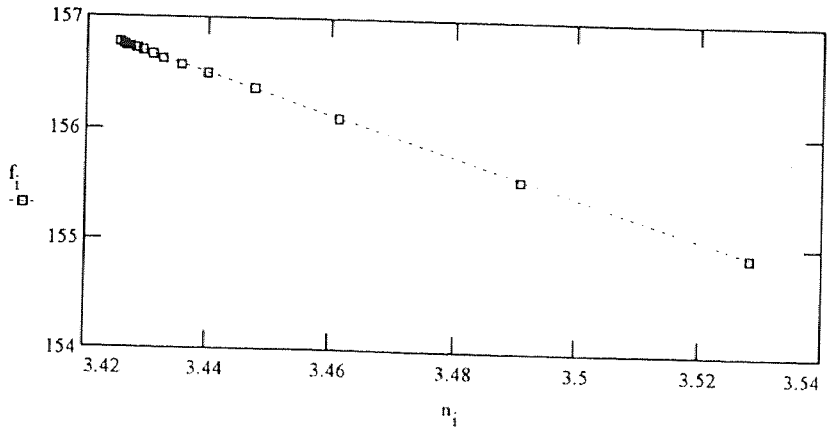
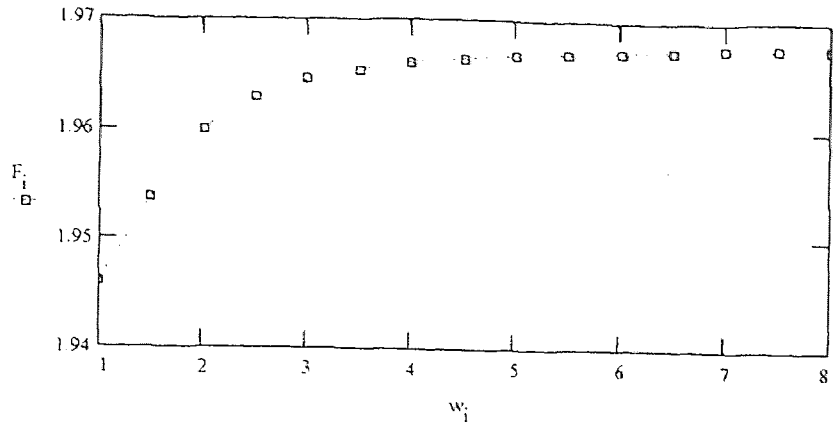
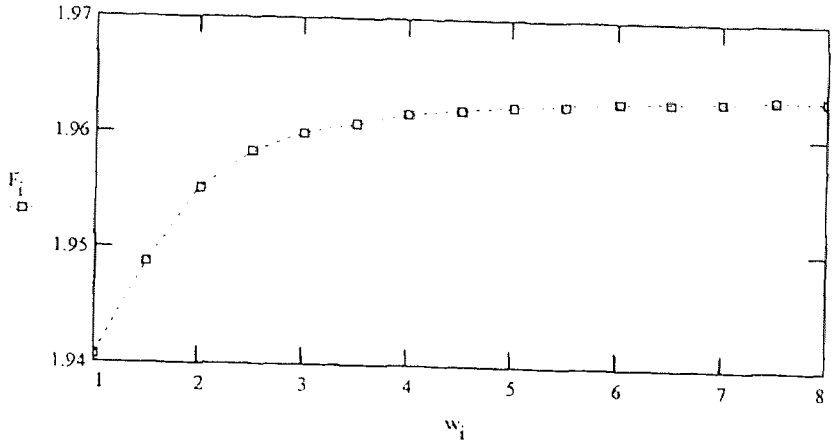


Figure 6.8 Graph of focal length(f) Vs refractive index(n) at (a) 100 ^{0}**K** (b) 250 ^{0}**K** (c) 350 ^{0}**K**

(a)



(b)



(c)

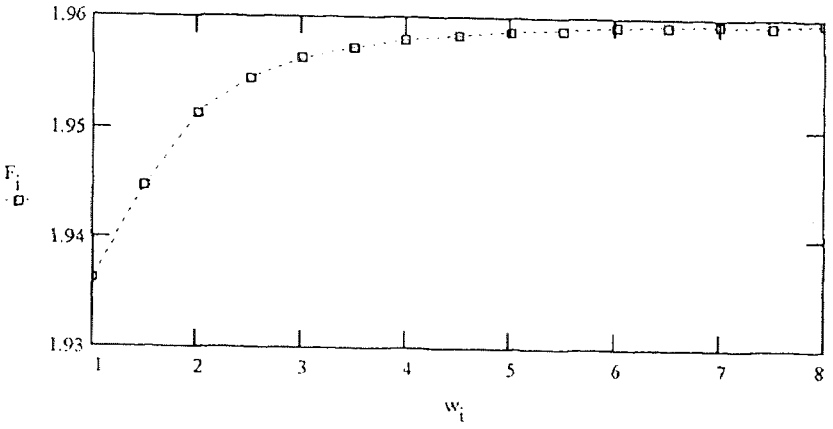


Figure 6.9 Graph of focal number($F_{\#}$) Vs Wavelength(w) at (a) 100 ^{0}**K** (b) 250 ^{0}**K** (c) 350 ^{0}**K**

CHAPTER 7

ISSUES

This method of fabricating lenses is subjected to strong limitations. One of the restrictions is the limited lower value of the numerical aperture(NA) and hence the limited focal length of the lens. Another disadvantage is the large deviation from a sphere, for low aspect ratios. The aspect ratio is defined as the cylinder height divided by the cylinder diameter of the initial resist cylinders. The sphericity of the photoresist microlenses can be improved by varying the melting temperature and reflow duration or by using the base layer, but these techniques suffer from limitations, due to the polymerization of the photoresist material during thermal reflow. Furthermore, the thermally melted lenses lose the option of further photolithographic processing[10]. A detailed understanding of the etch process is required for the successful production of good microlenses. An appropriate choice of etch parameters can minimize the aberrations. The careful removal of metal ions is crucial to obtain small roughness values[11]. Roughness is a serious problem in all dry etching techniques. Better results can be achieved by adding noble gas (He) to the etching gas. Helium has a higher thermal conductivity, and provides some additional cooling for the wafer. Another important reason for surface roughness is the rinse time for the resist lenses with deionized water after the wet chemical development. A disadvantage with longer rinse time is the deposition of water into resist. For this reason, the resist lenses can not be melted the same day after the development. After one day, the water in the resist has evaporated and the melting process can be initiated without damage[11].

The fabrication, mounting and alignment of microlens arrays on a CCD imager requires submicrometer precision[61]. Bonding of separately produced microlenses to microchips is a nontrivial procedure requiring proper alignment. Moreover the necessary alignments may be difficult to maintain over extended periods of time due to environmental factors. For example, high temperature swing may cause differential thermal expansion between the substrate and the microlenses and the electro-optic device on which they are mounted. Some designs may also require short distances (perhaps a few tens of microns) between microlenses and the plane of the IC chip. In this case, the very thin substrates needed to hold microlenses may be difficult to handle in a production environment. It is therefore clear that monolithic production of microlenses and microlens arrays would have substantial practical advantages over production methods in which microlenses are produced separately and subsequently bonded[54].

Thus microlenses can be directly fabricated on the backside of the Si wafer, opposite to the PtSi detector and made themselves compared as part of the silicon substrate.

CHAPTER 8

CONCLUSION

For the imaging sensors considered, a theoretical improvement of light sensitivity of 28% (preliminary) can be achieved. But with precision modeling and deployment of AR coating, the light sensitivity could reach upto ~90 %. A compact lens system, primarily for use with solid state image capture sensors, has been designed. The lens design which launches a format of low-cost, imaging lenses, is particularly advantageous in wide angle, low light applications. The lens is substantially smaller and simpler in structure than most conventional designs. Although limited by a lens with a fixed aperture, control of camera exposure by varying the sensor integration time compensates for this lens design restriction, but this technique does not provide the bonus of higher resolution and long depth of field that results when aperture reduction is used to control sensitivity[61].

The critical mechanical tolerances that affect image quality are the sphericity of the hemisphere and the overall length of the lens(distance from the front to the rear surface). One can improve the lens performance slightly by moving the refracting surface between the two elements along the z-axis towards the image plane. This makes the first element a hemisphere. Practically, this also means moving the aperture which is not desirable and reduces the numerical aperture. A slight curve in this surface, in theory, will also produce marginal improvements.

For lenses, with a narrower field of view, sherical geometry limits the image quality and resolution. One can obtain an improvement in performance by using an aspheric surface although this often negates the cost effectiveness of lens for manufacture in low

volumes. In wide-angle applications, the lens offers a performance that is better than can be obtained from other conventional solutions. If the design were used for narrower fields, the physical size of the lens would be larger and the speed of lens would drop; the design thus looses its performance advantage over an aspheric single design[5].

What is the future of binary optics technology development ? High quality micro-optics will be integrated into layered systems. Such multilayered systems optics and optics integrated with photonics and microelectronics will form the initial building blocks of amacronic Focal plane arrays. By exploiting the fill factor enhancement made possible by microlens arrays, photodetectors can be made smaller and spaced further apart; the newly available space can be filled with processing circuitry. Monolithic integration of active and passive devices on the same substrate will eliminate difficult and time consuming alignments between discreet planes of discreet devices.

It is hoped that this work will provide further impetus for resurgence of this field. Further the microlenses can be used for other micro-optics applications as well. Since the objective and the microlenses are circular in shape, a similar shape for the detector is preferred. The microlens is an important topic for imaging sensors. Our suggestion for further study includes: aberration allowances, image, energy distribution, image quality evaluation, modular transfer function, anti-reflection coating and monolithic fabrication.

APPENDIX A

PHOTOLITHOGRAPHY

A.1 Introduction

The basic steps of the lithographic process are shown in the figure. The photoresist (PR) is applied as a thin film to the substrate(e.g. SiO_2 on Si), and subsequently exposed through a mask. The mask contains clear and opaque features that define pattern to be created in the PR layer. The areas in the PR exposed to light are made either soluble or insoluble in a specific solvent known as developer. In the case when irradiated (exposed) regions are soluble, a positive image of the mask is produced in the resist. Such material is therefore termed a positive photoresist. On the other hand, if the non irradiated regions are dissolved by the developer, a negative image results. Hence the resist is termed a negative resist. Following development, the regions of SiO_2 no longer covered by resist, are removed by etching, thereby replicating the mask pattern in that oxide layer.

The resist is seen to perform two roles in this process. First, it must respond to exposing radiation in such a way that mask image can be replicated in the resist. Second, the remaining areas of resist must protect the underlying substrate during subsequent processing. In fact the name resist evolved from the ability to resist etchants.

Although both negative and positive resists are used to manufacture semiconductor components, the higher resolution capabilities of positive resists have virtually made them exclusive choice. Conventional positive optical lithographic processes and resists are capable of producing images on VLSI substrates

with dimensions as small as 0.8-1.5μm. For submicron features, however, diffraction effects during exposure may ultimately cause other higher resolution techniques to replace optical lithography

A.2 Description of Lithographic Process

The first step in this process is the application of photoresist. The photoresist is applied by spin coating technique. This procedure involves three stages : a)dispensing the resist solution onto the wafer; b) accelerating the wafer to the final rotational speed; and c) spinning at a constant speed to establish the desired thickness (and to dry the film).

The dispensing stage can either be accomplished by flooding the entire wafer with resist solution before the beginning the spinning, or by dispensing a smaller volume of resist solution at the center of the wafer and spinning at lower speeds to produce a uniform liquid layer across the wafer.

In the next stage the wafers are normally accelerated as quickly as is practical to the final spin speed and finally spinning at the constant speed to obtain desired thickness.

In this work the rotational speed was maintained at 1500 rpm. The wafers were spun at this speed for a period of 20 seconds. This gave a photoresist of 2μm thickness. Prior to exposure the wafers are baked for one minute at 115°C or for a period of 20 minutes in an air oven maintained at the same temperature in order to remove the moisture present. The baking is done to remove the moisture from the wafer. Moisture can reduce the adhesion.

The exposure was carried out using a SUSS MA6 mask aligner. The lamphouse is equipped with a 350 W mercury high pressure lamp and a SUSS diffraction reducing

optics The usable wavelength falls between 350-450 nm The lamphouse has an ellipsoidal mirror, and a 45° cold light mirror The type of exposure lamp depends on the optical range selected. The cold light mirror reflects the desired short wavelength UV light through a fly's lens and transmits the longer wavelengths to a heat sink located in the bottom of the lamphouse. The lamphouse also contains a condenser lens, diffraction reducing lens plates, a 45° turning mirror and a collimation lens. A holder is provided in the mirror house for a filter. SUSS diffraction reducing exposure system provides a high resolution over the entire exposure area, resulting in steep resist edges and small diffraction effects.

The wafers were exposed for 20 seconds in the SUSS MA6 mask aligner. After the exposure the wafer must undergo "development" in order to leave behind the image which will serve as a mask for etching. The developer is poured on the wafer and allowed to develop for 30 second before it is spun at a high rpm(~2000-3000). This procedure is repeated for another 10 seconds of development. The wafer is then washed with DI water and spun again to remove all the water. The wafers are baked as before to rid of the moisture that may been absorbed by the substrate. The windows are then inspected under the microscope for their integrity.

APPENDIX B

ETCHING

B.1 Introduction

In general etching process is not completely attainable. That is etching process are not capable of transferring the pattern established by protective mask into the underlying material. Degree to which the process fail to satisfy the ideal is specified by two parameters: bias and tolerance. *Bias* is the difference between the etched image and mask image. *Tolerance* is a measure of statistical distribution of bias values that characterizes the uniformity of etching.

The rate at which material is removed from the film by etching is known as etch rate. The units of *etch rate* are Å/min, μm/min, etc. Generally high etch rates are desirable as they allow higher production throughputs, but in some cases high etch rates make the control of lateral etching a problem. That is since material removal can occur in both horizontal and vertical directions, the horizontal etch rate as well as vertical etch rate may need to be established in order to characterize an etching process. The lateral etch ratio, L_R, is defined as the ratio of the etch rate in a horizontal direction to that in a vertical direction. Thus:

$$L_R = \frac{\text{Horizontal etch rate of material}}{\text{Vertical etch rate of material}}$$

In the case of an ideal etch process the mask pattern would be transferred to the underlying layer with a zero bias. This would then create a vertical edge of the mask

Therefore the lateral etch rate would also have to have been zero. For nonzero L_R, the film material is etched to some degree under the mask and this effect is called undercut. When the etching proceed in all directions at the same rate, it is said to be *isotropic*.

By definition, however, any etching that is not isotropic is anisotropic. If etching proceeds exclusively in one directions (e.g. only vertically), the etching process is said to be completely *anisotropic*. A typical anisotropic etch profile is shown in the figure.

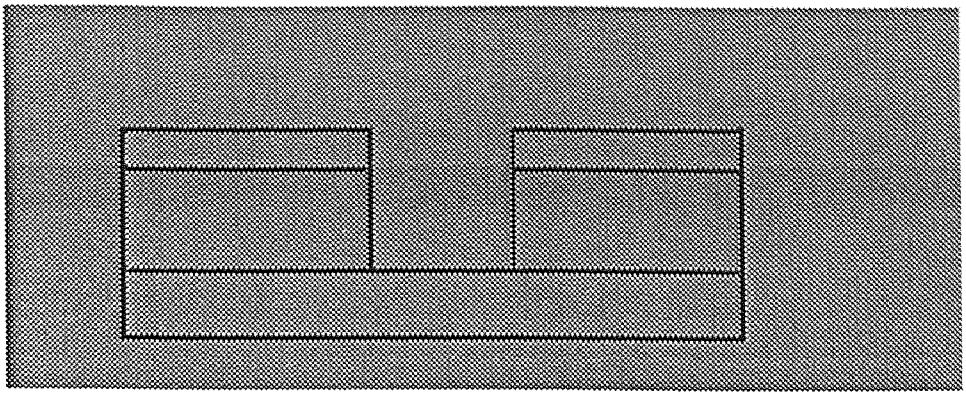


Figure B.1 Anisotropic etch profile

So far it has been assumed that the mask is not attacked by the etchant and did not consider that the layers under the etched film can also be attacked by the etchant. In fact both the mask and the underlying layer materials are generally etchable, and these effects may play a significant role in specifying etch processes. The underlying material subject to attack may either be the silicon wafer itself, or a film grown or deposited during a previous fabrication step. The ratio of the etch rates of different materials is known as *selectivity of an etched process*. Thus both the selectivity with respect to the mask material ands the selectivity with respect to the substrate materials are important characteristics of an etch process.

B.2 Wet Etching Technology

Wet etching processes are generally isotropic. They are inadequate for defining features less than 3μm. Nevertheless for those processes that involve patterning of linewidths greater than 3μm, wet etching continues to b a viable technology.

The reason wet etching has found widespread acceptance in microelectronic fabrication is that it is a low cost, reliable, high throughput process with excellent selectivity for most etch process with respect to both mask and substrate materials.

In general wet etch processes can be broken down into three steps:

- diffusion of the reactant to the reacting surface
- reaction
- diffusion of reaction products from the surface.

The second step can obviously be further differentiated into adsorption prior to, and desorption subsequent to, the actual reaction step. The slowest of the steps will be rate controlling. That is, the rate of that step will be the rate of the overall reaction.

Chemical etching can occur by several processes. The simplest involves dissolution of the material in a liquid solvent without any change in the chemical nature of the dissolved species. Most etching process, however, involve one or more chemical reactions. Various types of reactions my take place, although one commonly encountered in semiconductor fabrication is oxidation-reduction (redox). That is, a layer of oxide is formed, then the oxide is dissolved and the next layer of oxide is formed, etc.(e.g wet etching of Si and Al)

In semiconductor applications, wet etching is used to produce patterns on the silicon substrate or in thin films A mask is typically used to protect desired surface regions from the etchant and this mask is stripped after the etching has been performed Thus, when choosing a wet etch process, in addition to selecting an etchant, a suitable masking material must be picked to have good adhesion to the underlying films, good coating integrity and ability to withstand attack by etchant. Photoresist is the most commonly encountered masking layer, but sometimes it falls short in this role Problems involved include loss of adhesion at the edge of the mask-film interface due to etchant attack, and large area failure of the resist. Large area failures of the resist are usually due to differential stress buildups in the substrate and mask layers. Also bubble formation during etching process can lead to poor pattern definition, particularly at the pattern edges.

B.3 Dry Etching

Wet etching processes are typically isotropic, therefore if the thickness of the film being etched is comparable to the minimum pattern dimension, undercutting due to isotropic etching becomes intolerable. One alternative pattern transfer method that offers the capability of non isotropic(or anisotropic) etching is "dry etching". As a result, considerable effort has been expended to develop dry etch processes as replacements for wet etch processes.

The overall goal of an etch process, as mentioned earlier, is to be able to reproduce the features on the mask with fidelity. This should be achievable together with control of following aspects of etched features:

- the slope of the feature sidewalls(e.g. the slope of the sidewalls of the etched feature should have the desired angle, in some cases vertical)
- the degree of undercutting(i.e. usually the less undercutting the better)

There are a variety of dry etch processes. The mechanism of etching in each type of process can have a physical bias(e.g. glow-discharge sputtering), a chemical bias(e.g. plasma etching), or a combination of the two(e.g. reactive ion etching, RIE, and reactive ion beam etching RIBE)

In processes that rely predominantly on the physical mechanism of sputtering(including RIBE), the strongly directional nature of the incident energetic ions allows substrate material to be removed in a highly anisotropic manner(i.e. essentially vertical etch profiles are produced). Unfortunately such material mechanisms are non selective against both masking material and materials underlying the layers being etched. That is, the selectivity depends largely on sputter yield differences between materials. On the other hand purely chemical mechanisms for etching can exhibit very high selectivity against both mask and underlying substrate material. Such purely chemical etching mechanisms, however, typically etch in an isotropic fashion.

By adding a physical component to a purely chemical etching mechanism, however the shortcomings of both sputter based and purely chemical dry etching process can be surmounted. Plasma etching process is a purely chemical process and reactive ion etching processes is a physical/chemical process.

The basic concept of plasma etching is rather direct. A glow discharge is utilized to produce chemically reactive species from a relatively inert molecular gas. The etching gas is chosen so as to generate species, which react chemically with the material to be etched,

and whose reaction product is volatile. An ideal dry etch process based solely on chemical mechanisms for material removal, can thus be broken down into six steps

- reactive species are generated in a plasma
- these species diffuse to the surface of the material being etched
- the species are adsorbed on the surface
- a chemical reaction occurs with the formation of a volatile by product
- the by product is desorbed from the surface
- the desorbed species diffuse into the bulk of the gas

If any of these steps fail to occur, the overall etch process ceases. Many reactive species can react rapidly with a solid surface, but unless the product has a reasonable vapor pressure so that desorption occurs, no etching takes place. Reactive ion etching as described before is an anisotropic etching technique. After the lithographic step, windows are formed on the photoresist layer. The silicon nitride is exposed in these windows. RIE is carried out to remove this silicon nitride and expose the underlying silicon substrate.

B.4 Description of the Reactor for RIE

Plasma etching systems consist of several components: a) an etching chamber, that is evacuated to reduced pressures; b) a pumping system for establishing and maintaining the reduced pressure; c) pressure gauges to monitor the pressure in the chamber; d) a variable conductance between the pump and etching chamber so that the pressure and flow rate in the chamber can be controlled independently; e) an RF power supply to create the glow discharge; f) a gas handling capability to meter and control the flow of reactant gases; and

g) electrodes. There are several types of commercially available etching systems. They include

1 barrel reactors

2 "downstream" etchers

3 parallel-electrode(planar) reactor etchers

4 stacked parallel-electrode etchers

5 hexode batch etchers

6 magnetron ion etchers

The RIE system in the class 10 clean room, where the fabrication of the V grooves was carried out, is a stacked parallel electrode etching system.

The stacked parallel electrode etcher is a small batch machine capable of handling 6 wafers at a time. Its unique design provides an individual pair of electrodes for each wafer thereby combining some of the advantages of a single wafer and batch etchers. Operating chamber pressures and RF power densities can be kept in the ranges between those of low pressure, low power density hexode batch etchers, and high pressure.

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