High-performance matrix multiplication on Intel and FPGA platforms

Gang Li
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Matrix multiplication is at the core of high-performance numerical computation. Software methods of accelerating matrix multiplication fall into two categories. One is based on calculation simplification. The other one is based on increasing the memory access efficiency. Also matrix multiplication can be accelerated using vector processors. In this investigation, various matrix multiplication algorithms and the vector-based hardware acceleration method are analyzed and compared in terms of performance and memory requirements. Results are shown for Intel and Xilinx FPGA platforms. They show that when the CPU is fast, Goto’s algorithm runs faster than Strassen’s algorithm because the data access speed is the bottleneck in this case. On the contrary, when the CPU is slow, Strassen’s algorithm runs faster because the computation complexity becomes the key factor in this case. Also, the results show that SIMD platforms, such as Intel Xeon and SIMD extensions and an in-house developed VP (Vector co-Processor), for an FPGA, can accelerate matrix multiplication substantially. It is even shown that the VP runs faster than MKL (Intel’s optimized Math Kernel Library). This is because not only can the VP take advantage of larger vector lengths but it also minimizes inherent hardware overheads.
HIGH-PERFORMANCE MATRIX MULTIPLICATION
ON INTEL AND FPGA PLATFORMS

by
Gang Li

A Thesis
Submitted to the Faculty of
New Jersey Institute of Technology
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Master of Science in Computer Engineering

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May 2012
HIGH-PERFORMANCE MATRIX MULTIPLICATION ON INTEL AND FPGA PLATFORMS

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To my parents and Yayun.
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CHAPTER 1
INTRODUCTION

The objective of this thesis is to present high-performance matrix multiplication algorithms and a relevant hardware acceleration method. Software methods of accelerating matrix multiplication fall into two categories. One is based on calculation simplification. The other one is based on increasing memory access efficiency. The hardware acceleration is done by using an in-house built vector co-processor for FPGAs.

Strassen’s algorithm is a typical algorithm based on calculation simplification. Strassen’s algorithm has complexity \( O(n^{2.807}) \) [1] [5] for \( n \times n \) matrices. It is a recursive algorithm. First, the input matrix is divided into four sub-matrices for independent multiplications, then recursively into sixteen sub-matrices, etc. But this by itself does not reduce the time complexity which is still \( O(n^3) \). However, Strassen found a way to also reduce the complexity of single sub-matrix multiplication. Thus, the time complexity is reduced to \( O(n^{2.807}) \). The Coppersmith-Winograd algorithm has a time complexity of \( O(n^{2.3737}) \) [4]. However, this algorithm has a very large constant, so it is only useful for the multiplication of extremely large matrices. The lower bound is \( O(n^2) \), i.e., the same as the number of elements in the product.

A block-based matrix multiplication method is based on increasing memory access efficiency. It calculates the resulting matrix block by block instead of line by line (row or column), most of the time, in order to keep the data needed small enough to fit in the cache and thus take advantage of cache hits.
Besides elaborately identifying blocks in the matrix, the Goto’s method [2] increases the memory access efficiency further by copying the most frequently used data into contiguous memory locations in order to reduce the TLB misses.

MKL is the Math Kernel Library developed by Intel [10]. It heavily uses the Intel architecture’s SSE instruction extensions to do the computations in parallel in the SIMD (Single Instruction Multi Data) mode.

The vector processor is an efficient implementation of an SIMD architecture for array operations. It can simultaneously execute the same operation, e.g. single-precision floating-point multiplication, on all the elements in an array.

The rest of the thesis introduces the details of the studied algorithms or methods and presents their implementations on Intel and FPGA platforms. Then, it compares the results.
CHAPTER 2
BRUTE-FORCE IMPLEMENTATION

Brute-force matrix multiplication (MM) is implemented exactly according to the matrix multiplication definition. It is simple and straightforward and provides a baseline in order to facilitate comparisons with other MM algorithms.

2.1 Introduction
The definition of matrix multiplication is: for N * N matrices A and B, the result of their multiplication is matrix C whose elements are:

\[ C[i][j] = \sum_{k=0}^{N-1} A[i][k] \times B[k][j] \]

for i, j = 0, … , N-1

It could be easily implemented using there nested for loops as follows:

```c
for( i = 0; i < N; i++ )
    for( j = 0; j < N; j++ ) {
        sum=0;
        for( k = 0; k < N; k++ )
            sum += A[i][k] * B[k][j];
        C[i][j] = sum;
    }
```

The process of calculating the result is shown in Figure 2.1 for 6 by 6 matrices. Each square represents an element of a matrix. Each element of C is calculated by multiplying corresponding elements from one row of A with one column of B.
2.2 Analysis

2.2.1 Time Complexity

To calculate one element of C, there are N multiplications and N additions. In total, there are \(N^3\) multiplications and \(N^3\) additions. So the time complexity of calculating matrix C is \(O(N^3)\).

2.2.2 Cache Performance

Consider only cache capacity misses and compulsory misses for simplifying the analysis (i.e. ignore conflict misses). Capacity misses are those misses that occur regardless of the associativity or the block size, solely due to the finite size of the cache. Compulsory misses are those misses caused by the first reference to a datum. Conflict misses are those misses that could have been avoided, had the cache not evicted an entry earlier.

For the Brute-force implementation, Table 2.1 shows the absolute cache miss numbers for various cache sizes. An explanation for cache size > \((L+1)N\) follows as an example. In this case, one row of A and L columns of B could be held in the cache. In
order to calculate one row of C, a row of A is repeatedly accessed and there are \(N/L\) misses. So to calculate the whole matrix C, there will be \(N^2/L\) misses. At the same time, when calculating one row of C, \(N^2/L\) misses will occur for scanning the whole matrix B. So to calculate the whole matrix C, there will be \(N^3/L\) misses.

As for the cache organization, if it is directly mapped, there will be more cache conflict misses than in the case of set associative.

**Table 2.1** Cache Miss Numbers of Brute-force Implementation for Various Cache Sizes (in Number of Elements)

<table>
<thead>
<tr>
<th>Cache Size</th>
<th>Matrix Size</th>
<th>&gt; (N+1)N</th>
<th>&gt; (L+1)N</th>
<th>&gt; (N+L)</th>
<th>&gt;2L</th>
<th>0</th>
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<td>A</td>
<td>N^2/L</td>
<td>N^2/L</td>
<td>N^2/L</td>
<td>N^3/L</td>
<td>N^3</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>N^2/L</td>
<td>N^3/L</td>
<td>N^3</td>
<td>N^3</td>
<td>N^3</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>N^2</td>
<td>N^2</td>
<td>N^2</td>
<td>N^2</td>
<td>N^2</td>
<td></td>
</tr>
<tr>
<td>Subtotal</td>
<td>N^2 + 2N^2/L</td>
<td>N^2 + N^3/L + N^2/L</td>
<td>N^3 + N^2/L + N^2/L</td>
<td>N^3 + N^2 + N^3/L</td>
<td>2N^3 + N^2</td>
<td></td>
</tr>
</tbody>
</table>

**2.2.3 Memory Consumption**

In terms of memory consumption, the Brute-force implementation does not need extra memory but just memory to store the three matrices; this requires the storage of \(3N^3\) elements.


2.3 Results

2.3.1 Intel Xeon Platform

The specifications of the Intel platform are shown in Table 2.2. It has a dual-core CPU and each core has two threads. In order to analyze the algorithms, only one thread is used.

The running time of the implementation for various matrix sizes is shown in Table 2.3. This shows how much more time is needed for the calculation when N doubles. The time complexity is $O(N^3)$, but Table 2.3 shows that the slowdown is not always 8 when N doubles. This is because the cache performance and the constants in the complexity affect the time spent.

**Table 2.2** The Specifications of the Intel Xeon Platform

<table>
<thead>
<tr>
<th>CPU</th>
<th>Xeon 3.20G Hz * 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>3GB</td>
</tr>
<tr>
<td>L1 cache</td>
<td>16KB, 8-way 64-byte line size</td>
</tr>
<tr>
<td>L2 cache</td>
<td>1024KB, 8-way 64-byte line size</td>
</tr>
<tr>
<td>Compiler</td>
<td>Intel c/c++ compiler</td>
</tr>
<tr>
<td>Compile option</td>
<td>-OD(optimization disabled)</td>
</tr>
</tbody>
</table>

**Table 2.3** Execution Time (in Seconds) of the Brute-force Implementation on the Intel Xeon Platform

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Spent (sec)</td>
<td>0.002336</td>
<td>0.029708</td>
<td>0.253991</td>
<td>2.684</td>
<td>63.753</td>
<td>537.389</td>
</tr>
<tr>
<td>Slowdown</td>
<td>NA</td>
<td>12.717</td>
<td>8.549</td>
<td>10.608</td>
<td>23.752</td>
<td>8.429</td>
</tr>
</tbody>
</table>
When \( N \leq 64 \), matrix B could fully fit in the L1 cache (16KB). The cache misses become \( N^2 + 2N^2/L \). If \( N \) is larger than 64, the cache misses are \( N^2 + N^2/L + N^3/L \). That is why the slowdown for \( N = 128 \) is larger than 8.

When \( N=128 \) or 256, matrix B could fit in L2 cache, therefore the cache miss rate for \( N=128 \) or 256 are similar. In this case the slowdown is depended on computation complexity, thus the slowdown for \( N=256 \) is close to 8.

When \( N=512 \), the L2 cache could exactly hold matrix B (no more place for one row of matrix \( A \)), this makes the L2 cache miss rate higher than in the case of \( N=256 \). So the slowdown is slightly higher than 8.

When \( N \geq 1024 \), the L2 cache (1024KB) is not large enough to hold matrix B, so the cache miss rate increases. This causes the slowdown (23.752) for \( N = 1024 \) to be larger than 8. And because the speed gap between the L2 cache and main memory is wide, the slowdown (23.752) is so large.

2.3.2 Xilinx ML501 FPGA Platform

The platform’s specifications are shown in Table 2.4. The Xilinx MicroBlaze processor was used. It contains the XC5VLX50 FPGA and runs at 125 MHz.

Table 2.4 The Specifications of the Xilinx FPGA Platform

<table>
<thead>
<tr>
<th>CPU</th>
<th>Microblaze 125MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>256MB</td>
</tr>
<tr>
<td>L1 cache</td>
<td>8KB, 1-way 32-byte line size</td>
</tr>
<tr>
<td>Compiler</td>
<td>GNU c compiler</td>
</tr>
<tr>
<td>Compile option</td>
<td>-OD(optimization disabled)</td>
</tr>
</tbody>
</table>
The running time of the implementation for various matrix sizes is shown in Table 2.5.

**Table 2.5** Execution Time (in Seconds) of the Brute-force Implementation on the Xilinx FPGA Platform

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Spent (sec)</td>
<td>0.105</td>
<td>0.841</td>
<td>6.717</td>
<td>53.664</td>
<td>429.12</td>
</tr>
<tr>
<td>Slowdown</td>
<td>NA</td>
<td>8.009</td>
<td>7.986</td>
<td>7.989</td>
<td>7.996</td>
</tr>
</tbody>
</table>

It is shown that the slowdowns are all close to 8. This is because the cache (8KB) is too small to hold even the 64 by 64 matrix, which means that for all the cases the cache performance is quite similar. Thus, the slowdown is depended on the computation complexity.
CHAPTER 3

BASIC BLOCK-BASED IMPLEMENTATION

The Brute-force implementation repeatedly accesses the whole matrix B, column by column. If matrix B cannot fit in the cache, the cache miss rate increases. The cost of the cache is much higher than that of the memory, so it cannot be too large. The basic Block-based method provides a way to access matrix B block by block instead of scanning the whole matrix. In this way, a small cache could hold all the needed data in each iteration, therefore the cache miss rate decreases even when the matrices are large.

3.1 Introduction

The chosen Block-based implementation calculates one row of C part by part. The process is rather complicated and it will be shown in pictures in the following discussion.

The basic Block-based algorithm implementation [1] in the C language is:

```c
for (jj=0; jj<N; jj=jj+K)
    for (kk=0; kk<N; kk=kk+K)
        for (i=0; i<N; i=i+1)
            for (j=jj; j<min(jj+K,N); j++) {
                sum=0.0;
                for (k=kk; k<min(kk+K,N); k++)
                    sum+=A[i][k] * B[k][j];
                C[i][j] += sum;
            }
```

There are five “for loops” assuming blocks of size K*K. The following pictures illustrate the process for 6 * 6 matrices.
3.1.1 Calculating the First Three Columns of C

In the first iteration:


Calculating a part of the first row of C is shown in Figure 3.1. A light shade means an older access and a dark shade means a current access.

![Figure 3.1](image1.png)

**Figure 3.1** Calculating a part of the first three elements of the first row of matrix C.

The elements accessed in the whole iteration are shown in Figure 3.2.

![Figure 3.2](image2.png)

**Figure 3.2** The first iteration of calculating the first three columns of matrix C. White means the data has not been accessed; light gray means completed accesses.

After the shown iteration, the calculation of the first 3 columns of C is not completed yet. Only one “layer” of the calculation is finished, which means that only some summations have been completed.

In the second iteration:


Calculating a part of one row of C is shown in Figure 3.3.
3.1.2 Calculating the Other Three Columns of C

In the first iteration:


In the second iteration:

3.2 Analysis

3.2.1 Time Complexity

There are five “for” loops in this implementation.

\[
\text{Total number of multiplications} = \frac{N}{K} \times \frac{N}{K} \times N \times K \times K
\]

\[= N^3\]

where \( K \times K \) is the block size in matrix B used in each iteration.

So the time complexity of the basic Block-based implementation is \( O(N^3) \).

3.2.2 Cache Performance

When \( K < L \) (cache line size), the data stored in the cache will not be fully used, which is not efficient and will not be discussed here.

When \( K \geq L \), Table 3.1 shows the cache misses for different scenarios.

Take the case of cache size \( > (2NK+K^2) \) as an example to explain the cache misses. In this case, \( K \) columns of matrices C and A as well as \( K^2 \) elements of matrix B can be in the cache. To calculate \( K \) columns of matrix C, the cache misses are

\[\left(\frac{K}{L}\right) \times N = \frac{NK}{L}\]
There are $N/K$ calculations of this type to produce the whole matrix $C$, so the cache misses are

$$(NK/L) * N/K = N^2/L$$

**Table 3.1** Cache Miss Numbers of Basic Block-based Implementation for Various Cache Sizes (in Number of Elements)

<table>
<thead>
<tr>
<th>Cache Size</th>
<th>Matrix Size</th>
<th>$&gt;(2NK+K^2)$</th>
<th>$&gt;K^2+2K$</th>
<th>$&gt;K^2+K$</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>$N^2/L$</td>
<td>$N^3/KL$</td>
<td>$N^3/KL$</td>
<td>$N^3$</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>$N^2/L$</td>
<td>$N^2/L$</td>
<td>$N^2/L$</td>
<td>$N^3$</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>$N^2/L$</td>
<td>$N^3/KL$</td>
<td>$N^3/K$</td>
<td>$N^3/K$</td>
<td></td>
</tr>
</tbody>
</table>

3.2.3 Memory Consumption

No extra memory is needed other than storing matrices A, B and C, so the storage needed is $3N^3$.

3.3 Results

3.3.1 Intel Xeon Platform

Table 3.2 shows the time needed for calculating matrices of various sizes for the basic Block-based implementation.

The cache line size is 64 bytes. One cache line stores 16 floating point numbers. As discussed above, when $K < L$ memory accesses are less efficient. This is verified in Table 3.2.
Table 3.2 Execution Time (in Seconds) of the Basic Block-based Implementation on the Intel Xeon Platform

<table>
<thead>
<tr>
<th>Block Size</th>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.004130</td>
<td>0.051724</td>
<td>0.298041</td>
<td>2.895</td>
<td>36.908</td>
<td>297.644</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>0.004972</td>
<td>0.029490</td>
<td>0.253050</td>
<td>2.102</td>
<td>19.530</td>
<td>157.101</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>0.002773</td>
<td>0.040463</td>
<td>0.236596</td>
<td>1.817</td>
<td>15.030</td>
<td>120.654</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>0.002677</td>
<td>0.043091</td>
<td>0.227063</td>
<td>1.683</td>
<td>13.470</td>
<td>108.300</td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>0.002651</td>
<td>0.037837</td>
<td>0.206537</td>
<td>1.572</td>
<td>15.737</td>
<td>126.023</td>
<td></td>
</tr>
</tbody>
</table>

As shown in Table 3.2, for large matrices the calculation is the most efficient for block sizes 32*32. Table 3.3 takes this case as an example to further illustrate the effect of the cache as a function of the matrix size.

Table 3.3 Execution Time (in Seconds) of the Basic Block-based Implementation on the Intel Xeon for K=32

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Spent (sec)</td>
<td>0.002677</td>
<td>0.043091</td>
<td>0.227063</td>
<td>1.683</td>
<td>13.470</td>
<td>108.300</td>
</tr>
<tr>
<td>Slowdown</td>
<td>NA</td>
<td>16.096</td>
<td>5.269</td>
<td>7.412</td>
<td>8.003</td>
<td>8.040</td>
</tr>
</tbody>
</table>

When N increases, less data can fit in the cache. As shown in Table 3.1, when cache size < (2NK+K^2), the cache misses will increase. For K=32 and N > 64

\[16K < 2*N*32*4 + 32*32*4\]

This is verified in Table 3.3 for N = 128, where the slowdown is much larger than 8. Compared to the Brute-force implementation for N > 256, the L1 cache could not hold (N+1)L data and cache misses increased. But in the basic Block-based implementation it is easy to hold K^2+2K data, and the cache miss rate is kept at a low level. It is verified
from Table 2.3 and Table 3.3 that, for \( N > 256 \), the basic Block-based implementation takes less time.

### 3.3.2 Xilinx ML501 FPGA Platform

Table 3.4 shows the time needed for calculating matrices of various sizes for the basic Block-based implementation on Xilinx FPGAs.

**Table 3.4** Execution Time (in Seconds) of the Basic Block-based Implementation on a Xilinx FPGA Platform

<table>
<thead>
<tr>
<th>Basic Block-Based Implementation</th>
<th>Matrix Size</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>64</td>
</tr>
<tr>
<td>4</td>
<td>0.054</td>
</tr>
<tr>
<td>8</td>
<td>0.050</td>
</tr>
<tr>
<td>16</td>
<td>0.049</td>
</tr>
<tr>
<td>32</td>
<td>0.107</td>
</tr>
</tbody>
</table>

Take \( K = 8 \) as an example. Table 3.5 shows a comparison of execution times.

**Table 3.5** Execution Time (in Seconds) of the Basic Block-based Implementation on the Xilinx FPGA Platform for \( K = 8 \)

<table>
<thead>
<tr>
<th>Basic Block-Based Implementation</th>
<th>Matrix Size</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>64</td>
</tr>
<tr>
<td>Time Spent (sec)</td>
<td>0.054</td>
</tr>
<tr>
<td>Time Ratio</td>
<td>NA</td>
</tr>
</tbody>
</table>

The slowdown converges to 8. This is because, as analyzed before, the basic block-based implementation’s time complexity is \( O(N^3) \). So when \( N \) doubles, the execution time becomes about 8 times as much.
The Goto’s implementation[3] not only decomposes the matrices into blocks in order to reduce the cache misses but also takes into account TLB misses. The results show that the Goto’s implementation has better performance than the basic Blocked-based implementation.

4.1 Introduction

4.1.1 Goto’s Block-based Method

Figure 4.1 shows all possible cases of matrix multiplication for matrices A and B having sizes m*k and k*n, respectively, according to the Goto’s classification.

<table>
<thead>
<tr>
<th>m</th>
<th>n</th>
<th>k</th>
<th>Illustration</th>
<th>Label</th>
</tr>
</thead>
<tbody>
<tr>
<td>large</td>
<td>large</td>
<td>large</td>
<td></td>
<td>GEMM</td>
</tr>
<tr>
<td>large</td>
<td>large</td>
<td>small</td>
<td></td>
<td>GEPP</td>
</tr>
<tr>
<td>large</td>
<td>small</td>
<td>large</td>
<td></td>
<td>GEMP</td>
</tr>
<tr>
<td>small</td>
<td>large</td>
<td>large</td>
<td></td>
<td>GEMP</td>
</tr>
<tr>
<td>small</td>
<td>large</td>
<td>small</td>
<td></td>
<td>GEBP</td>
</tr>
<tr>
<td>large</td>
<td>small</td>
<td>small</td>
<td></td>
<td>GEPE</td>
</tr>
<tr>
<td>small</td>
<td>small</td>
<td>large</td>
<td></td>
<td>GEPDOT</td>
</tr>
<tr>
<td>small</td>
<td>small</td>
<td>small</td>
<td></td>
<td>GEPP</td>
</tr>
</tbody>
</table>

Figure 4.1 All possible shapes of matrix multiplication [taken from 2].
Goto’s algorithm tries to find the best way to divide the matrices into blocks. All possible block-based approaches are shown in Figure 4.2.

Figure 4.2 All possible methods to break down matrix multiplication [taken from 2].
Goto’s algorithm chooses the number 2 method to implement the matrix multiplication if the matrix is stored in the row-major order.

In Figure 4.2, cases 1, 4, 5 and 6 are not TLB friendly in that there are horizontal panels (rectangle shape matrix). Every two adjacent accesses of the elements of a horizontal panel have a gap of N elements in the memory. This means, when N is large every access will cause a TLB miss if there is a cache miss first.

Now case 2 and case 3 will be compared. It is observed that, for case 2 in order to calculate a layer of C, K columns of matrix A are repeatedly accessed. This gives better cache performance especially when K columns of A could fit in the L2 cache. For case 3, the whole matrix A is accessed in each outer loop, so the chances of reducing the cache miss rate for accessing matrix A is relatively low.

4.1.2 Calculation Process for Goto’s Algorithm

First, assume the block-based decomposition of matrices A and B as shown in Figure 4.3,

\[
\begin{array}{ccc}
A1 & A2 & A3 \\
\hline
A & B & \\
\hline
B1 & \\
B2 & \\
B3 & \\
\end{array}
\]

**Figure 4.3** Block-based decomposition of matrices A and B.

Second, calculate C1 which is the first layer of summations of each element in matrix C (shown in Figure 4.4).
Third, calculate C1 block by block (shown in Figure 4.5 and Figure 4.6),

**Figure 4.5** Calculate C11.

**Figure 4.6** Calculate C12.

It is noticed that B11 is not stored in contiguous memory. By adjusting the block size, the cache miss rate could be reduced, but cache misses could not be avoided completely because of conflict and capacity misses. When a miss happens in this case, the system will access the TLB table. Because B11 is not in contiguous memory, the
possibility of having a TLB miss is high. And the cost of a TLB miss is high. Therefore, B11 is copied into contiguous memory in order to reduce cache and TLB misses.

Finally, every layer of C is accumulated to produce the result matrix C (shown in Figure 4.7).

\[
\begin{array}{c}
\text{C} \\
\end{array} = \begin{array}{ccc}
C11 & C12 & C13 \\
\end{array} + \ldots + \begin{array}{ccc}
C31 & C32 & C33 \\
\end{array}
\]

**Figure 4.7** Adding each layer of C.

### 4.2 Analysis

#### 4.2.1 Time Complexity

It is observed that the number of element multiplications is not reduced. Goto’s algorithm only changes the order of multiplications. So the time complexity of Goto’s implementation is \(O(N^3)\).

#### 4.2.2 Cache Performance

Table 4.1 shows the cache misses for various scenarios.
Table 4.1  Cache Miss Numbers of Goto’s Implementation for Various Cache Sizes (in Number of Elements)

<table>
<thead>
<tr>
<th>Cache Size Matrix Size</th>
<th>&gt; (N^2+NK+K^2)</th>
<th>&gt; NK+K^2</th>
<th>&gt; K^2+2K</th>
<th>&gt; K^2+K</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>N^2/L</td>
<td>N^2/L</td>
<td>N^3/KL</td>
<td>N^3/KL</td>
<td>N^3</td>
</tr>
<tr>
<td>B</td>
<td>N^2/L</td>
<td>N^2/L</td>
<td>N^2/L</td>
<td>N^2/L</td>
<td>N^3</td>
</tr>
</tbody>
</table>

Take the case of cache size > (K^2 + 2K) as an example to explain the cache miss calculation. In this case, K elements of C, K elements of A and K * K elements of B are in the cache. To calculate one layer of C, the cache misses for matrix B are:

\[(K^2/L) \times N/K = NK/L\]

There are N/K layers of C to be calculated, so the total number of cache misses for matrix B is:

\[(NK/L) \times N/K = N^2/L\]

4.2.3 Memory Consumption

No extra memory is needed other than storing matrices A, B and C, so the storage needed is 3N^3.
4.3 Results

4.3.1 Intel Xeon Platform

Table 4.2 shows the time needed for calculating matrices of various sizes for Goto’s implementation.

**Table 4.2** Execution Time (in Seconds) of the Goto’s Implementation on the Intel Xeon Platform

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.002912</td>
<td>0.031643</td>
<td>0.196508</td>
<td>1.492234</td>
<td>11.565</td>
<td>90.610</td>
</tr>
<tr>
<td>8</td>
<td>0.003932</td>
<td>0.022385</td>
<td>0.191102</td>
<td>1.453994</td>
<td>11.486</td>
<td>90.126</td>
</tr>
<tr>
<td>16</td>
<td>0.003226</td>
<td>0.025004</td>
<td>0.200335</td>
<td>1.466154</td>
<td>11.504</td>
<td>90.230</td>
</tr>
<tr>
<td>32</td>
<td>0.002824</td>
<td>0.022765</td>
<td>0.196912</td>
<td>1.457312</td>
<td>11.495</td>
<td>90.709</td>
</tr>
<tr>
<td>64</td>
<td>0.002831</td>
<td>0.027742</td>
<td>0.190376</td>
<td>1.445694</td>
<td>11.480</td>
<td>90.626</td>
</tr>
</tbody>
</table>

The performance is overall stable and better than that for the basic Block-based implementation. Table 4.3 shows the slowdown as a function of the matrix size for 32*32 blocks.

**Table 4.3** Execution Time (in Seconds) of the Goto’s Implementation on the Intel Xeon for K=32

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Spent</td>
<td>0.002824</td>
<td>0.022765</td>
<td>0.196912</td>
<td>1.457312</td>
<td>11.495</td>
<td>90.709</td>
</tr>
<tr>
<td>Slowdown</td>
<td>NA</td>
<td>8.061</td>
<td>8.649</td>
<td>7.400</td>
<td>7.887</td>
<td>7.891</td>
</tr>
</tbody>
</table>

The slowdown is always around 8. This is because the time complexity is O(N^3) which is analyzed in Section 4.2.1.
4.3.2 Xilinx ML501 FPGA Platform

Table 4.4 shows results for the Goto’s implementation on a MicroBlaze processor embedded in a Xilinx FPGA.

Table 4.4  Execution Time (in Seconds) of Goto’s Implementation on the Xilinx FPGA Platform

<table>
<thead>
<tr>
<th>Block Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.055</td>
<td>0.476</td>
<td>4.410</td>
<td>34.452</td>
<td>270.092</td>
</tr>
<tr>
<td>8</td>
<td>0.054</td>
<td>0.472</td>
<td>4.335</td>
<td>32.975</td>
<td>264.281</td>
</tr>
<tr>
<td>16</td>
<td>0.054</td>
<td>0.468</td>
<td>4.639</td>
<td>36.827</td>
<td>295.163</td>
</tr>
<tr>
<td>32</td>
<td>0.054</td>
<td>0.517</td>
<td>4.625</td>
<td>38.321</td>
<td>317.821</td>
</tr>
<tr>
<td>64</td>
<td>0.075</td>
<td>0.516</td>
<td>4.618</td>
<td>37.385</td>
<td>300.296</td>
</tr>
</tbody>
</table>

The performance is relatively stable and better than that of the basic Block-based implementation. Take block size = 8 as an example to examine the slowdowns in Table 4.5.

Table 4.5  Execution Time (in Seconds) of Goto’s Implementation on the Xilinx FPGA Platform for K =8

<table>
<thead>
<tr>
<th>Time Spent (sec)</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.054</td>
<td>0.472</td>
<td>4.335</td>
<td>32.975</td>
<td>264.281</td>
<td></td>
</tr>
<tr>
<td>Slowdown</td>
<td>NA</td>
<td>8.740</td>
<td>9.184</td>
<td>7.606</td>
<td>8.014</td>
</tr>
</tbody>
</table>

The slowdown is close to 8.
CHAPTER 5

STRASSEN’S IMPLEMENTATION

The previous algorithms all have time complexity of $O(N^3)$. Strassen’s algorithm has time complexity of $O(N^{2.807})$. It is a recursive algorithm and in each iteration it divides each matrix into four sub-matrices. The result will be calculated by sub-matrix multiplications.

5.1 Introduction

First, matrix multiplication could be implemented recursively. For example, A, B and C are $N*N$ matrixes and $C = A*B$.

\[
C = \begin{pmatrix}
\alpha & \beta \\
\gamma & \delta
\end{pmatrix}, \quad A = \begin{pmatrix}
a & b \\
c & d
\end{pmatrix}, \quad B = \begin{pmatrix}
e & f \\
g & h
\end{pmatrix}
\]

The sub-matrices of $C$ could be calculated using the sub-matrices of $A$ and $B$ as follows:

\[
r = ae + bg \\
s = af + bh \\
t = ce + dg \\
u = cf + dh
\]

There are 8 sub-matrix multiplications. Each multiplication is done in the same way until the sub-matrix contains only one element.

The time complexity is:

\[T(n) = 8T(N/2) + O(N^2)\]
Resolving the recurrence, it gives us:

\[ T(N) = O(N^3) \]

The time complexity of the recursive version of matrix multiplication is still \( O(N^3) \). However, Strassen found a way to reduce one sub-matrix multiplication in each iteration. The process is as follows:

1) Calculate \( s \):

\[
\begin{align*}
\text{let } P_1 &= a ( f - h ) = af - ah \\
\text{let } P_2 &= ( a + b ) h = ah + bh \\
s &= P_1 + P_2 = af + bh
\end{align*}
\]

2) Calculate \( t \):

\[
\begin{align*}
\text{let } P_3 &= ( c + d ) e = ce + de \\
\text{let } P_4 &= d ( g - e ) = dg - de \\
t &= P_3 + P_4 = ce + dg
\end{align*}
\]

3) Calculate \( r \):

\[
\begin{align*}
\text{let } P_5 &= ( a + d ) ( e + h) = ae + ah + de + dh \\
\text{let } P_6 &= ( b - d ) ( g + h ) = bg + bh - dg - dh \\
r &= P_5 + P_4 - P_2 + P_6 = ae + bg
\end{align*}
\]

4) Calculate \( u \):

\[
\begin{align*}
\text{let } P_7 &= ( a - c ) ( e + f) = ae + af - ce - cf \\
u &= P_5 + P_1 - P_3 - P_7 = cf + dh
\end{align*}
\]

P1 to P7 are intermediate sub-matrices. They are produced by 7 sub-matrix multiplications.

The process is shown in Figure 5.1 to Figure 5.3.
Figure 5.1 Sub-matrices of A and B.

Seven intermediate sub-matrices are produced:

<table>
<thead>
<tr>
<th></th>
<th>P1</th>
<th>P2</th>
<th>P3</th>
<th>P4</th>
<th>P5</th>
<th>P6</th>
<th>P7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>a(f-h)</td>
<td>(a+b)h</td>
<td>(c+d)e</td>
<td>d(g-e)</td>
<td>(a-d)(e+h)</td>
<td>(b-d)(g+h)</td>
<td>(a-c)(e+f)</td>
</tr>
</tbody>
</table>

Figure 5.2 Calculate intermediate sub-matrices P1 to P7.

To calculate the result matrix C:

C:

<table>
<thead>
<tr>
<th></th>
<th>P3 + P4</th>
<th>P5 + P4 - P2 + P6</th>
<th>P1 + P2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>P3 + P4</td>
<td>P5 + P1 - P3 - P7</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5.3 Calculate matrix C from sub-matrices P1 to P7.
5.2 Analysis

5.2.1 Time Complexity

There are seven multiplications of sub-matrices in each iteration, so

\[ T(N) = 7T(N/2) + O(N^2) \]

Resolving the recurrence, we get

\[ T(N) = O(N^{\lg 7}) = O(N^{2.807}) \]

5.2.2 Cache Performance

It is observed from the process followed by Strassen’s algorithm that the memory accesses are quite scattered, so the cache performance is not good.

5.2.3 Memory Consumption

Strassen’s is a recursive algorithm. In iteration i, except the last one, it needs 17 intermediate \( N/2^i \) by \( N/2^i \) matrices. When the function returns, the intermediate memory will be freed. There are \( \log_2^{N/K} \) iterations. Therefore, the memory needed could be calculated as follows:

\[
\text{Memory} = 3N^2 + 17((N/2)^2 + (N/4)^2 + \ldots + K^2)
\]

\[ = 3N^2 + (17N^2/3)(1-(K/N)^2) \]

(in elements)

When \( K/N \) is small:

\[ \text{Memory} = 3N^2 + (17N^2/3) \]

\[ = 8.7 \times N^2 \]

So it needs 2.9 times the memory of the previous algorithms.
5.2.4 Disadvantages

Strassen’s algorithm does not have stable performance. If $N$ is not a power of 2, matrices $A$, $B$ and $C$ will be padded to make their sizes powers of 2. This means extra memory and computing time. In the worst case, $N$ increases by 1, the computing complexity increases six times and the memory consumption increases three times.

5.3 Results

In the actual implementation, it was found that it is inefficient for the algorithm to go recursively down to a sub-matrix with one element. So a minimum block size is defined. If the sub-matrix is smaller than the minimum block, the matrix multiplication is implemented using the Brute-force algorithm. Various minimum block sizes were tried and the performance of the algorithm is shown in the following sections.

5.3.1 Intel Xeon platform

Table 5.1 shows the time needed for calculating matrices of various sizes for Strassen’s algorithm.

<table>
<thead>
<tr>
<th>Block Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.007765</td>
<td>0.058314</td>
<td>0.389617</td>
<td>2.702897</td>
<td>19.372</td>
<td>132.834</td>
</tr>
<tr>
<td>8</td>
<td>0.004404</td>
<td>0.038448</td>
<td>0.251321</td>
<td>1.708744</td>
<td>11.963</td>
<td>82.893</td>
</tr>
<tr>
<td>16</td>
<td>0.003736</td>
<td>0.027557</td>
<td>0.213323</td>
<td>1.461209</td>
<td>10.102</td>
<td>70.350</td>
</tr>
<tr>
<td>32</td>
<td>0.005010</td>
<td>0.037459</td>
<td>0.202927</td>
<td>1.416484</td>
<td>10.004</td>
<td>69.778</td>
</tr>
<tr>
<td>64</td>
<td>0.004127</td>
<td>0.028823</td>
<td>0.208687</td>
<td>1.499320</td>
<td>10.429</td>
<td>72.877</td>
</tr>
</tbody>
</table>
The performance is better than Goto’s algorithm. Take block size = 32 as an example to examine the figures for slowdowns and memory consumptions, as shown in Table 5.2.

**Table 5.2** Execution Time (in Seconds) of the Strassen’s Implementation on the Intel Xeon for K=32

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Spent (sec)</td>
<td>0.005010</td>
<td>0.037459</td>
<td>0.202927</td>
<td>1.416484</td>
<td>10.004</td>
<td>69.778</td>
</tr>
<tr>
<td>Slowdown</td>
<td>-</td>
<td>7.476</td>
<td>5.417</td>
<td>6.980</td>
<td>7.062</td>
<td>6.975</td>
</tr>
<tr>
<td>Memory Consumption</td>
<td>-</td>
<td>-</td>
<td>1.084M</td>
<td>6.876M</td>
<td>31.120M</td>
<td>121.8M</td>
</tr>
<tr>
<td>Size of three Matrices</td>
<td>-</td>
<td>-</td>
<td>0.768M</td>
<td>3M</td>
<td>12M</td>
<td>48M</td>
</tr>
<tr>
<td>Memory Expansion</td>
<td>-</td>
<td>-</td>
<td>1.41</td>
<td>2.29</td>
<td>2.59</td>
<td>2.54</td>
</tr>
</tbody>
</table>

The slowdown is close to 7 independent of the matrix size. It is consistent with the time complexity of O(N^2.807).

The memory expansion is defined as follows:

\[
\text{Memory expansion} = \frac{\text{Memory consumption}}{\text{Size of three matrices}}
\]

The memory expansions observed in Table 5.2 have values close to but less than the theoretical 2.9. This is because the calculation in the previous section does count other memory consumptions, like local variables.
5.3.2 Xilinx ML501 FPGA Platform

Table 5.3 shows the time needed for calculating matrices of various sizes with Strassen’s algorithm.

**Table 5.3** Execution Time (in Seconds) of Strassen’s Implementation on the Xilinx FPGA Platform

<table>
<thead>
<tr>
<th>Block Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0.074</td>
<td>0.560</td>
<td>4.069</td>
<td>29.075</td>
<td>210</td>
</tr>
<tr>
<td>8</td>
<td>0.056</td>
<td>0.436</td>
<td>3.202</td>
<td>23.011</td>
<td>170</td>
</tr>
<tr>
<td>16</td>
<td>0.053</td>
<td>0.410</td>
<td>3.038</td>
<td>21.855</td>
<td>155</td>
</tr>
<tr>
<td>32</td>
<td>0.052</td>
<td>0.441</td>
<td>3.234</td>
<td>23.224</td>
<td>165</td>
</tr>
<tr>
<td>64</td>
<td>0.127</td>
<td>0.935</td>
<td>6.691</td>
<td>51</td>
<td>334</td>
</tr>
</tbody>
</table>

The performance is better than Goto’s algorithm.

When the block size is 16*16, the slowdowns are shown in Table 5.4.

**Table 5.4** Execution Time (in Seconds) of Strassen’s Implementation on the Xilinx FPGA Platform for K=16

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Spent (sec)</td>
<td>0.053</td>
<td>0.410</td>
<td>3.038</td>
<td>21.855</td>
<td>155</td>
</tr>
<tr>
<td>Slowdown</td>
<td>NA</td>
<td>7.735</td>
<td>7.409</td>
<td>7.193</td>
<td>7.092</td>
</tr>
</tbody>
</table>

The slowdown is always close to 7. It is consistent with the theoretical analysis.
CHAPTER 6
MKL IMPLEMENTATION

6.1 Introduction

MKL is Intel’s Math Kernel Library [10]. It is an optimized library for math. There are several aspects of optimization.

1) Multithreading. MKL puts emphasis on multithreaded optimization for multicores.

2) SIMD instructions. Execute in parallel using Intel’s SIMD instruction extensions (SSE) which operate on eight 128-bit vector registers.

3) Assembly. Writing kernel functions in assembly. Carefully arrange instructions to reduce stalls.

4) Cache. Increase cache performance by blocking in order to improve both the spatial and temporal localities for better data accesses.
6.2 Results

Table 6.1 shows the execution results for MKL’s MM implementation.

**Table 6.1** Execution Time (in Seconds) of the MKL’s MM Implementation on the Intel Xeon Platform

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
<th>4096</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time Spent (sec)</td>
<td>0.02705</td>
<td>0.00123</td>
<td>0.00431</td>
<td>0.03038</td>
<td>0.328</td>
<td>2.516</td>
<td>20.00</td>
</tr>
<tr>
<td>Slowdown</td>
<td>NA</td>
<td>0.045</td>
<td>3.501</td>
<td>7.049</td>
<td>10.7</td>
<td>7.7</td>
<td>7.9</td>
</tr>
<tr>
<td>Memory Consumption (MB)</td>
<td>14.500</td>
<td>14.548</td>
<td>14.748</td>
<td>14.992</td>
<td>15.000</td>
<td>64.2</td>
<td>212.2</td>
</tr>
<tr>
<td>Size of the 3 Matrices (MB)</td>
<td>0.048</td>
<td>0.192</td>
<td>0.768</td>
<td>3</td>
<td>12</td>
<td>48</td>
<td>192</td>
</tr>
<tr>
<td>Memory Expansion</td>
<td>302.08</td>
<td>75.77</td>
<td>19.2</td>
<td>5.0</td>
<td>1.25</td>
<td>1.34</td>
<td>1.11</td>
</tr>
</tbody>
</table>

The slowdown keeps getting closer to 8 with increases in the matrix size. And the memory expansion becomes close to 1. This implies that MKL is not using Strassen’s algorithm but a block-based algorithm, otherwise the memory expansion will not be close to 1.
CHAPTER 7
ACCELERATION USING VECTOR CO-PROCESSOR

7.1 Hardware Architecture

Figure 7.1 shows an in-house developed (at CAPPL laboratory) vector co-processor (VP) computing platform [12] [13]. The scalar CPU is a Xilinx MicroBlaze (125MHz). The CPU issues vector instructions to the VP. The VP loads data from the vector memory (VM) into the VP vector register(s), carries out computations and then, stores the results back into the VM. The CPU is responsible to transfer data from the off-chip DDR memory to the vector memory through DMA transfers before the computations, and from the vector memory to the DDR memory after the computations.

![Vector processor computing platform architecture](taken from 12).

Figure 7.1 Vector processor computing platform architecture [taken from 12].
7.2 Calculation Process

The fundamental operation used is SAXPY (Single-precision real Alpha X Plus Y: \(z=\alpha x+y\)), which is a combination of scalar multiplication and vector addition in computations with vector processors. In order to use vector instructions, the matrix multiplication operation needs to be conducted in a different way than the traditional one. The calculation process is as follows.

Figure 7.2 shows that C1 (sub-matrix of C) is calculated from A1 (sub-matrix of A) and B, C2 from A2 and B, and so on.

![Figure 7.2](image)

**Figure 7.2** Partitioning matrices A and C for VP-based MM.

Figure 7.3 shows that C1 is actually calculated as A1*B.

![Figure 7.3](image)

**Figure 7.3** C1 is calculated as A1 * B.

Figure 7.4 shows how the columns of A1 are multiplied with the rows in matrix B. The first column of A1 is multiplied with the first row from B, to produce one layer of C1. The second column of A1 is multiplied with the second row from B, and the results are accumulated to C1. This procedure repeats until the final C1 is produced.
Figure 7.4 Partitioning A1 and B.

Figure 7.5 shows that how one column of elements of A1 is multiplied with one row of elements of B. One row of elements of B is divided into several sections. The section size is the chosen vector length. The vector length is the number of elements that can be processed by one vector instruction. Before the calculation, B1 is transferred from the DDR memory to vector memory. To overlap computations with data transfers, when the computation happens on B1, B2 is being transferred to the vector memory.

Figure 7.5 Partitioning of C1.

Figure 7.6 shows how C11 is produced. The first element of A11 is multiplied with B11 to produce the first row of C11. The second element of A11 is multiplied with B11 to produce the second row of C11, and so on.

Figure 7.6 Partitioning C11.
7.3 Analysis

7.3.1 Time Complexity
The number of multiplications of elements is not reduced. The time complexity is still \( O(N^3) \). However, in a vector processor, all lanes (processing units) in the VP can conduct element multiplication simultaneously. Thus, the speedup depends on the number of lanes. In this experiment, the number of lanes is eight. So the expected speedup is 8.

7.3.2 Memory Consumption
No extra memory in the DDR is needed, so the memory consumption is still \( 3*N^2 \) elements.

7.4 Results
Tables 7.1 and 7.2 show the performance of matrix multiplication on the VP platform (125MHz). The vector length determines how many elements can be loaded into the VP at one time. Compared to other methods that were tested previously, the speedup is substantial.

<table>
<thead>
<tr>
<th>Vector Length</th>
<th>Matrix Size</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>32</td>
<td>6.325</td>
</tr>
<tr>
<td></td>
<td>128</td>
<td>3.141</td>
</tr>
</tbody>
</table>
Table 7.2 Execution Time (in million clock cycles) of Matrix Multiplication on the VP Platform

<table>
<thead>
<tr>
<th>Vector Length</th>
<th>Matrix Size</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td></td>
<td>809.6</td>
</tr>
<tr>
<td>128</td>
<td></td>
<td>402.0</td>
</tr>
</tbody>
</table>
CHAPTER 8
PERFORMANCE COMPARISONS

The previous chapters presented the algorithms’ performance individually and the implementations were compiled by disabling the optimizations. This chapter presents thorough performance results in various scenarios.

8.1 Intel Xeon Platform

8.1.1 Optimization Disabled (OD)

The comparison is shown in Table 8.1. K*K is the block size in number of elements.

Table 8.1  Execution Time (in Seconds) of All the Implementations on the Intel Xeon Platform with Compiling Optimization Disabled

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>Matrix Size</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
<th>2048</th>
</tr>
</thead>
<tbody>
<tr>
<td>Brute-force</td>
<td></td>
<td>0.002336</td>
<td>0.029708</td>
<td>0.253991</td>
<td>2.684</td>
<td>63.753</td>
<td>537.389</td>
</tr>
<tr>
<td>Basic Block-based</td>
<td></td>
<td>0.002677</td>
<td>0.043091</td>
<td>0.227063</td>
<td>1.683</td>
<td>13.470</td>
<td>108.300</td>
</tr>
<tr>
<td>(K=32)</td>
<td></td>
<td>0.003932</td>
<td>0.022385</td>
<td>0.191102</td>
<td>1.453994</td>
<td>11.486</td>
<td>90.126</td>
</tr>
<tr>
<td>Goto’s (K=8)</td>
<td></td>
<td>0.005010</td>
<td>0.037459</td>
<td>0.202927</td>
<td>1.416484</td>
<td>10.004</td>
<td>69.778</td>
</tr>
<tr>
<td>Strassen’s (K=32)</td>
<td></td>
<td>0.027051</td>
<td>0.001231</td>
<td>0.004310</td>
<td>0.030382</td>
<td>0.328</td>
<td>2.516</td>
</tr>
<tr>
<td>MKL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Compiler optimizations are disabled to provide a baseline reference. In reality, some degree of optimization will be specified. Table 8.1 shows that Strassen’s implementation runs slightly faster than Goto’s for large matrix multiplications.
8.1.2 Full Optimization (O3)

The comparison is shown in Table 8.2. K*K is the block size in number of elements.

Table 8.2 shows that when compiling with the O3 option, Goto’s implementation runs faster than Strassen’s algorithm and produces results even close to those of MKL. This shows that when the computation becomes faster, the bottleneck results from memory accesses.

8.2 Xilinx FPGA Platform

The comparison is shown in Table 8.1. K is the block size in number of elements.

Table 8.3 shows that the vector processor speeds up the computation drastically. It also shows that Strassen’s implementation runs faster than the Goto’s implementation. This is because when the processor is slow (125MHz for our FPGA implementation), the algorithm’s time complexity is more influential than the memory access efficiency.
Table 8.3 Execution Time (in Seconds) of All the Implementations on the Xilinx FPGA Platform with and without the VP

<table>
<thead>
<tr>
<th>Matrix Size</th>
<th>Algorithm</th>
<th>64</th>
<th>128</th>
<th>256</th>
<th>512</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Brute-force</td>
<td>0.105</td>
<td>0.841</td>
<td>6.717</td>
<td>53.664</td>
<td>429.12</td>
</tr>
<tr>
<td></td>
<td>Basic Block-based (K=8)</td>
<td>0.054</td>
<td>0.457</td>
<td>4.029</td>
<td>32.648</td>
<td>269.376</td>
</tr>
<tr>
<td></td>
<td>Goto’s (K=8)</td>
<td>0.054</td>
<td>0.472</td>
<td>4.335</td>
<td>32.975</td>
<td>264.281</td>
</tr>
<tr>
<td></td>
<td>Strassen’s (K=16)</td>
<td>0.053</td>
<td>0.410</td>
<td>3.038</td>
<td>21.855</td>
<td>155</td>
</tr>
<tr>
<td></td>
<td>Vector Processor</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>3.141</td>
</tr>
</tbody>
</table>

8.3 MKL vs. VP

MKL was tested on the Intel Xeon platform which has a much higher clock frequency than the VP platform. In order to compare the performance of MKL and VP, the execution time is recorded in clock cycles. The result is shown in Table 8.4.

Table 8.4 Execution Time (in million clock cycles) of MM using MKL and the VP

<table>
<thead>
<tr>
<th>Method</th>
<th>Matrix Size</th>
<th>1024</th>
</tr>
</thead>
<tbody>
<tr>
<td>MKL</td>
<td></td>
<td>640.5</td>
</tr>
<tr>
<td>VP</td>
<td></td>
<td>402.0</td>
</tr>
</tbody>
</table>

The result shows that the VP consumes fewer clock cycles than MKL.
CHAPTER 9
CONCLUSIONS

In terms of time complexity: Strassen’s matrix multiplication algorithm has time complexity of $O(N^{2.807})$. The Brute-force, basic Block-based, Goto’s algorithm and VP implementation all have time complexity of $O(N^{3})$. In terms of memory accesses: the basic Block-based and Goto’s algorithm improve the cache performance by blocking, which improves data access locality. Other than that, Goto’s algorithm improves the TLB performance by copying kernel blocks into contiguous memory. The Brute-force and Strassen’s algorithms have inferior cache performance due to poor data locality. The results show that when the CPU is fast, Goto’s algorithm runs faster than Strassen’s algorithm because the data access speed is the bottleneck in this case. On the contrary, when the CPU is slow, Strassen’s algorithm runs faster because the computation complexity becomes the key factor in this case. Finally, the results show that SIMD platforms, such as the Intel Xeon with instruction extensions and the in-house developed VP (Vector Processor) for FPGA prototyping, matrix multiplication is accelerated substantially. In fact, the results show that the VP runs much faster than MKL (Intel’s optimized Math Kernel Library) because the VP has can take advantage of much larger vector lengths while its overheads are negligible.
APPENDIX

C SOURCE CODE

Here is all the source code implemented.

//config.h

#ifndef __CONFIG_H__
#define __CONFIG_H__

#define EN_THR
#define EN_BLK
#define EN_GOTO
#define EN_STRSN
#define EN_MKL

/* define DEBUG to use simpler initialized matrix value */
#define DEBUG

//#define PRT_MALLOC

//#define PRT_MTX
#define PRT_LIGHT

#if PRT_LIGHT
#define PRT_SIZE 4
#else
#define PRT_SIZE mtx_sz
#endif

//#define EN_CHK

//#define CTN_ERR
#define MTX_SIZE 64
#define B_SZ 4
#define GOTO_BL_SZ 4
#define STRSN_BL_SZ 4

#define MAX_MTX_SIZE 2048
#define MAX_B_SZ 64
#define MAX_GOTO_BL_SZ 64
#define MAX_STRSN_BL_SZ 64

#define TEST_SIZE 2

// Strassen's
// #define MY_MALLOC
#define EN_FREE

#define MALLOC_BASE ( XPAR_DDR2_SDRAM_MPMC_BASEADDR + 0x01000000)

#define A_MTX_BASE XPAR_DDR2_SDRAM_MPMC_BASEADDR
#define B_MTX_BASE ( XPAR_DDR2_SDRAM_MPMC_BASEADDR + 0x00400000)
#define C_MTX_BASE ( XPAR_DDR2_SDRAM_MPMC_BASEADDR + 0x00800000)
#define TST_MTX_BASE ( XPAR_DDR2_SDRAM_MPMC_BASEADDR + 0x00C00000)

/* if define "CLOCK", it will use millisecond clock, otherwise high precision.*/
// #define CLOCK
#define EN_FREE

// misc.h
#ifndef __MISC_H__
#define __MISC_H__
#include <malloc.h>
#include "config.h"

#define min(a,b) ((a)<(b)?(a):(b))
#define max(a,b) ((a)>(b)?(a):(b))

char* malloc_li(unsigned int size);
int free_li(char *p, unsigned int size);

void init_mtxs(float *DDR_A_mtx, float *DDR_B_mtx, float *DDR_C_mtx, unsigned int mtx_sz);

void blocking_mm(float *DDR_A_mtx, float *DDR_B_mtx, 
 float *DDR_C_mtx, unsigned int mtx_sz, 
 unsigned int B);

int cmp_mtx(float *A, float *B, unsigned int mtx_sz);

void printm(float *A, int lda, int n);

void resetm(float *A, unsigned int mtx_sz);

void goto_sgemm(float *A, int lda, 
 float *B, int ldb, 
 float *C, int ldc, 
 int Msz, int blk_size);

void stra_sgemm(float *A, int lda, float *B, int ldb, float *C, int ldc, 
 int lka, int lkb, int lkc, int lkA, int lkB, int lkC, 
 int blk_size);

int cmp_mtx(float *A, float *B, unsigned int mtx_sz);

void init_mtxs(float *DDR_A_mtx, float *DDR_B_mtx, float *DDR_C_mtx, unsigned int mtx_sz);

void blocking_mm(float *DDR_A_mtx, float *DDR_B_mtx, 
 float *DDR_C_mtx, unsigned int mtx_sz, 
 unsigned int B);

int cmp_mtx(float *A, float *B, unsigned int mtx_sz);

void printm(float *A, int lda, int n);

void resetm(float *A, unsigned int mtx_sz);

void goto_sgemm(float *A, int lda, 
 float *B, int ldb, 
 float *C, int ldc, 
 int Msz, int blk_size);

void stra_sgemm(float *A, int lda, float *B, int ldb, float *C, int ldc, 
 int lka, int lkb, int lkc, int blk_size);
int n, unsigned int strsn_blsz;

double clock_it(void);

void thr_for_loop(float *DDR_A_mtx, float *DDR_B_mtx, float *DDR_C_mtx, unsigned int mtx_sz);

#endif

//goto_blas.c
#include "config.h"
#include "misc.h"

/*
 * Block multiply Panel.
 */
static void sgebp(float *A, int lda,
   float *B, int ldb,
   float *C, int lde, 
   int Msz, int blk_size)
{
   float *a;
   unsigned int bs = blk_size * blk_size;
   int m, k, n, lixa, lixb, lixc, lixA;

   //copy A to continuous memory
#undef MY_MALLOC
a = (float*)malloc_li(bs*sizeof(float));  
#else  
a = (float*)malloc(bs*sizeof(float));  
#endif

for(m=0; m < blk_size; m++){
    lixA = m*lda;  
    lixa = m*blk_size;  
    for(k=0; k < blk_size; k++){
        *(a + lixa + k) = *(A + lixA + k);  
    }
}

//normal MM mutliplication  
for(k=0; k < blk_size; k++){
    for(m=0; m <blk_size; m++){
        lixa=m*blk_size;  
        lixb=k*ldb;  
        lixc=m*ldc; //line index  
        for(n=0; n <Msz; n++)
            *(C+ lixc +n) += *(a + lixa + k) * *(B + lixb + n);  
    }
}

#ifdef MY_MALLOC
    free_li((char *)a, bs*sizeof(float));  
#else  
    free(a);  
#endif
static void sgepp(float *A, int lda, float *B, int ldb, float *C, int ldc, int Msz, int blk_size) {
    int N = Msz / blk_size;
    int i = 0;
    float *Ax = A;
    float *Cx = C;
    int idxGapA = lda * blk_size;
    int idxGapC = ldc * blk_size;
    for (i = 0; i < N; i++) {
        sgebp(Ax, lda, B, ldb, Cx, ldc, Msz, blk_size);
        Ax += idxGapA;
        Cx += idxGapC;
    }
}

static void sgepp(float *A, int lda, float *B, int ldb, float *C, int ldc, int Msz, int blk_size) {
    int N = Msz / blk_size;
    int i = 0;
    float *Ax = A;
    float *Cx = C;
    int idxGapA = lda * blk_size;
    int idxGapC = ldc * blk_size;
    for (i = 0; i < N; i++) {
        sgebp(Ax, lda, B, ldb, Cx, ldc, Msz, blk_size);
        Ax += idxGapA;
        Cx += idxGapC;
    }
}

/*
 * Panel multiply Panel.
 */

/*
 * Matrix multiply Matrix.
 */
void goto_sgemm(float *A, int lda,
    float *B, int ldb,
    float *C, int ldc, 
    int Msz, int blk_size)
{

    int N, i;
    int idxGapA, idxGapB;
    float *Ax, *Bx;
    blk_size = blk_size < Msz ? blk_size : Msz;
    N = Msz/blk_size;
    Ax = A;
    Bx = B;
    idxGapA = blk_size;
    idxGapB = ldb * blk_size;
    for( i = 0; i < N; i++) {
        sgepp(Ax, lda,
            Bx, ldb,
            C, ldc,
            Msz, blk_size);
        Ax += idxGapA;
        Bx += idxGapB;
    }
}

//main.c

/*

* Xilinx EDK 12.3 EDK_MS3.70d
*/
This file is a sample test application

This application is intended to test and/or illustrate some functionality of your system. The contents of this file may vary depending on the IP in your system and may use existing IP driver functions. These drivers will be generated in your XPS project when you run the "Generate Libraries" menu item in XPS.

Your XPS project directory is at:

D:\Programs\Xilinx\FALL_11\mb_board_test_v01\n
// Located in: microblaze_0/include/xparameters.h
#include <stdio.h>
#include <malloc.h>
#include <time.h>
#include <mkl_blas.h>
#include <windows.h>

#include "config.h"
#include "misc.h"

#ifdef MY_MALLOC
extern unsigned int malloc_current ;
extern unsigned int malloc_base ;
extern unsigned int malloc_high ;
#endif
int main (void) {
    unsigned int mtx_sz;

#ifdef EN_BLK
    unsigned int B;
#endif

#ifdef EN_GOTO
    unsigned int goto_blsz;
#endif

#ifdef EN_STRSN
    unsigned int strsn_blsz;
#endif

#ifdef EN_MKL
    const float alpha = 1;
    const float beta = 0;
    const char transa='t';
    const char transb='t';
#endif

int re;
float* DDR_A_mtx;
float* DDR_B_mtx;
float* DDR_C_mtx;
float* DDR_T_mtx;
double execTime;

#ifdef CLOCK
    double startTime, endTime;
#else
    LARGE_INTEGER nFreq;
    LARGE_INTEGER nBeginTime;
    LARGE_INTEGER nEndTime;
    double nCycles;
    QueryPerformanceFrequency(&nFreq);
#endif

#ifdef MY_MALLOC
    malloc_base = (unsigned int)malloc(256*1024*1024);//256M memory
    malloc_current = malloc_base;
    malloc_high = malloc_base + 256*1024*1024 - 1;
#endif

for(mtx_sz = MTX_SIZE; mtx_sz <= MAX_MTX_SIZE; mtx_sz *= 2)
{
    DDR_A_mtx = (float *)malloc(sizeof(float) * mtx_sz * mtx_sz);
    DDR_B_mtx = (float *)malloc(sizeof(float) * mtx_sz * mtx_sz);
    DDR_C_mtx = (float *)malloc(sizeof(float) * mtx_sz * mtx_sz);
    DDR_T_mtx = (float *)malloc(sizeof(float) * mtx_sz * mtx_sz);

    init_mtxs(DDR_A_mtx, DDR_B_mtx, DDR_C_mtx, mtx_sz);
    resetm(DDR_T_mtx, mtx_sz);
#endif
printf("A:\r\n");
printm(DDR_A_mtx, mtx_sz, PRT_SIZE);
printf("B:\r\n");
printm(DDR_B_mtx, mtx_sz, PRT_SIZE);
printf("C:\r\n");
printm(DDR_C_mtx, mtx_sz, PRT_SIZE);
#endif

#ifdef EN_THR
    // Algorithm 1
    printf("n------- 3-for-loop\r\n");
    printf("Matrix size = %d\r\n", mtx_sz);
    printf("START 3-for-loop implementation\r\n");
#endif

#ifdef CLOCK
    startTime = clock_it();

    // START PERFORMANCE ROUTINE
    thr_for_loop(DDR_A_mtx, DDR_B_mtx, DDR_T_mtx, mtx_sz);
    // END PERFORMANCE ROUTINE

    endTime = clock_it();
    execTime = endTime - startTime;
    printf("Execution time is %.4f seconds\n", execTime);
#else
    QueryPerformanceCounter(&nBeginTime);

    // START PERFORMANCE ROUTINE
    thr_for_loop(DDR_A_mtx, DDR_B_mtx, DDR_T_mtx, mtx_sz);
    // END PERFORMANCE ROUTINE
    QueryPerformanceCounter(&nEndTime);
#endif
nCycles = (double)(nEndTime.QuadPart-nBeginTime.QuadPart);
execTime = nCycles /(double)nFreq.QuadPart;

printf("The cpu's frequency is: %.0f Hz\n", (double)nFreq.QuadPart);
printf("Execution takes %.0f cycles\n", nCycles);
printf("Execution takes %.9f seconds\n", execTime);
#endif

#ifdef PRT_MTX
    printf("T:\r\n");
    printm(DDR_T_mtx, mtx_sz , PRT_SIZE);
#endif
    printf("END 3-for-loop implementation\n");
}
#endif

#ifdef EN_BLK
for(B = B_SZ; B <= MAX_B_SZ; B*=2){
    //Algorithm 2
    resetm(DDR_C_mtx, mtx_sz);
    printf("---------- Blocking algorithm\n");
    printf("Matrix size = %d\n", mtx_sz);
    printf("Block size = %d\n", B);
    printf("START blocking implementation\n");
    #ifdef CLOCK
        startTime = clock_it();
    #endif
}
#endif
// START PERFORMANCE ROUTINE
blocking_mm(DDR_A_mtx, DDR_B_mtx, DDR_C_mtx, mtx_sz, B);
// END PERFORMANCE ROUTINE

endTime = clock_it();
execTime = endTime - startTime;
printf("Execution time is %3.4f seconds\n", execTime);
#else
QueryPerformanceCounter(&nBeginTime);
// START PERFORMANCE ROUTINE
blocking_mm(DDR_A_mtx, DDR_B_mtx, DDR_C_mtx, mtx_sz, B);
// END PERFORMANCE ROUTINE
QueryPerformanceCounter(&nEndTime);

nCycles = (double)(nEndTime.QuadPart-nBeginTime.QuadPart);
execTime =nCycles /(double)nFreq.QuadPart;

printf("The cpu's frequency is: %.0f Hz\n", (double)nFreq.QuadPart);
printf("Execution takes %.0f cycles\n", nCycles);
printf("Execution takes %.9f seconds\n", execTime);
#endif

#ifdef PRT_MTX
printf("C:\r\n");
printm(DDR_C_mtx, mtx_sz,PRT_SIZE);
#endif

#ifdef EN_CHK

#endif
if((re = cmp_mtx(DDR_C_mtx, DDR_T_mtx, mtx_sz)) != -1)
{
    printf("Calculation wrong at row %d, column %d\r\n", re/mtx_sz, re%mtx_sz);
#ifndef CTN_ERR
    printf("Abort.\r\n");
    return -1;
#endif
}
else
{
    printf("Result correct!\r\n");
}
#endif

printf("END blocking implementation\r\n");

}//for
#endif

#ifndef EN_GOTO
for(goto_blsz = GOTO_BL_SZ; goto_blsz <= MAX_GOTO_BL_SZ; goto_blsz*=2){
    //Algorithm 3
    resetm(DDR_C_mtx, mtx_sz);
    printf("-------- GotoBLAS algorithm: \r\n");
    printf("Matrix size = %d\r\n", mtx_sz);
    printf("Block size = %d\r\n", goto_blsz);
    printf("START GotoBLAS implementation\r\n");
#ifndef CLOCK
    startTime = clock_it();
#endif
    // START PERFOMANCE ROUTINE
goto_sgemm(DDR_A_mtx, mtx_sz, DDR_B_mtx, mtx_sz, DDR_C_mtx, mtx_sz, mtx_sz,
goto_blsz);

    // END PERFORMANCE ROUTINE

endTime = clock_it();
execTime = endTime - startTime;
printf("Execution time is %3.4f seconds\n", execTime);

#else
    QueryPerformanceCounter(&nBeginTime);
    // START PERFORMANCE ROUTINE
    goto_sgemm(DDR_A_mtx, mtx_sz, DDR_B_mtx, mtx_sz, DDR_C_mtx, mtx_sz, mtx_sz,
goto_blsz);
    // END PERFORMANCE ROUTINE
    QueryPerformanceCounter(&nEndTime);

    nCycles = (double)(nEndTime.QuadPart-nBeginTime.QuadPart);
    execTime =nCycles /(double)nFreq.QuadPart;

    printf("The cpu's frequency is: %.0f Hz\n", (double)nFreq.QuadPart);
    printf("Execution takes %.0f cycles\n", nCycles);
    printf("Execution takes %.9f seconds\n", execTime);

#endif

#endif PRT_MTX
    printf("C:\r\n");
    printm(DDR_C_mtx,mtx_sz,PRT_SIZE);
#endif

#ifdef EN_CHK
if((re = cmp_mtx(DDR_C mtx, DDR_T mtx, mtx_sz)) != -1) {
    printf("Calculation wrong at row %d, column %d\n", re/mtx_sz, re%mtx_sz);
    #ifndef CTN_ERR
    printf("Abort.\n");
    return -1;
    #endif
}
else {
    printf("Result correct!\n");
}
#endif
printf("END GotoBLAS implementation\n");
}
#endif

#ifndef EN_STRSN
for(strsn_blsz = STRSN_BL_SZ; strsn_blsz <= MAX_STRSN_BL_SZ; strsn_blsz*=2){
    resetm(DDR_C mtx, mtx_sz);
    //Algorithm 4
    printf("-------- Strassen:\n");
    printf("Matrix size = %d\n", mtx_sz);
    printf("Block size = %d\n", strsn_blsz);
    printf("START STRASSEN\n");
    #ifdef CLOCK
    startTime = clock_it();
    // START PERFOMANCE ROUTINE
stra_sgemm(DDR_A_mtx, mtx_sz, DDR_B_mtx, mtx_sz, DDR_C_mtx, mtx_sz, mtx_sz, strsn_blsz);

// END PERFORMANCE ROUTINE

eTime = clock_it();
execTime = endTime - startTime;
printf("Execution time is %3.4f seconds\n", execTime);

#else
QueryPerformanceCounter(&nBeginTime);
// START PERFORMANCE ROUTINE
stra_sgemm(DDR_A_mtx, mtx_sz, DDR_B_mtx, mtx_sz, DDR_C_mtx, mtx_sz, mtx_sz, strsn_blsz);
// END PERFORMANCE ROUTINE
QueryPerformanceCounter(&nEndTime);

nCycles = (double)(nEndTime.QuadPart-nBeginTime.QuadPart);
execTime =nCycles /(double)nFreq.QuadPart;

printf("The cpu's frequency is: %.0f Hz\n", (double)nFreq.QuadPart);
printf("Execution takes %.0f cycles\n", nCycles);
printf("Execution takes %.9f seconds\n", execTime);
#endif

#endif PRT_MTX

printf("C:\r\n");
printm(DDR_C_mtx,mtx_sz,PRT_SIZE);
#endif
#ifdef EN_CHK
    if((re = cmp_mtx(DDR_C_mtx, DDR_T_mtx, mtx_sz)) != -1)
    {
        printf("Calculation wrong at row %d, column %d\n", re/mtx_sz, re%mtx_sz);
        #ifndef CTN_ERR
        printf("Abort.\n");
        return -1;
        #endif
    }
    #endif

else
    {
        printf("Result correct!\n");
    }
#endif

printf("END STRASSEN\n");
}
#endif

#ifdef EN_MKL
    //Algorithm 3
    resetm(DDR_C_mtx, mtx_sz);
    printf("-------- MKL library:\n");
    printf("Matrix size = %d\n", mtx_sz);
    printf("START MKL implementation\n");
    //using function from MKL.
    //void sgemm(const char *transa, const char *transb, const MKL_INT *m, const MKL_INT *n, const MKL_INT *k,
    //const float *alpha, const float *a, const MKL_INT *lda, const float *b, const MKL_INT *ldb,
    //const float *beta, float *c, const MKL_INT *ldc);
    #ifdef CLOCK

startTime = clock_it();

//result = alpha * A * B + beta * C
sgemm(&transa, &transb, &mtx_sz, &mtx_sz, &mtx_sz,
    &alpha, DDR_A_mtx, &mtx_sz, DDR_B_mtx, &mtx_sz,
    &beta, DDR_C_mtx, &mtx_sz);

endTime = clock_it();
execTime = endTime - startTime;
printf("Execution takes %3.4f seconds\n", execTime);

#else

QueryPerformanceCounter(&nBeginTime);
//result = alpha * A * B + beta * C
sgemm(&transa, &transb, &mtx_sz, &mtx_sz, &mtx_sz,
    &alpha, DDR_A_mtx, &mtx_sz, DDR_B_mtx, &mtx_sz,
    &beta, DDR_C_mtx, &mtx_sz);
QueryPerformanceCounter(&nEndtime);
nCycles = (double)(nEndTime.QuadPart-nBeginTime.QuadPart);
execTime = nCycles / (double)nFreq.QuadPart;
printf("The cpu's frequency is: %.0f Hz\n", (double)nFreq.QuadPart);
printf("Execution takes %.0f cycles\n", nCycles);
printf("Execution takes %.9f seconds\n", execTime);

#endif

#elifdef PRT_MTX

printf("C:\r\n");
printm(DDR_C_mtx, mtx_sz, PRT_SIZE);
#endif

#elifdef EN_CHK

#endif
if((re = cmp_mtx(DDR_C_mtx, DDR_T_mtx, mtx_sz)) != -1)
{
    printf("Calculation wrong at row %d, column %d\r\n", re/mtx_sz, re%mtx_sz);
#ifndef CTN_ERR
    printf("Abort.\r\n");
    return -1;
#endif
}
else
{
    printf("Result correct!\r\n");
}
#endif
printf("END MKL implementation\r\n");
#endif

free(DDR_A_mtx);
free(DDR_B_mtx);
free(DDR_C_mtx);
free(DDR_T_mtx);
}//outer most "for"

printf("-- Exiting main()--\r\n");

return 0;
}

//strassen.c
#include <stdio.h>
#include "misc.h"
#include "config.h"

// single precision general matrix-matrix addition
// 'ld' is leading dimension, for example, for submatrix in A[m][n], their leading dimension is 'm'.
void sgema(float *A, int lda, float *B, int ldb, float *C, int ldc, int n)
{
    int i, j;
    for(i=0; i < n; i++)
    {
        for(j=0; j < n; j++)
        {
            *(C + i*ldc + j) = *(A + i*lda + j) + *(B + i*ldb + j);
        }
    }
}

// single precision general matrix-matrix subraction
void sgems(float *A, int lda, float *B, int ldb, float *C, int ldc, int n)
{
    int i, j;
    for(i=0; i < n; i++)
    {
        for(j=0; j < n; j++)
        {
            *(C + i*ldc + j) = *(A + i*lda + j) - *(B + i*ldb + j);
        }
    }
}
//matrix-matrix multiplication

void stra_sgemm( float *A, int lda, float *B, int ldb, float *C, int ldc, 
                 int n, unsigned int strsn_blsz)
{

    //print("Entering sgemm.\r\n");
    if( n <= strsn_blsz)
    {
        int i,j,k;
        for( i=0; i<n; i++)
        {
            for( j=0; j<n; j++)
            {
                *(C + i*ldc +j) = 0;
                for( k=0; k<n; k++)
                {
                    *(C + i*ldc +j) += *(A + i*lda +k) * *(B + k*ldb + j);
                }
            }
        }
    }
    else
    {
        int ldm = n/2;
        float *a,*b,*c,*d;
        float *e,*f,*g,*h;
        float *r,*s,*t,*u;

        #ifdef MY_MALLOC

        float *p1 = (float *)malloc_li(sizeof(float) * ldm * ldm);
        float *p2 = (float *)malloc_li(sizeof(float) * ldm * ldm);
        float *p3 = (float *)malloc_li(sizeof(float) * ldm * ldm);

        #endif
        
    }
float *p4 = (float *)malloc(sizeof(float) * ld * ldm);
float *p5 = (float *)malloc(sizeof(float) * ld * ldm);
float *p6 = (float *)malloc(sizeof(float) * ld * ldm);
float *p7 = (float *)malloc(sizeof(float) * ld * ldm);

float *A1 = (float *)malloc(sizeof(float) * ld * ldm);
float *A2 = (float *)malloc(sizeof(float) * ld * ldm);
float *A3 = (float *)malloc(sizeof(float) * ld * ldm);
float *A4 = (float *)malloc(sizeof(float) * ld * ldm);
float *A5 = (float *)malloc(sizeof(float) * ld * ldm);
float *B5 = (float *)malloc(sizeof(float) * ld * ldm);
float *A6 = (float *)malloc(sizeof(float) * ld * ldm);
float *A7 = (float *)malloc(sizeof(float) * ld * ldm);
float *B7 = (float *)malloc(sizeof(float) * ld * ldm);

#else

float *p1 = (float *)malloc(sizeof(float) * ld * ldm);
float *p2 = (float *)malloc(sizeof(float) * ld * ldm);
float *p3 = (float *)malloc(sizeof(float) * ld * ldm);
float *p4 = (float *)malloc(sizeof(float) * ld * ldm);
float *p5 = (float *)malloc(sizeof(float) * ld * ldm);
float *p6 = (float *)malloc(sizeof(float) * ld * ldm);
float *p7 = (float *)malloc(sizeof(float) * ld * ldm);

float *A1 = (float *)malloc(sizeof(float) * ld * ldm);
float *A2 = (float *)malloc(sizeof(float) * ld * ldm);
float *A3 = (float *)malloc(sizeof(float) * ld * ldm);
float *A4 = (float *)malloc(sizeof(float) * ld * ldm);
float *A5 = (float *)malloc(sizeof(float) * ld * ldm);
float *B5 = (float *)malloc(sizeof(float) * ld * ldm);
float *A6 = (float *)malloc(sizeof(float) * ldm * ldm);
float *B6 = (float *)malloc(sizeof(float) * ldm * ldm);
float *A7 = (float *)malloc(sizeof(float) * ldm * ldm);
float *B7 = (float *)malloc(sizeof(float) * ldm * ldm);
#endif

a = A;
b = A + ldm;
c = A + lda * ldm;
d = c + ldm;
e = B;
f = B + ldm;
g = B + ldb * ldm;
h = g + ldm;

r = C;
s = C + ldm;
t = C + ldc * ldm;
u = t + ldm;

//p1 = a * (f - h);
sgems(f, ldb, h, ldb, A1, ldm, ldm);
stra_sgemm(a, lda, A1, ldm, p1, ldm, ldm, strsn_blsz);

//p2 = (a + b) * h;
sgema(a, lda, b, lda, A2, ldm, ldm);
stra_sgemm(A2, ldm, h, ldb, p2, ldm, ldm, strsn_blsz);

//p3 = (c + d) * e;
sgema(c, lda, d, lda, A3, ldm, ldm);
stra_sgemm(A3, ldm, e, ldb, p3, ldm, ldm, strsn_blsz);

//p4 = d * (g - e);
sgems(g, ldb, e, ldb, A4, ldm, ldm);
stra_sgemm(d, lda, A4, ldm, p4, ldm, ldm, strsn_blsz);

//p5 = (a + d) * (e + h);
sgema(a, lda, d, lda, A5, ldm, ldm);
sgema(e, ldb, h, ldb, B5, ldm, ldm);
stra_sgemm(A5, ldm, B5, ldm, p5, ldm, ldm, strsn_blsz);

//p6 = (b - d) * (g + h);
sgems(b, lda, d, lda, A6, ldm, ldm);
sgema(g, ldb, h, ldb, B6, ldm, ldm);
stra_sgemm(A6, ldm, B6, ldm, p6, ldm, ldm, strsn_blsz);

//p7 = (a - c) * (e + f);
sgems(a, lda, c, lda, A7, ldm, ldm);
sgema(e, ldb, f, ldb, B7, ldm, ldm);
stra_sgemm(A7, ldm, B7, ldm, p7, ldm, ldm, strsn_blsz);

//r = p5 + p4 - p2 + p6;
sgema(p5, ldm, p4, ldm, A1, ldm, ldm);
sgems(A1, ldm, p2, ldm, A2, ldm, ldm);
sgema(A2, ldm, p6, ldm, r, ldc, ldm);

//s = p1 + p2;
sgema(p1, ldm, p2, ldm, s, ldc, ldm);
/t = p3 + p4;
sgema(p3, ldm, p4, ldm, t, ldc, ldm);

//u = p5 + p1 - p3 - p7;
sgema(p5, ldm, p1, ldm, A1, ldm, ldm);
sgems(A1, ldm, p3, ldm, A2, ldm, ldm);
sgems(A2, ldm, p7, ldm, u, ldc, ldm);

#ifdef MY_MALLOC

#ifdef EN_FREE
//free space

#endif
#endif

free_li((char*)B7, sizeof(float) * ldm * ldm);
free_li((char*)A7, sizeof(float) * ldm * ldm);
free_li((char*)B6, sizeof(float) * ldm * ldm);
free_li((char*)A6, sizeof(float) * ldm * ldm);
free_li((char*)B5, sizeof(float) * ldm * ldm);
free_li((char*)A5, sizeof(float) * ldm * ldm);
free_li((char*)A4, sizeof(float) * ldm * ldm);
free_li((char*)A3, sizeof(float) * ldm * ldm);
free_li((char*)A2, sizeof(float) * ldm * ldm);
free_li((char*)A1, sizeof(float) * ldm * ldm);
free_li((char*)p7, sizeof(float) * ldm * ldm);
free_li((char*)p6, sizeof(float) * ldm * ldm);
free_li((char*)p5, sizeof(float) * ldm * ldm);
free_li((char*)p4, sizeof(float) * ldm * ldm);
free_li((char*)p3, sizeof(float) * ldm * ldm);
free_li((char*)p2, sizeof(float) * ldm * ldm);
free_li((char*)p1, sizeof(float) * ldm * ldm);

#endif

#else

free(p1);
free(p2);
free(p3);
free(p4);
free(p5);
free(p6);
free(p7);
free(A1);
free(A2);
free(A3);
free(A4);
free(A5);
free(B5);
free(A6);
free(B6);
free(A7);
free(B7);
#endif

} }

} }

//utility.c
#include <stdio.h>
#include <time.h>
#include "config.h"
#include "misc.h"

#ifdef MY_MALLOC

unsigned int malloc_current = 0;
unsigned int malloc_base = 0;
unsigned int malloc_high = 0;

char* malloc_li(unsigned int size)
{
    char *ret;
    ret = (char*)malloc_current;
    if((malloc_current + size) > malloc_high)
    {
        printf("Error: Malloc(), not enough memory.\n\n");
        printf("size: %d, current: 0x%x \n", size, malloc_current);
        return 0;
    }
    else
    {
        malloc_current += size;
    }
#endif
    #ifdef PRT_MALLOC
        xil_printf("malloced: %d, current: 0x%x \n", size, malloc_current);
    #endif
    return ret;
}

int free_li(char *p, unsigned int size)
{
if (malloc_current - size) < malloc_base)
{
    printf("Error: free_li(), reached bottom.\r\n");
    printf("size: %d, current: 0x%x \r\n", size, malloc_current);
    return -1;
}
else
{
    malloc_current -= size;
    p = 0;
#ifdef PRT_MALLOC
    xil_printf("freed: %d, current: 0x%x \r\n", size, malloc_current);
#endif
    return 0;
}
#endif

void init_mtxs(float *DDR_A_mtx, float *DDR_B_mtx, float *DDR_C_mtx, unsigned int mtx_sz)
{
    unsigned int i, j;

    printf("START Initialize DDRAM\r\n");
    // Initialize DDRAM
    for (i=0; i<mtx_sz; i++) {
        for (j=0; j<mtx_sz; j++) {
            #ifndef DEBUG
            DDR_A_mtx[i*mtx_sz+j] = (float)(i*j+1)/(float)23;
            DDR_B_mtx[i*mtx_sz+j] = (float)(i*j+3)/(float)31;
            #endif
        }
    }
}
```c
#include <stdio.h>
#include <stdlib.h>
#include <time.h>

#define mtx_sz 10

// DDR matrices
float DDR_A_mtx[mtx_sz][mtx_sz];
float DDR_B_mtx[mtx_sz][mtx_sz];
float DDR_C_mtx[mtx_sz][mtx_sz];

// Initialize DDRAM
void init_DDRAM(void) {
    int i, j;
    #else
    DDR_A_mtx[i*mtx_sz+j] = (float)((i*j+1)%2)/(float)10.0;
    DDR_B_mtx[i*mtx_sz+j] = (float)((i*j+3)%3)/(float)10.0;
    DDR_C_mtx[i*mtx_sz+j] = (float)0.0;
    #endif
}

// get the current time in seconds
double clock_it(void) {
    clock_t start;
    double timeInSec;
    start = clock();
    timeInSec = (double)(start) / CLOCKS_PER_SEC;
    return timeInSec;
}

// three for loops implementation of Matrix-Matrix Multiplication
void thr_for_loop(float *DDR_A_mtx, float *DDR_B_mtx, float *DDR_C_mtx, unsigned int mtx_sz) {
    unsigned int i, j, k;
    float sum;
    for (i=0; i<mtx_sz; i++) {
        for (j=0; j<mtx_sz; j++) {
            sum = 0.0;
            for (k=0; k<mtx_sz; k++) {
                sum += DDR_A_mtx[i][k] * DDR_B_mtx[k][j];
            }
            DDR_C_mtx[i][j] = sum;
        }
    }
    printf("END Initialize DDRAM\n");
}
```

for (j=0; j<mtx_sz; j++) {
    sum=0.0;
    for (k=0; k<mtx_sz; k++) {
        sum+= DDR_A_mtx[i*mtx_sz+k] * DDR_B_mtx[k*mtx_sz+j];
    }
    DDR_C_mtx[i*mtx_sz+j]=sum;
}

xAAABBBAC

/*
 * Blocking implementation of MM Multiplication.
 * Calculate block by block to increase cache hit rate.
 */

void blocking_mm(float *DDR_A_mtx, float *DDR_B_mtx, 
                 float *DDR_C_mtx, unsigned int mtx_sz,
                 unsigned int B)
{
    unsigned int i, j, k, jj, kk;
    float sum;
    B = B < mtx_sz ? B : mtx_sz;
    for (jj=0; jj<mtx_sz; jj=jj+B) {
        for (kk=0; kk<mtx_sz; kk=kk+B) {
            for (i=0; i<mtx_sz; i=i+1) {
                for (j=jj; j<min(jj+B,mtx_sz); j++) {
                    sum=0.0;
                    for (k=kk; k<min(kk+B,mtx_sz); k++) {
                        sum+=DDR_A_mtx[i*mtx_sz+k] * 
                             DDR_B_mtx[k*mtx_sz+j];
                    }
                    DDR_C_mtx[i*mtx_sz+j]+=sum;
                }
            }
        }
    }
}
```c
int cmp_mtx(float *A, float *B, unsigned int mtx_sz)
{
    int i, j;
    int test_size;
    test_size = TEST_SIZE < mtx_sz ? TEST_SIZE : mtx_sz;
    for (i=0; i<test_size; i=i+1) {
        for (j=0; j<test_size; j=j+1) {
            if ((A[i*mtx_sz+j] - B[i*mtx_sz+j]) < 1)
                continue;
            else
                return i*mtx_sz+j;
        }
    }
    return -1;
}

// print matrix
void printm(float *A, int lda, int n)
{
    float x;
    int i, j;
    for (i=0; i < n; i++)
    {
```
for(j=0; j < n; j++)
{
    x = *(A + i*lda + j);
    printf("%.2f",x);
}
printf("n");
}
printf("n");
}

void resetm(float *A, unsigned int mtx_sz)
{
    unsigned int i,j;
    for (i=0; i<mtx_sz; i=i+1) {
        for (j=0; j<mtx_sz; j=j+1)
        {
            A[i*mtx_sz+j] = 0;
        }
    }
}
REFERENCE


