Fall 2024

ECE 495 - COMP ENGINEER DESIGN LAB

Sui-Hoi Hou

ECE 495 Fall 2024
Computer Engineering Design Laboratory

Course Description:	This course emphasizes hardware design and debugging. Topics include combinational and sequential logic design using CAD tools, VHDL, and design based upon PLA/PLD.
Instructor:	Dr. Edwin Hou 357 ECEC, (973) 596-3521 hou@njit.edu
Lecture/Laboratory meet at:	M 1:00pm–2:20pm (ECEC 100) / Section 001, R 8:30am–12:05pm (FMH 204A) Section 003, R 1:00pm–4:35pm (FMH 204A)
Office hours:	W 10:00am-11:00am or by appointment
Prerequisites:	ECE 353 and (ECE 294 or ECE 394)
Recommended Text:	J. Knoots, E. Hou, Laboratory and Supplementary Notes, ECE 495: Computer Engineering Design Laboratory, Ver. 3.0, ECE Dept. 2007. **This manual is for reference only. Refer to lecture notes for up to date information**. Any book on VHDL.
Academic Integrity:	**Academic Integrity is the cornerstone of higher education and is central to the ideals of this course and the university. Cheating is strictly prohibited and devalues the degree that you are working on. As a member of the NJIT community, it is your responsibility to protect your educational investment by knowing and following the academic code of integrity policy that is found at: NJIT Academic Integrity Code** Please note that it is my professional obligation and responsibility to report any academic misconduct to the Dean of Students Office. **Any student found in violation of the code by cheating, plagiarizing or using any online software inappropriately will result in disciplinary action. This may include a failing grade of F, and/or suspension or dismissal from the university.** If you have any questions about the code of Academic Integrity, please contact the Dean of Students Office at dos@njit.edu
Generative AI:	**This course requires students to work independently without the assistance of artificial intelligence (AI) to fully develop their skills in this subject. AI use is only permitted for enhancing the clarity and readability of reports; otherwise, it is not allowed throughout the course.**

Course Learning Outcomes (CLO):

Student should be able to

1. design sequential circuits (using EEPROM) that meets a given design specification.
2. design hardware system that meets a given design specification and write VHDL program to implement them.
3. write lab reports documenting the results of the lab experiments.

Relevant ABET 1-7 Student Outcomes:

1. an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics (CLO 1)
3. an ability to communicate effectively with a range of audiences (CLO 3)
6. an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions (CLOs 1, 2)

Grading Policy

Lab assessment	5%	
Quizzes & Final	20%	
Lab.	60%	
Demo	40%	
Report	20%	Writing (10%) Logic Diagram, Wiring Diagram, Software/Code comments, Timing Diagram, etc. (10%)
Pre-lab	15%	Logic Diagram/Tables, Wiring Diagram, Software/Code, Timing Diagram, etc.

Out of the 75% for Pre-Lab and Lab.: Lab. 2 is 5%. Lab. 1, 3, 4, 5, 6 are 10% each. Lab. 7 is 20%.

Laboratory report is due one week after the lab is completed. A sample lab report and the grading rubric are available on canvas.
The quizzes will be conducted during the lecture.

Tentative Schedule

Meeting	**Experiment**
1-2	1
3	2
4-5	3 Quiz 1
6-7	4
8-9	5
10-11	6
12-15	7 Final