Spring 1-1-2020

ECET 215-002: Introduction to Digital Electronics

William Barnes

General Information for ECET 215

Class Hours

Tuesday	10:00 – 12:05	FMH 412
Thursday (lab)	1:00 – 3:05	FMH 304

Office Hours

No official office hours but available before class most days and also during the lab

Snow Delays and Closings, on njit.edu, Announcements:
Day classes by 6 A.M., evening classes by 2 P.M (also notifications by email)

Required Materials for Course
Text: Kleitz, Wm., ***Digital Electronics: A Practical Approach***, Pearson Prentice Hall, latest edition (available in various prices and formats)

Barnes, W., ***ECET 215 Study Guide***, latest version (provided to students during first week)

Barnes, W., ***ECET 215 Lab Manual***, latest version (provided to students during first week)

Grading:

Homework/ Homework quizes	10 %	Tests	25 %
Laboratory Work	35 %	Final Exam	25 %
Professional Society Meeting attendance*			
OR….Technical Journal article*	5 %		

*All students are required to submit, via email only, a report of attendance at a Professional Society Meeting and a report of a Technical Journal article (approved journals are: *EDN*, *Electronic Design*, *IEEE Spectrum*, *Circuit Cellar*, and *Nuts and Volts*).

STUDENT BEHAVIOR	• No eating or drinking is allowed at the lectures, recitations, workshops, and laboratories. • Cellular phones must be turned off during the class hours – if you are expecting an emergency call, leave it on vibrate and inform instructor. • No headphones can be worn in class. • Laptops should be closed during lecture. • During laboratory, if you are finished early, you must show the professor your work before you leave class • Class time should be participative. You should try to be part of a discussion • NJIT Honor Code will be strictly followed in this course
MODIFICATION TO COURSE	The Course Outline may be modified at the discretion of the instructor or in the event of extenuating circumstances. Students will be notified in class of any changes to the Course outline.
COURSE COORDINATOR	Daniel Brateris, ECET Program Coordinator

ECET 215 Lecture Schedule

Materials: Kleitz, ***Digital Electronics, A Practical Approach With VHDL(available in various formats)***
Barnes, W., ***ECET 215 Study Guide***, latest version (provided to students during first week

Week	Date (Tuesday)	Reading	Topics & Activities	Homework
1	1/21	Appendix F	Introduction to Basic DC Circuits	#1 Instructor assigned problems and p. 930: F1-F10, p. 931: F1-F2; p. 932: F3, F4
2	1/28	Ch. 1 and 2	Digital and Analog, Number Systems	#2 p. 25-26: 13, 14, 18 - 20
3	2/4	3.1 – 3.7	Digital Signals, Serial and Parallel Transmission, AND, OR, NOT gates, ICs	#3 p. 57, 60: 1,2, 19, 20; p. 98-100: 4-6, 7b, 8a, 9b, 10a, 12
4	2/11	3.8, 3.9, 3.11, 3.12	NAND, NOR, ICs, Troubleshooting, Alternate Symbols for Gates	#4 p. 102-106 : 26, 28- 32, 35, 41-42
5,6	2/18,25	5.1 – 5.3, 5.5	Combinational Logic, Boolean Laws and Algebra, DeMorgan's Theorem	#5 p. 216- 222: 2, 4- 7, 17-18, 22
7	3/3	5.7 – 5.9	NAND/NOR Universality, POS, SOP, K-maps	#6 p. 223: 31, 32, 35-39
8	3/10	6.1 – 6.4	XOR, XNOR, Parity Circuits, Controlled Inverters; Binary Addition and Subtraction	#7 p. 254- 256: 3 - 7, 10, 12, 14
===== SPRING RECESS =====				
9	3/24	7.1 – 7.10	Two's Complement System and Arithmetic, BCD Arithmetic, Half and Full Adders, Adder ICs, Adder/Subtractor, ALU	#8 p. 304: 5 – 9, 11 e-h, 12 e-h, 15, 20 – 22, 27
10	3/31	8.1 – 8.8	Comparators, Decoding/Encoding, Code Converters, MUXs, DeMUXs, Analog MUX/DeMUX, System Design	#9 p. 371 - : 8.4 - 8.9, 24
11,12	4/7,14,21	10.1 – 10.6, 10.8	Sequential Logic; Registers; SR Latch; D, JK, T Flip Flops; MS and Edge Triggering; IC Flip Flops; FF Function Tables	#10 p. 472 - 478: 1 – 6, 8, 10, 11, 15, 18- 21, 27, 29, 32 **Meeting&Article Reports Deadline**
13,14	4/28	12.1 – 12.9	Sequential Circuit Analysis, Ripple Counters, Modulus, Divide-by-n Counters, Synchronous Counters	#11 p. 613 - 616: 2, 4, 6, 7, 11, 12, 19

NOTES:

1. Students should study the excellent Summary, Review Questions and Glossary for every chapter in the textbook.
2. Although vhdl and Multisim are discussed in the text, they are not required for this course.
3. Tuesday, May 5, NJIT will follow a Saturday schedule, and May 6 - 7 are scheduled to be Reading Days.

ECET 215 Lab Schedule

Lab Manual: Barnes, W, ***ECET 215 Lab Manual (latest version)***

Week	Date (Thursday)	Lab #	Topics	Lab Notebook Checks
1	1/23	(no lab)	Electric Circuit Theory: I,V,R, Ohm's Law, Kirchoff's Laws, Simple Series and Parallel Circuits, Voltage Dividers	
2	1/30	1	Equipment Usage Lab Introduction and Basic DC Circuits Lab	
3	2/6	2	Introduction to the Basic Digital Gates	Lab Book Check #1
4,5	2/13,20	3	Simplification of Boolean Expressions and Their Proof in Hardware	
6,7	2/27, 3/5	4	Binary Arithmetic and a 2-Bit Adder	
8	3/12	5 and 6	Decoders and Multiplexers	Lab Book Check #2
9-10	3/26,4/2	7	Introduction to Flip Flops and Counters	
11-13	4/9,16,23	8	Birthday Display Project	**11/19 Project Full Pin Diagram Due on 4/16**
14	4/30		Lab Makeup and Review	Lab Books Collected

Lab Book: Each lab group will maintain a neat and clear notebook, which will be updated each lab period with a table of contents, student names, date, pin diagrams, answers to all questions in the labs, and initials from instructor as parts of lab are checked. The lab notebook will also list how lab work is distributed among partners for each lab exercise- members are expected to alternate tasks. The lab notebook will be kept with the digital trainer. See the current Lab Manual for more details.

Note 1: Keep in mind that lab work is an important part of the course, counting for 35% of the course grade. Also, the three major tests and final exam will include questions related to lab work.

Note 2: Tuesday, May 5, NJIT will follow a Saturday schedule, and May 6 - 7 are scheduled to be Reading Days.