Fall 2019

ECET 215-001: Introduction to Digital Electronics

William Barnes

COURSE NUMBER	**ECET 215**
COURSE TITLE	**Introduction to Digital Electronics**
COURSE STRUCTURE	2-2-3 (lecture hr/wk - lab hr/wk – course credits)
COURSE DESCRIPTION	The first course in digital electronics develops the fundamentals of the binary system, circuit implementation from Boolean functions and map minimization. Course includes study of combinational logic, sequential logic circuits, flip-flops, counters, and shift register. Computer simulation and laboratory experiments are designed to support the theory and obtain measurement skills.
PREREQUISITE(S)	None
COREQUISITE(S)	None
REQUIRED, ELECTIVE OR SELECTED ELECTIVE	Required
REQUIRED MATERIALS	• Text: Kleitz, ***Digital Electronics, A Practical Approach With VHDL*** • Software: none required • Barnes, ***ECET 215 Lab Manual***
COMPUTER USAGE	Introduction to Multisim
COURSE LEARNING OUTCOMES	By the end of the course students will be able to do the following: 1. Analyze and design simple DC series and parallel circuits making use of KCL, KVL and Ohm's Law 2. Analyze voltage dividers 3. Build and test circuits listed in (1) and (2) 4. Analyze and design simple combinational logic. 5. Analyze and incorporate into circuits the MSI logic including decoders, encoders, multiplexers, demultipexers, adders and subtractors. 6. Build, test and troubleshoot circuits listed in (4) and (5) 7. Describe the operation of basic latches and flip flops 8. Test latches and flip flops and the laboratory 9. Analyze and do some simple design of sequential logic such as counters 10. Build, test and troubleshoot circuits listed in (9) 11. Design a project based on knowledge learned in (1) through (10) 11. Work in teams of two or three students and maintain a lab notebook 12. Appreciate the value of professionalism in class work, projects and career 13. Appreciate the usefulness of, and role of professional societies in, lifelong learning.
RELATED ECET STUDENT OUTCOMES	**Student Outcome a** – an ability to select and apply the knowledge, techniques, skills, and modern tools of their disciplines to broadly-defined engineering technology activities **Related CLO – 4** **Student Outcome f** – an ability to identify, analyze, and solve broadly-defined engineering technology problems **Related CLO – 11**

	Student Outcome h – an understanding of the need for and an ability to engage in self-directed continuing professional development **Related CLO – 13** **Student Outcome e** – an ability to function effectively as a member or leader on a technical team **Related CLO – 11**
CLASS TOPICS	DC circuits, Boolean algebra, gates, combinational and sequential logic, hardware implementations, counters.
GRADING POLICY	Homework. 10%; Labs, 35%; Tests, 25%; Final Exam, 25%; Special Reports, 5%
ACADEMIC INTEGRITY	NJIT has a zero-tolerance policy regarding cheating of any kind and student behavior that is disruptive to a learning environment. Any incidents will be immediately reported to the Dean of Students. In the cases the Honor Code violations are detected, the punishments range from a minimum of failure in the course plus disciplinary probation up to expulsion from NJIT with notations on students' permanent record. Avoid situations where honorable behavior could be misinterpreted. For more information on the honor code, go to http://www.njit.edu/academics/honorcode.php
STUDENT BEHAVIOR	• No eating or drinking is allowed at the lectures, recitations, workshops, and laboratories. • Cellular phones must be turned off during the class hours – if you are expecting an emergency call, leave it on vibrate and inform instructor. • No headphones can be worn in class. • Laptops should be closed during lecture. • During laboratory, if you are finished early, you must show the professor your work before you leave class • Class time should be participative. You should try to be part of a discussion
MODIFICATION TO COURSE	The Course Outline may be modified at the discretion of the instructor or in the event of extenuating circumstances. Students will be notified in class of any changes to the Course outline.
COURSE INSTRUCTOR	William E. Barnes, Prof. Emeritus
COURSE COORDINATOR	Daniel Brateris

General Information for ECET 215

Class Hours

Tuesday (lab)	1:00 – 3:05	FMH 204A
Thursday	1:00 – 3:05	FMH 405

Office Hours (GITC 2101)

No official office hours but available before class most days and also during the lab

Snow Delays and Closings, on njit.edu, Announcements:
Day classes by 6 A.M., evening classes by 2 P.M (also notifications by email)

Required Materials for Course
Text: Kleitz, Wm., ***Digital Electronics: A Practical Approach***, Pearson Prentice Hall, latest edition

Class Notes: Barnes, W., ***ECET 215 Class Notes***, latest version (provided to students during first week)

Lab Manual: Barnes, W., ***ECET 215 Lab Manual***, latest version (provided to students during first week)

Grading:

Homework/ Homework quizes	10 %	Tests	25 %
Laboratory Work	35 %	Final Exam	25 %
Professional Society Meeting attendance*			
OR….Technical Journal article*	5 %		

*All students are required to submit, via email only, a report of attendance at a Professional Society Meeting and a report of a Technical Journal article (approved journals are: *EDN*, *Electronic Design*, *IEEE Spectrum*, *Circuit Cellar*, and *Nuts and Volts*).

STUDENT BEHAVIOR	• No eating or drinking is allowed at the lectures, recitations, workshops, and laboratories. • Cellular phones must be turned off during the class hours – if you are expecting an emergency call, leave it on vibrate and inform instructor. • No headphones can be worn in class. • Laptops should be closed during lecture. • During laboratory, if you are finished early, you must show the professor your work before you leave class • Class time should be participative. You should try to be part of a discussion • NJIT Honor Code will be strictly followed in this course
MODIFICATION TO COURSE	The Course Outline may be modified at the discretion of the instructor or in the event of extenuating circumstances. Students will be notified in class of any changes to the Course outline.
COURSE COORDINATOR	Daniel Brateris

ECET 215 Lecture Schedule

Text: Kleitz, ***Digital Electronics, A Practical Approach With VHDL***

Week	Date (Thur.)	Reading	Topics & Activities	Homework
1	9/5	Appendix F	Electric Circuit Theory: I,V,R, Ohm's Law, Kirchoff's Laws, Simple Series and Parallel Circuits, Voltage Dividers	#1 Instructor assigned problems and p. 930: F1-F10, p. 931: F1-F2
2	9/12	Ch. 1 and 2	Digital and Analog, Number Systems	#2 p. 932: F3, F4 p. 25-26: 13, 14, 18 - 20
3	9/19	3.1 – 3.7	Digital Signals, Serial and Parallel Transmission, AND, OR, NOT gates, ICs	#3 p. 57, 60: 1,2, 19, 20; p. 98-100: 4-6, 7b, 8a, 9b, 10a, 12
4	9/26	3.8, 3.9, 3.11, 3.12	NAND, NOR, ICs, Troubleshooting, Alternate Symbols for Gates	#4 p. 102-106 : 26, 28- 32, 35, 41-42
5,6	10/3, 10/10	5.1 – 5.3, 5.5	Combinational Logic, Boolean Laws and Algebra, DeMorgan's Theorem	#5 p. 216- 222: 2, 4- 7, 17-18, 22
7	10/17	5.7 – 5.9	NAND/NOR Universality, POS, SOP, K-maps	#6 p. 223: 31, 32, 35-39
8	10/24	6.1 – 6.4	XOR, XNOR, Parity Circuits, Controlled Inverters; Binary Addition and Subtraction	#7 p. 254- 256: 3 - 7, 10, 12, 14
9	10/31	7.1 – 7.10	Two's Complement System and Arithmetic, BCD Arithmetic, Half and Full Adders, Adder ICs, Adder/Subtractor, ALU	#8 p. 304: 5 – 9, 11 e-h, 12 e-h, 15, 20 – 22, 27
10	11/7	8.1 – 8.8	Comparators, Decoding/Encoding, Code Converters, MUXs, DeMUXs, Analog MUX/DeMUX, System Design	#9 p. 371 - : 8.4 - 8.9, 24
11,12	11/14, 11/21, 11/26	10.1 – 10.6, 10.8	Sequential Logic; Registers; SR Latch; D, JK, T Flip Flops; MS and Edge Triggering; IC Flip Flops; FF Function Tables	#10 p. 472 - 478: 1 – 6, 8, 10, 11, 15, 18- 21, 27, 29, 32 **Meeting&Article Reports Deadline**
13,14	12/5	12.1 – 12.9	Sequential Circuit Analysis, Ripple Counters, Modulus, Divide-by-n Counters,Synchronous Counters	#11 p. 613 - 616: 2, 4, 6, 7, 11, 12, 19

NOTES:

1. Study the excellent Summary, Review Questions and Glossary for every chapter in the textbook.

2. Although vhdl and Multisim are used in the text, they are not required for this course.

ECET 215 Lab Schedule

Lab Manual: Barnes, W, ***ECET 215 Lab Manual***

Week	Date (Tues.)	Lab Number	Topics	Report
1	9/3		Lecture: Introduction to Basic DC Circuits and Equipment Usage	
2	9/10	1	Lab Introduction and Basic DC Circuits Lab	
3	9/17	2	Introduction to the Basic Digital Gates	Lab Book Check
4,5	9/24, 10/1	3	Simplification of Boolean Expressions and Their Proof in Hardware	
6,7	10/8, 15	4	Binary Arithmetic and a 2-Bit Adder	Lab Book Check
8	10/22	5 and 6	Decoders and Multiplexers	
9-10	10/29, 11/5	7	Introduction to Flip Flops and Counters	
11-13	11/12, 11/19, 12/3	8	Birthday Display Project	**11/19 Full Pin Diagram Due**
14	12/10		Makeup and Review	Lab Books Collected

Lab Book: Each lab group will maintain a neat and clear notebook, which will be updated each lab period with names, date, pin diagrams, answers to all questions in the labs, and initials from instructor as parts of lab are checked that they have been properly performed. Besides documenting lab work, the lab notebook will also list how lab work is distributed among partners for each lab exercise- members are expected to alternate tasks. The lab notebook will be kept with the digital trainer. See more details in the Lab Manual.

Note 1: Lab work is an important part of the course, counting for 35% of the course grade, and also there will be some questions related to labs on the tests.

Note 2: December 12 and 13 are scheduled to be Reading Days.